

Features

- Dual-side cooled package with lowest junction-top thermal resistance
- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

Product Summary			
V_{DS}	$R_{DS(on)}$ (m Ω) Typ	I_D (A)	Q_g (Typ)
40V	0.67 @ 10V 20A	444	108nc

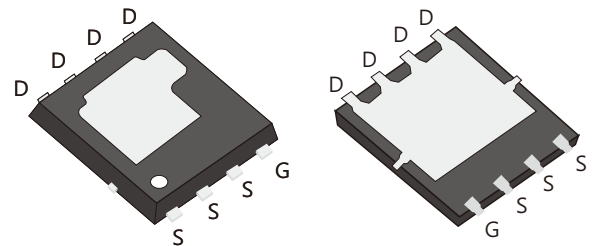
DFN5×6
DS0067N04GT3

Mechanical Data

- Case:DFN5×6 Package

Application

- Switching Application
- SR (Synchronous rectification)
- DC/DC converter
- General purpose applications



Ordering Information

Part No.	Marking.	Package Type	Package	Quantity(box)
DS0067N04GT3	DS0067N04GT3	DFN5×6	Tape & Reel	5000

Block Diagram

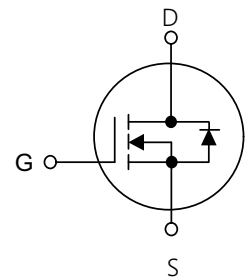


Table1 Absolute Maximum Ratings ($T_c=25^\circ\text{C}$, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 5)	$T_c=25^\circ\text{C}$ (Silicon limit)	I_D	444	A
	$T_c=100^\circ\text{C}$ (Silicon limit)		280	
Pulsed Drain Current (Note 1)		I_{DM}	1700	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	1369	mJ
Power Dissipation $T_c=25^\circ\text{C}$		P_D	266	W
Operating Junction and Storage Temperature		T_J/T_{STG}	$-55\sim+150$	$^\circ\text{C}$

Table 2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	43.2	$^{\circ}\text{C}/\text{W}$
Thermal resistance Junction to Case, bottom	$R_{\theta JC}$	0.47	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V,I _D =250μA	40	-	-	V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =20V,V _{DS} =0V	-	-	100	nA
	Reverse		V _{GS} = -20V,V _{DS} =0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} ,I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V,I _D =20A	-	0.67	0.9	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C _{ISS}	V _{DS} =20V,V _{GS} =0V,f=1MHz	-	6600	-	pF
Output Capacitance		C _{OSS}		-	2073	-	pF
Reverse Transfer Capacitance		C _{RSS}		-	248	-	pF
Gate Resitance		R _G	f=1MHz	-	1.2	-	Ω
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V _{DS} =20V,R _G =1.5Ω V _{GS} =10V	-	20	-	ns
Turn-On Rise Time		tr		-	145	-	ns
Turn-Off Delay Time		td(off)		-	55	-	ns
Turn-Off Fall Time		tf		-	18	-	ns
Total Gate Charge		Q _G	V _{DS} =20V,I _D =20A, V _{GS} =10V	-	108	-	nC
Gate-Source Charge		Q _{GS}		-	25	-	nC
Gate-Drain Charge		Q _{GD}		-	27	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Reverse Recovery Time		trr	V _{GS} =0V,I _F =20A	-	68	-	ns
Reverse Recovery Charge		Q _{RR}	dI _F /dt=100A/μs	-	120	-	nC

Notes: 1 Repetitive Rating: Pulse width limited by maximum junction temperature
2 $L=0.5\text{mH}$, $V_{GS}=10V$, Starting $T_J=25^{\circ}\text{C}$
3 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
4 Guaranteed by design, not subject to production
5 The maximum current is limited by the package.

Typical Characteristics Diagrams

Figure 1. Output Characteristics

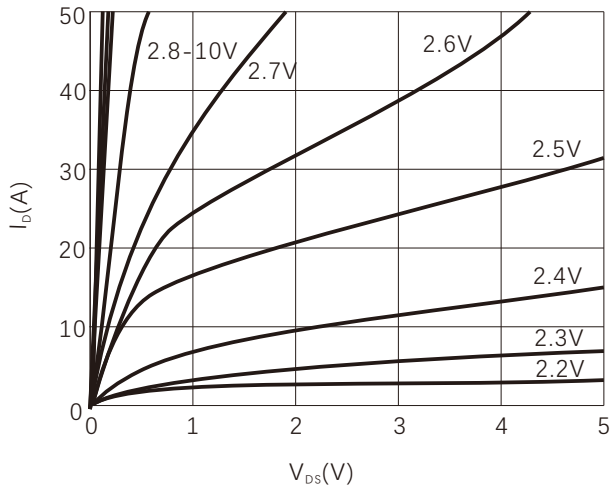


Figure 2. Normalized $R_{DS(on)}$ vs Temperature

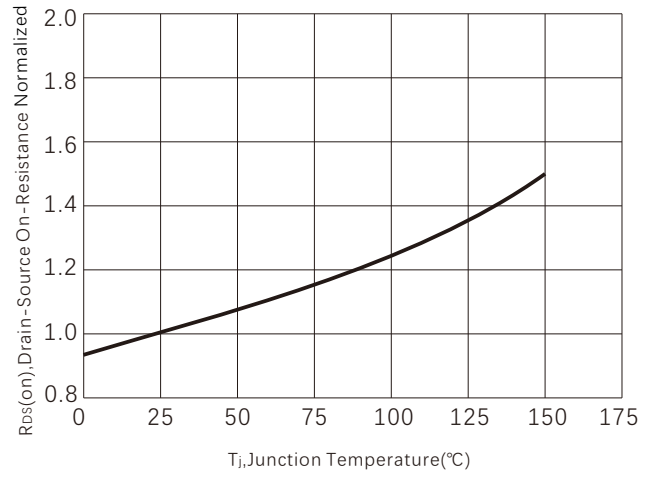


Figure 3. On-Resistance vs. Drain Current

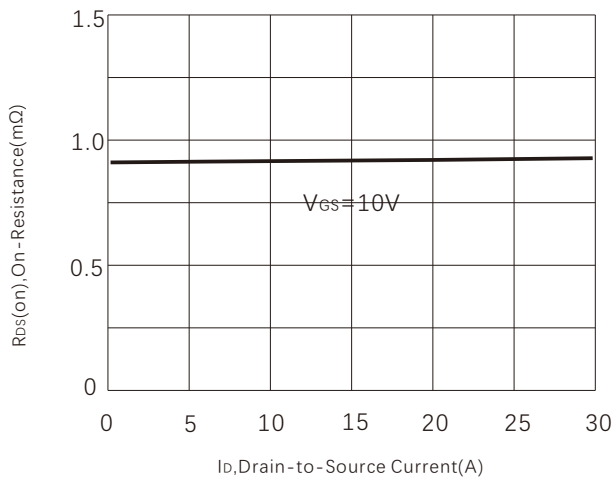


Figure 4. Capacitance

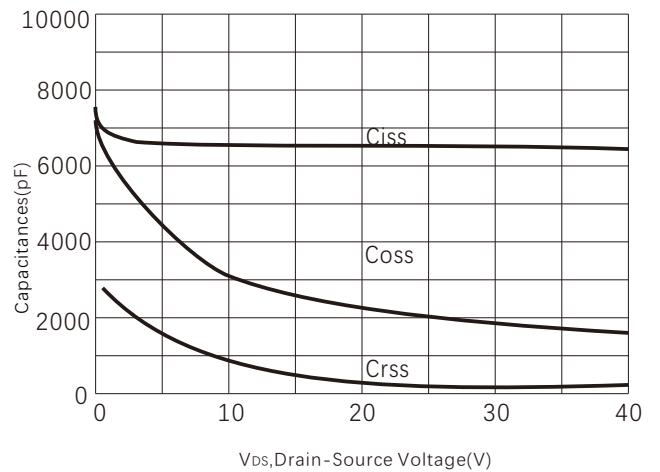


Figure 5. Gate charge

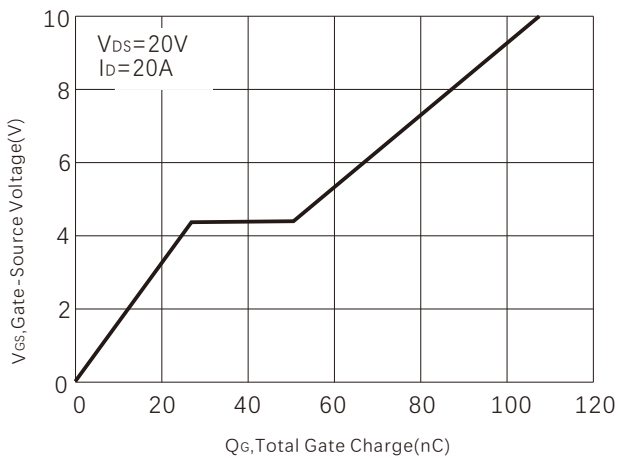


Figure 6. Source-Drain Diode Forward Voltage

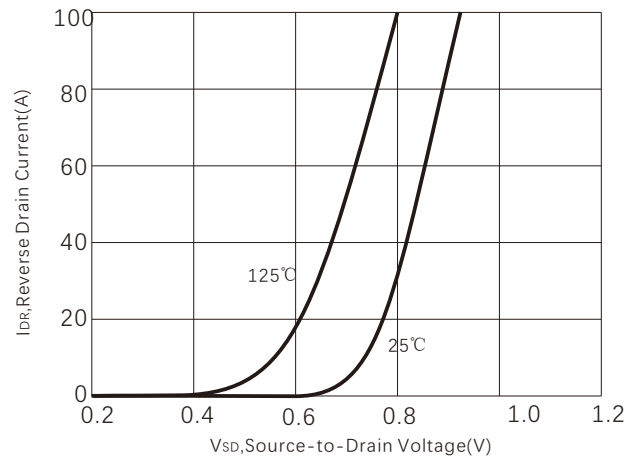


Figure 7. Transfer Characteristics

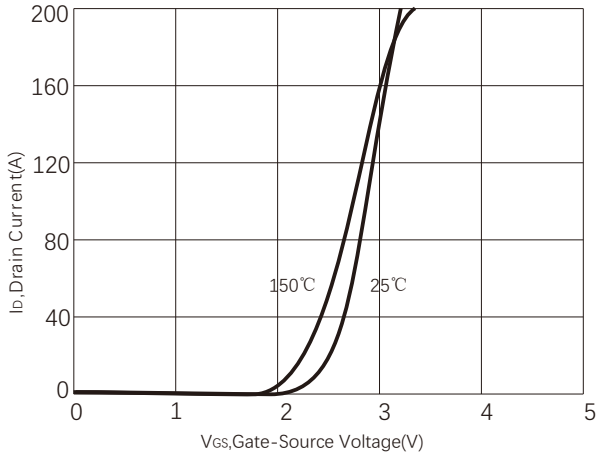


Figure 8. Power dissipation

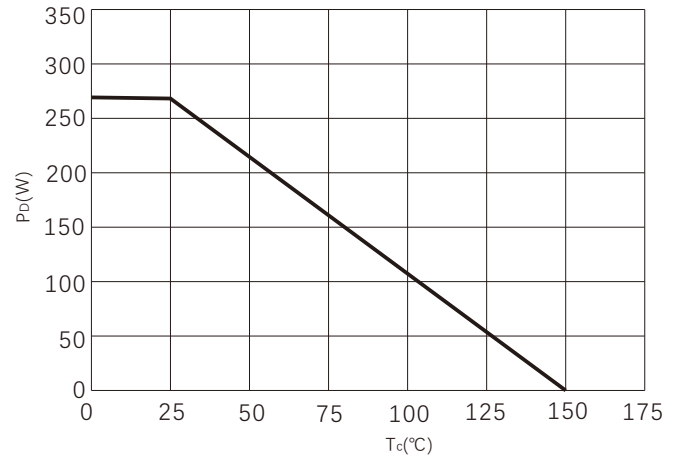


Figure 9.

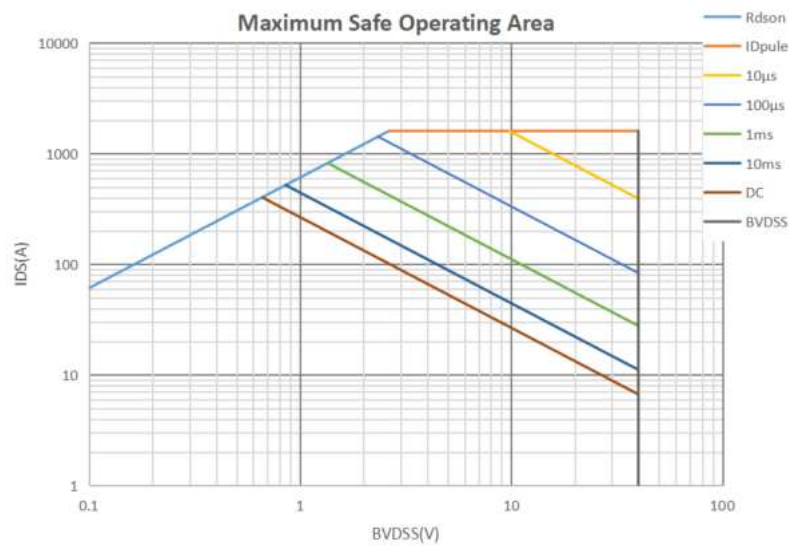
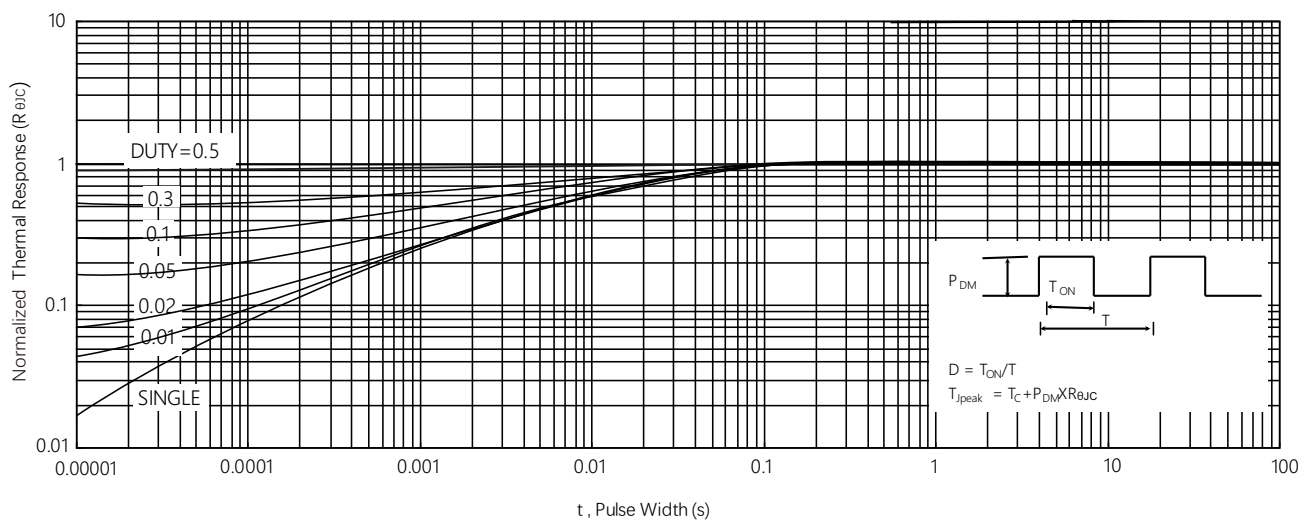
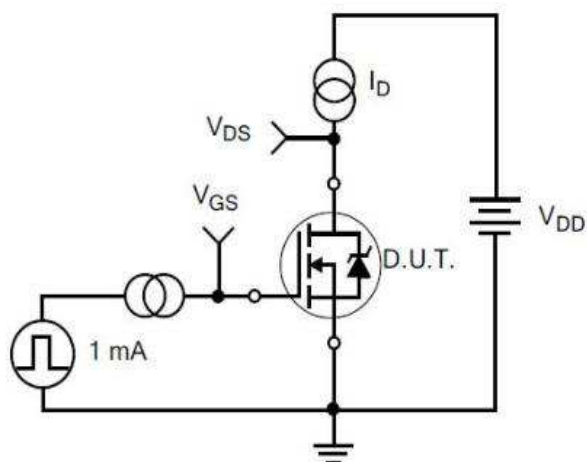


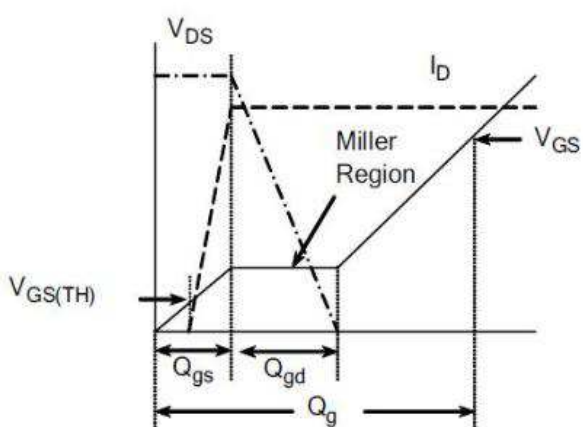
Figure 10. Normalized Maximum Transient Thermal Impedance



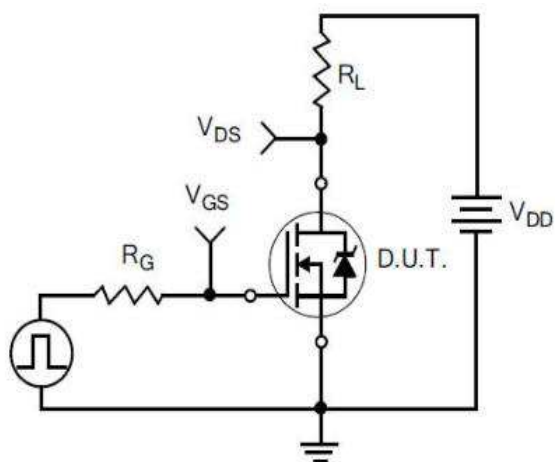
Typical Test Circuit



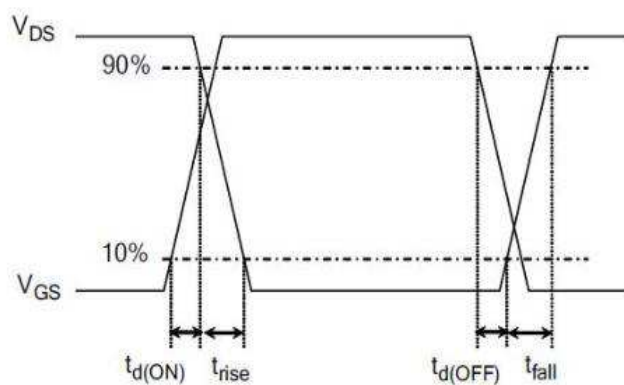
1) Gate Charge Test Circuit



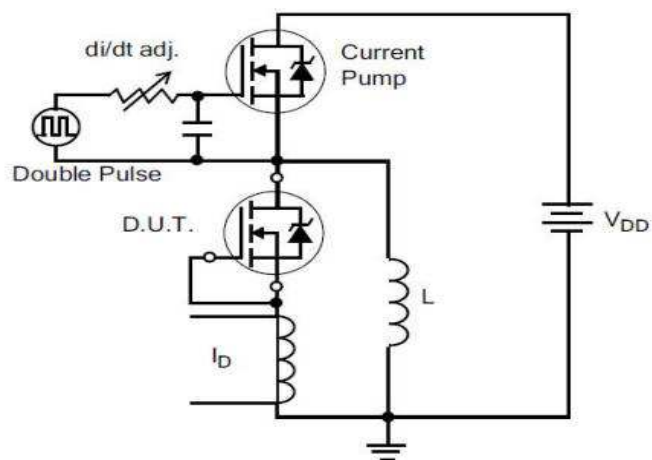
2) Gate Charge Waveform



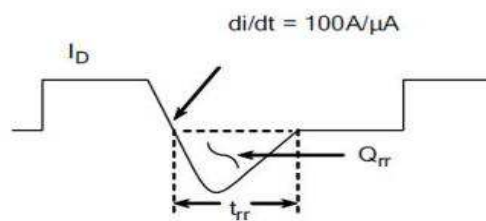
3) Resistive Switching Test Circuit



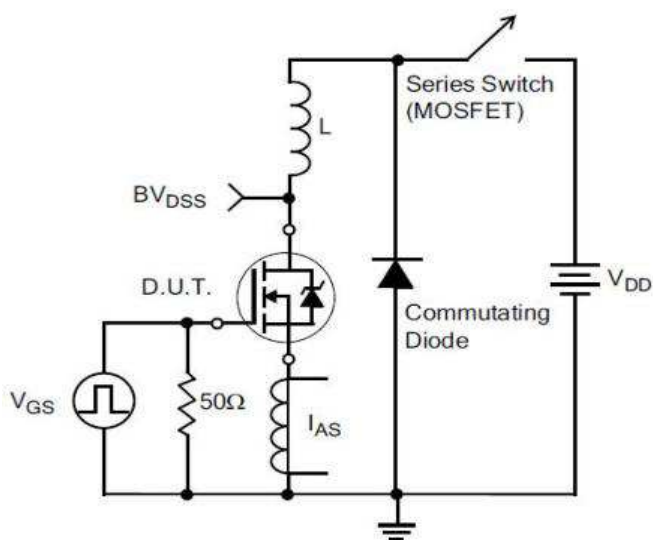
4) Resistive Switching Waveforms



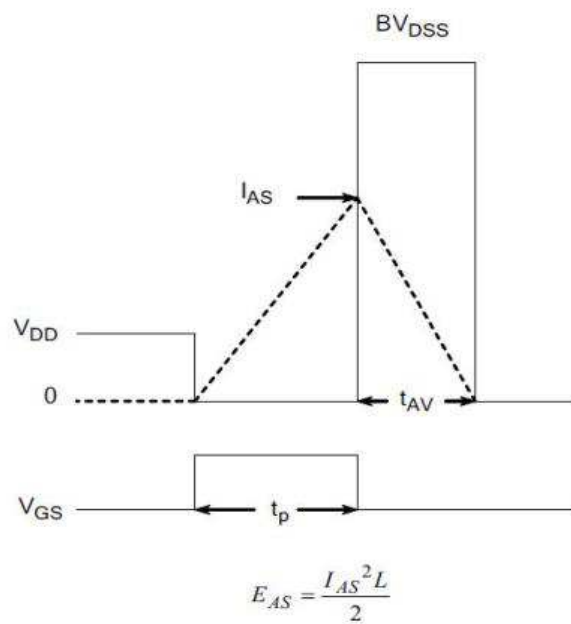
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

Product Names Rules

X X X X N E X X X

Process Type:
VDMOS:default
Super junction:SJ
Low Voltage trench:D

Rated Current Code
With 3 Digital,
For Example:
6.7mΩ:067,
10mΩ:010,

Channel Code
N channel:N
P channel:P

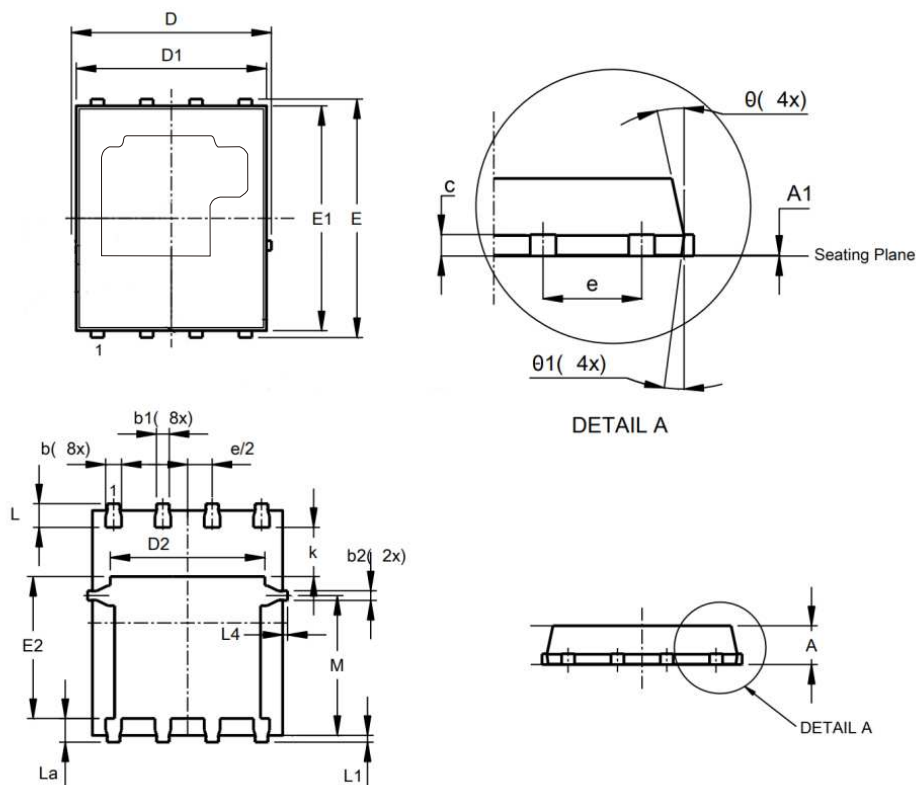
Package Code
TO-220:Default
ITO-220:F
TO-262:E
TO-263:D
TO-252:M
TO-251:N
TO-263-7L:D7
TOLL:T
DFN5×6:G

Rated Voltage Code
With 2 Digital,For Example:
600V:60
60V:06

Special Function Code
G-S ESD Protection:E
No Protection:Default

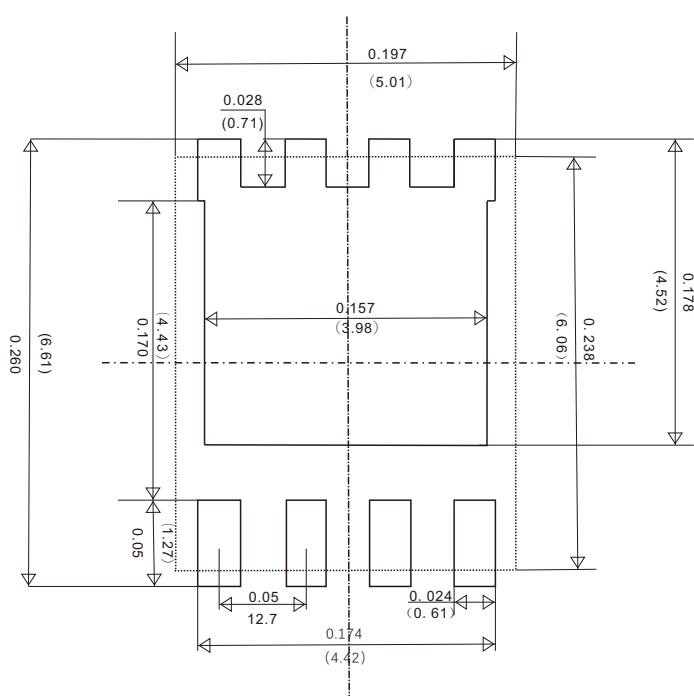
Dimensions

DFN5×6 PACKAGE OUTLINE DIMENSIONS



Dim	Min	Max	Type
A	0.90	1.10	1.00
b	0.23	0.41	0.32
b1	0.24	0.30	0.27
b2	0.16	0.32	0.23
c	0.17	0.27	0.22
D	-	-	5.01
D1	4.80	4.95	4.88
D2	-	-	3.98
E	-	-	6.06
E1	5.72	5.82	5.77
E2	3.42	3.52	3.47
k	-	-	1.33
L	0.56	0.66	0.61
La	0.57	0.67	0.63
L1	0.06	0.15	0.11
L4	-	-	0.06
M	3.00	3.20	3.08
ϕ	10	11	10.39

Suggested Pad Layout



Friendship Reminder

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