

General Description

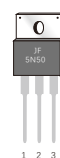
5N50 the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220, which accords with the RoHS standard.



Product Summary			
V _{DS}	R _{DS(on)} (Ω)Typ	I _D (A)	Q _g (Typ)
500V	1.35 @ 10V,2.5A	5	12.5nc

TO-220

5N50



Features

- Low on-resistance
- Low gate charge and Fast Switching
- 100% avalanche tested
- Rohs compliant

Mechanical Data

- Case:TO-220 Package

Application

- Power switch circuit of adaptor and charger

Block Diagram

Pin Definition:

- 1.Gate
- 2.Drain
- 3.Source

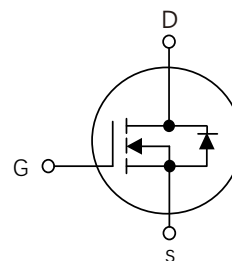


Table1 Absolute Maximum Ratings (T_c=25°C, unless otherwise specified)

Parameters	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	500	V
Gate-Source Voltage	V _{GS}	±30	V
Contionous Drain Current	I _D	T _C =25°C	5
		T _C =100°C	3.1
Pulsed Drain Current (Note 1)	I _{DM}	20	A
Single Pulse Avalanche Energy(Note 2)	EAS	210	mJ
Reverse Diode Recovery dv/dt(Note 3)	dv/dt	5.0	V/ns
Power Dissipation T _C =25°C	P _D	75	W
Operating Junction and Storage Temperature	T _J /T _{STG}	-55 ~ +150	°C

Table 2. Thermal Characteristics

Parameters	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	96.5	$^{\circ}\text{C}/\text{W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	1.67	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V,I _D =250μA	500			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =500V,V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =30V,V _{DS} =0V			10	μA
	Reverse		V _{GS} = -30V,V _{DS} =0V			-10	μA
On Characteristics(Note 4)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} ,I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V,I _D =2.5A		1.35	1.45	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C _{ISS}	V _{DS} =25V,V _{GS} =0V,f=1MHz		520		pF
Output Capacitance		C _{OSS}			40		pF
Reverse Transfer Capacitance		C _{RSS}			2.3		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		t _{d(on)}	V _{DD} =250V,I _D =5A, V _{GS} =10V,R _G =10Ω		10		ns
Turn-On Rise Time		t _r			9		ns
Turn-Off Delay Time		t _{d(off)}			28		ns
Turn-Off Fall Time		t _f			13		ns
Total Gate Charge		Q _G	V _{DS} =250V,I _D =5A, V _{GS} =10V		12.5		nC
Gate-Source Charge		Q _{GS}			2.7		nC
Gate-Drain Charge		Q _{GD}			6		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V,I _S =5A			1.5	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I _S				5	A
Reverse Recovery Time		t _{rr}	V _{GS} =0V,I _S =5A		318		ns
Reverse Recovery Charge		Q _{RR}	dI _F /dt=100A/μs(Note 4)		1520		nC

Notes: 1 Repetitive Rating: Pulse width limited by maximum junction temperature
2 $L=10\text{mH}, I_D=5.3A$, Starting $T_J=25^{\circ}\text{C}$
3 $I_{SD}=5A, di/dt \leq 100A/\mu s, V_{DD} \leq BV_{DSS}$, starting $T_J=25^{\circ}\text{C}$
4 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
5 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

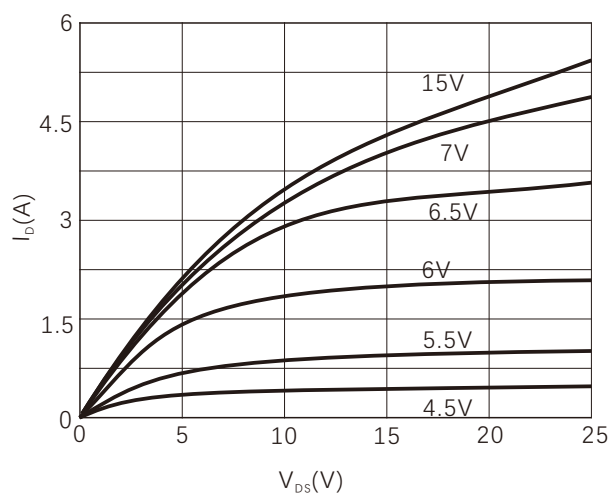


Figure 2. $R_{DS(ON)}$ vs Junction Temperature

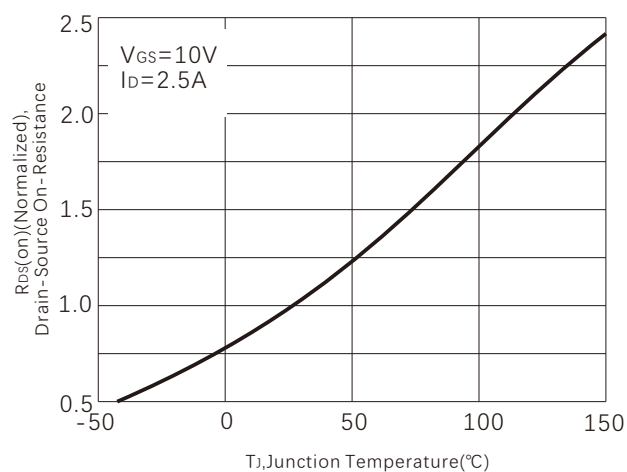


Figure 3. $R_{DS(on)}$ vs. Drain Current

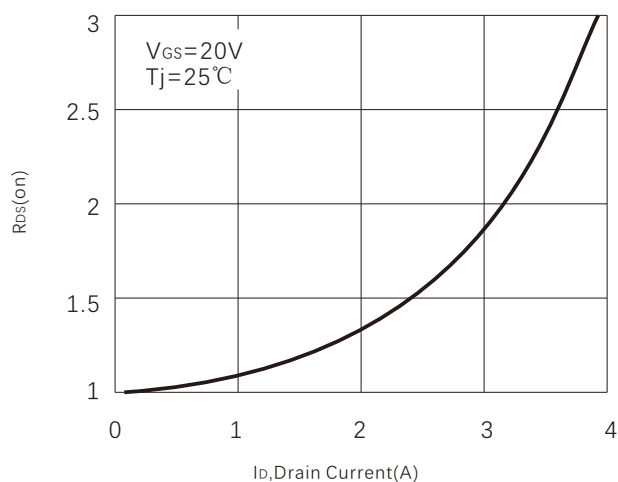


Figure 4. Capacitance

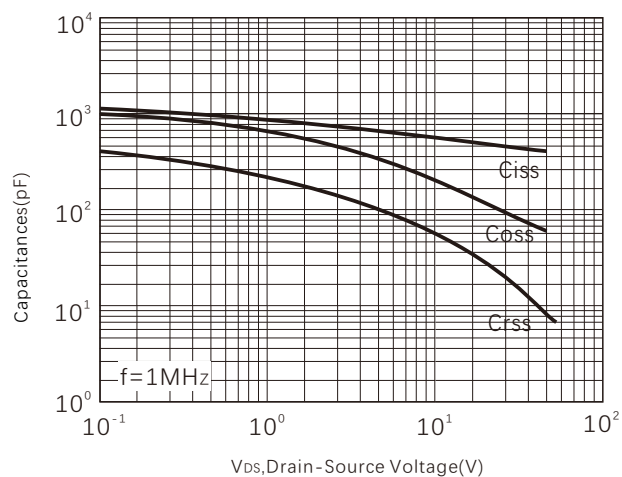


Figure 5. Gate charge

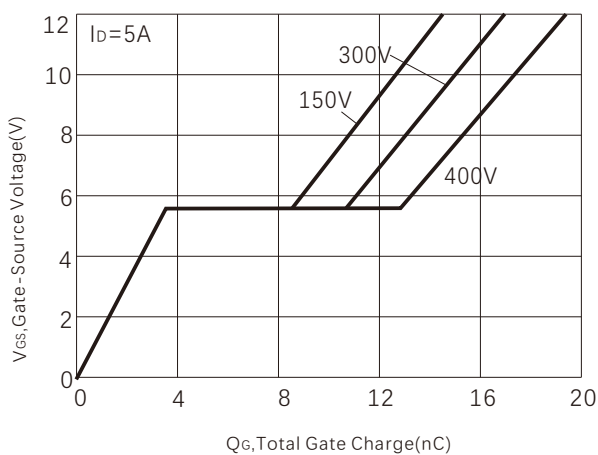


Figure 6. Typical Body Diode Transfer Characteristics

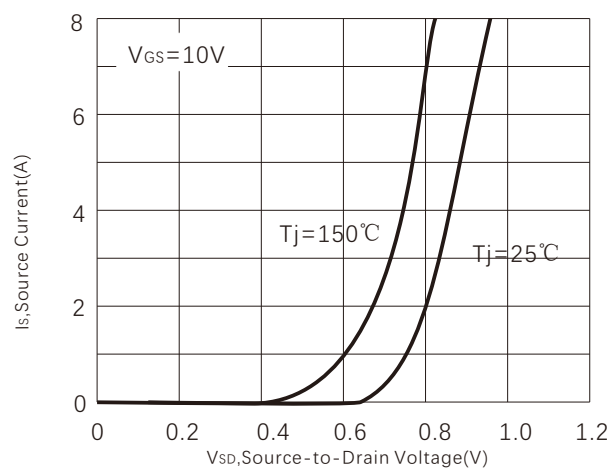


Figure7.Power dissipation

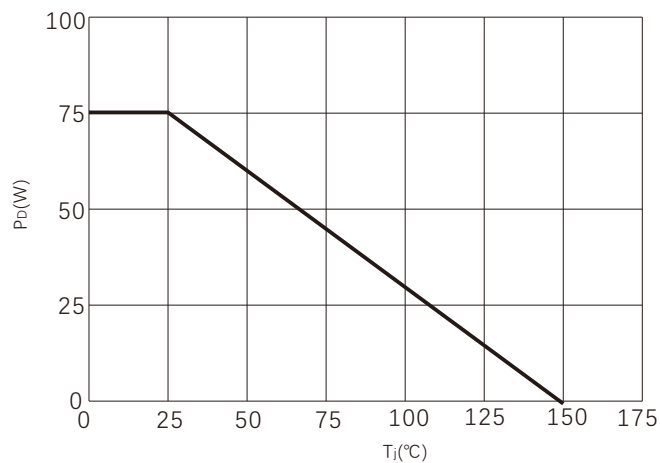


Figure 8. Safe operating area

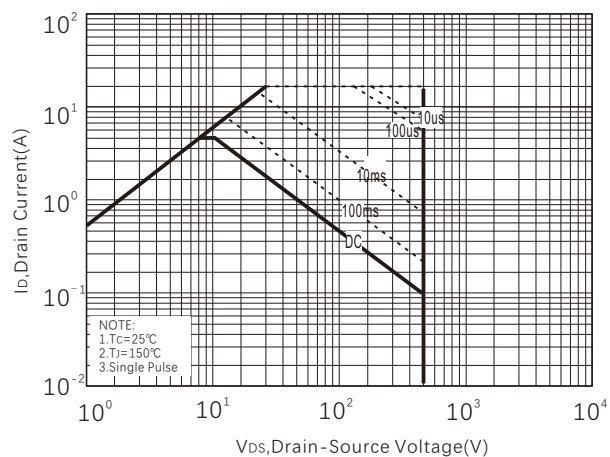


Figure 9. Drain Current

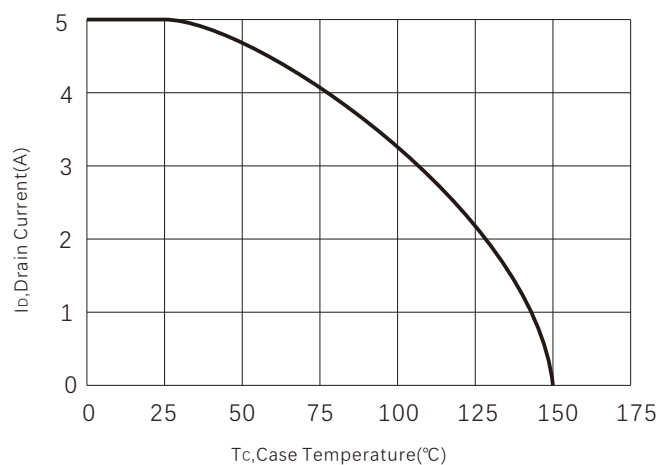
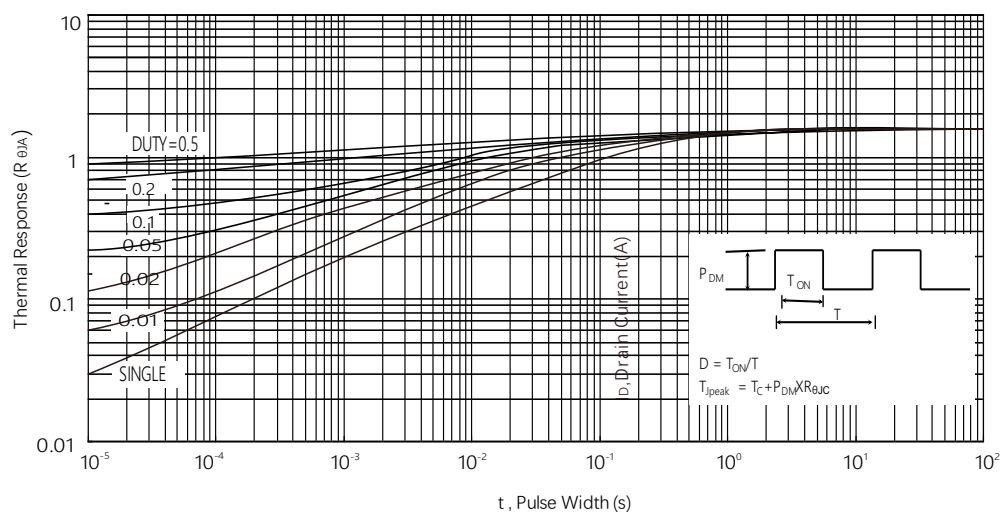
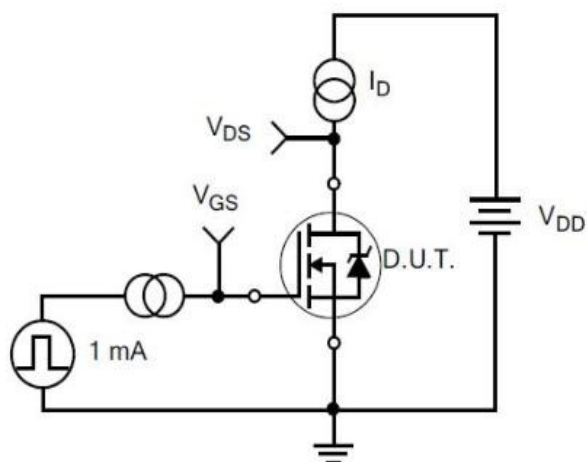


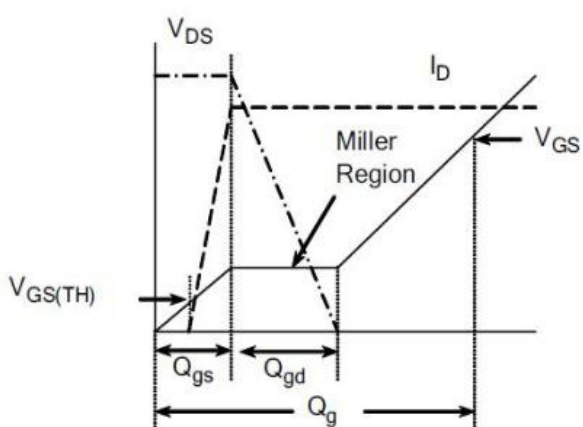
Figure 10. Maximum Transient Thermal Impedance



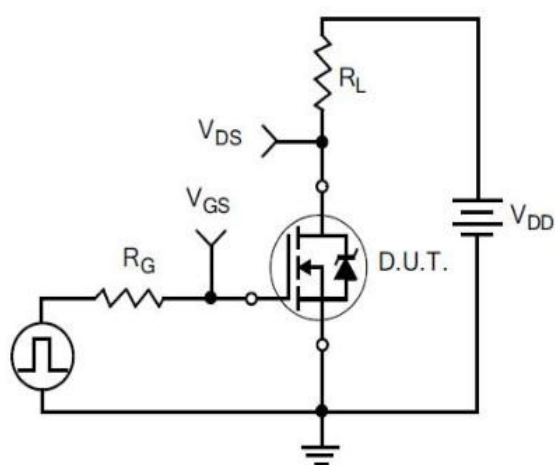
Typical Test Circuit



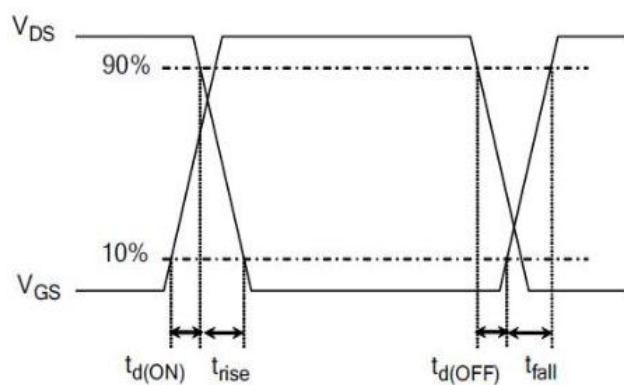
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

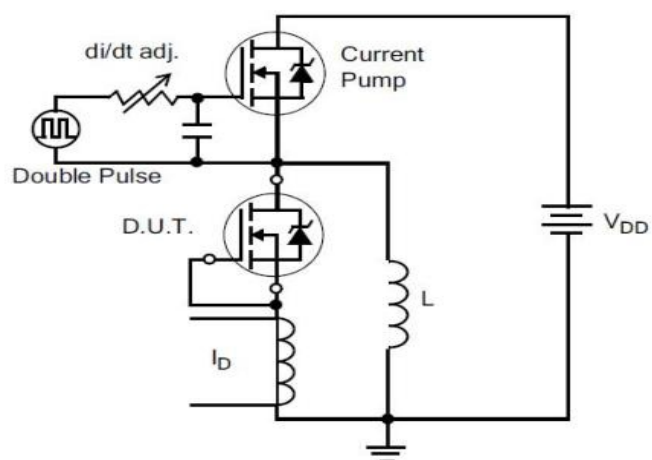


3) Resistive Switching Test Circuit

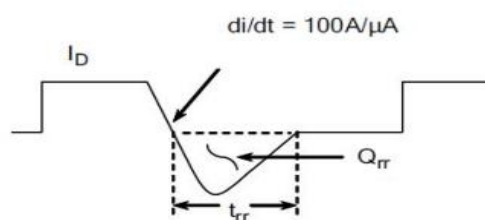


4) Resistive Switching Waveforms

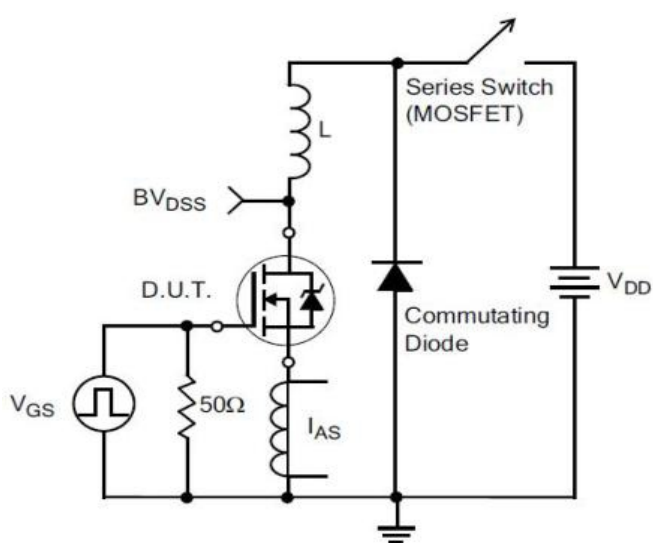
Typical Test Circuit



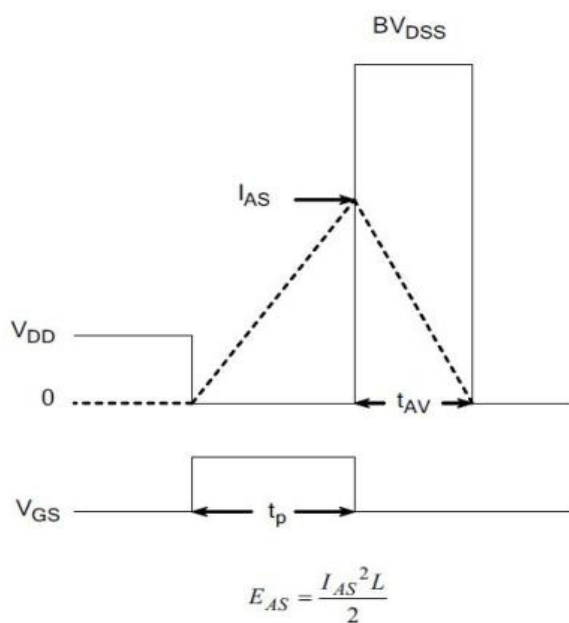
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

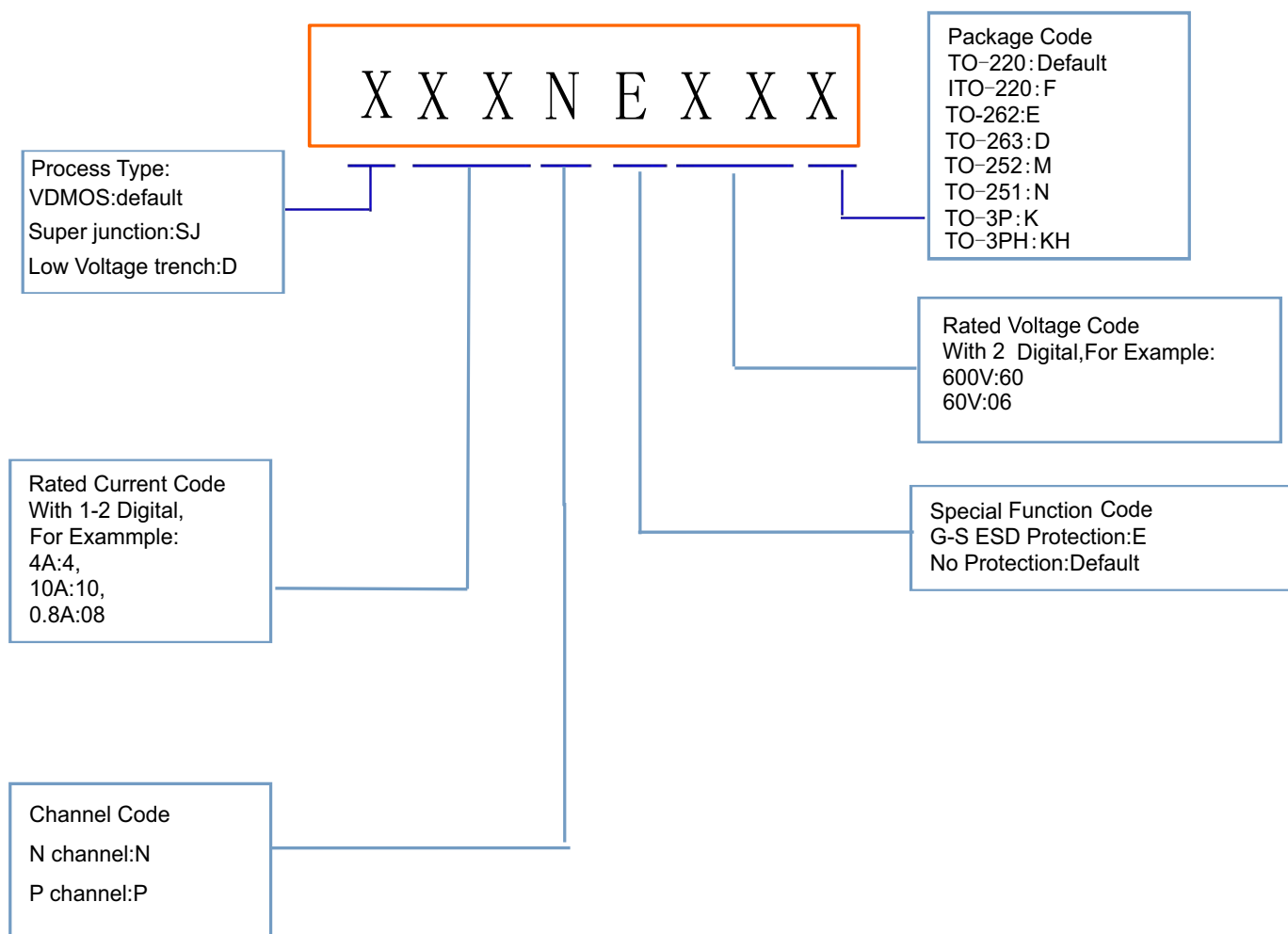


7) . Unclamped Inductive Switching Test Circuit



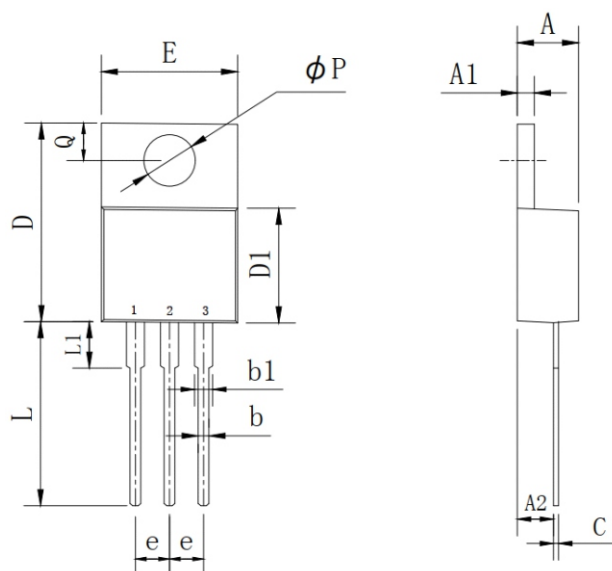
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-220 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	4.25	4.87	0.167	0.192
A1	1.07	1.47	0.042	0.058
A2	2.03	2.92	0.080	0.115
b	0.51	1.11	0.020	0.044
b1	0.97	1.6	0.038	0.063
C	0.3	0.7	0.012	0.028
D	14.6	15.9	0.575	0.626
D1	8.04	9.3	0.317	0.366
E	9.57	10.57	0.377	0.416
e	2.34	2.74	0.092	0.108
L	12.58	14.3	0.495	0.563
L1	2.8	4.2	0.110	0.165
P	3.4	4.14	0.134	0.163
Q	2.45	3	0.096	0.118

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