SEMICONDUCTOR

DS021N10T

246A 100V N-Channel Enhancement Mode Power MOSFET

Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

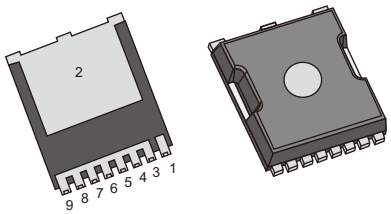
Product Summary			
V_{DS}	$R_{DS(on)}$ (mΩ) Typ	I_D (A)	Qg (Typ)
100V	2.1 @ 10V 40A	246	169nc

Mechanical Data

- Case:TOLL Package

TOLL

DS021N10T



Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

Ordering Information

Part No.	Marking.	Package Type	Package	Quality(box)
DS021N10T	DS021N10T	TOLL	Tape & Reel	2000

Pin Definition:

1. Gate
2. Drain

3/4/5/6/7/8/9. Source

Block Diagram

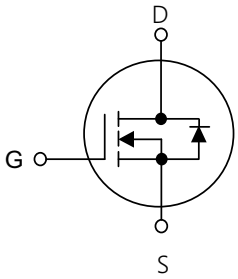


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	246	A
	T_C=100°C		155	
Pulsed Drain Current (Note 1)		I_{DM}	960	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	1521	mJ
Power Dissipation	T_C=25°C	P_D	272	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient. Max	$R_{\theta JA}$	40.0	°C/W
Thermal resistance Junction to Case. Max	$R_{\theta JC}$	0.46	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	100	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	-	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=40A	-	2.1	2.5	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=40V,V_{GS}=0V,f=1MHz	-	9162	-	pF
Output Capacitance		C_{OSS}		-	2148	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	168	-	pF
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DS}=50V, V_{GS}=10V,R_G=3Ω,	-	35	-	ns
Turn-On Rise Time		t_R		-	111	-	ns
Turn-Off Delay Time		td(off)		-	84	-	ns
Turn-Off Fall Time		tf		-	112	-	ns
Total Gate Charge		Q_G	V_{DS}=50V,I_D=40A, V_{GS}=10V	-	169	-	nC
Gate-Source Charge		Q_{GS}		-	67	-	nC
Gate-Drain Charge		Q_{GD}		-	30	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=40A	-	-	1.2	V
Reverse Recovery Time		trr	I_F=100A,dI_F/dt=100A/μs	-	101	-	ns
Reverse Recovery Charge		Q_{RR}	I_F=100A,dI_F/dt=100A/μs	-	338	-	nC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L = 0.5mH, R_G = 25Ω,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

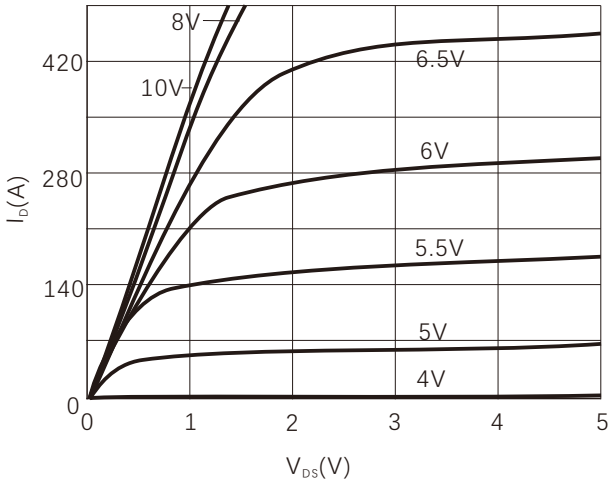


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

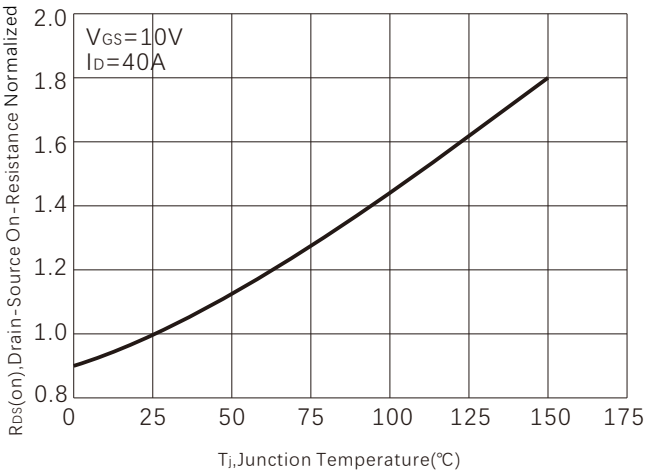


Figure 3.On-Resistance vs.Drain Current

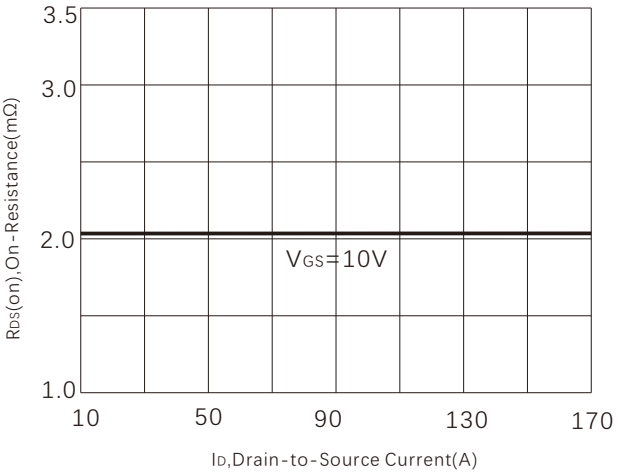


Figure 4. Capacitance

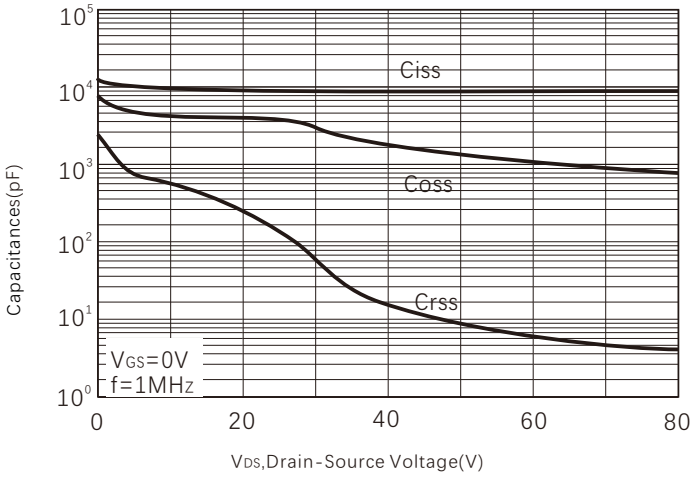


Figure 5.Gate charge

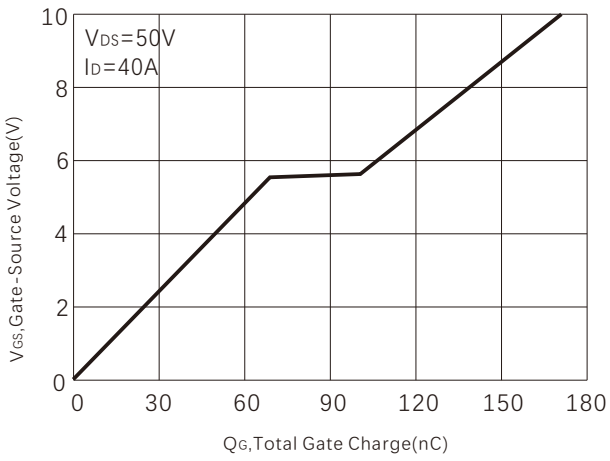


Figure 6.Source-Drain Diode Forward Voltage

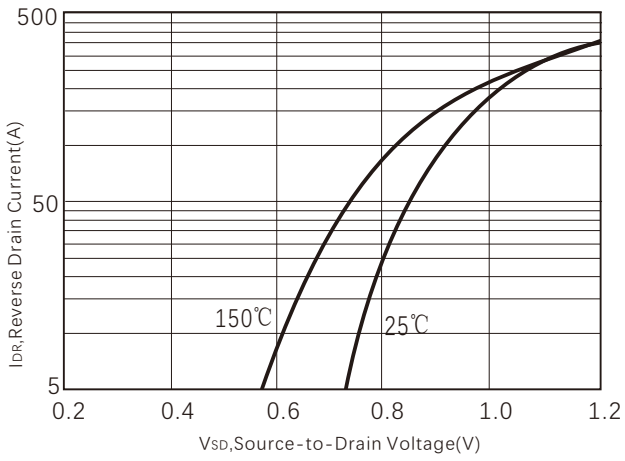


Figure7.Maximum Drain Current vs Temperature

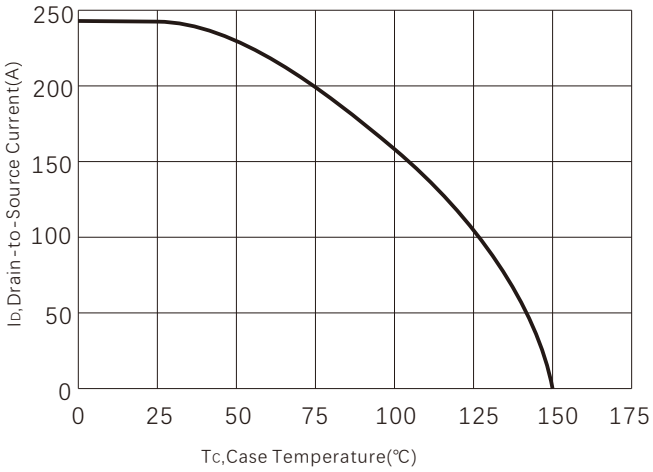


Figure 8. Power dissipation

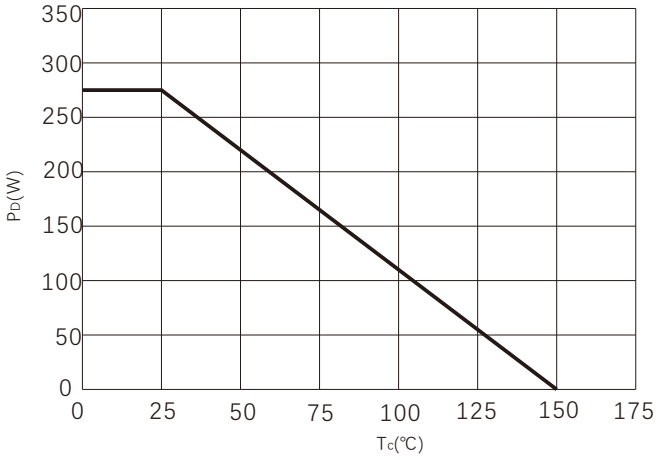


Figure 9.

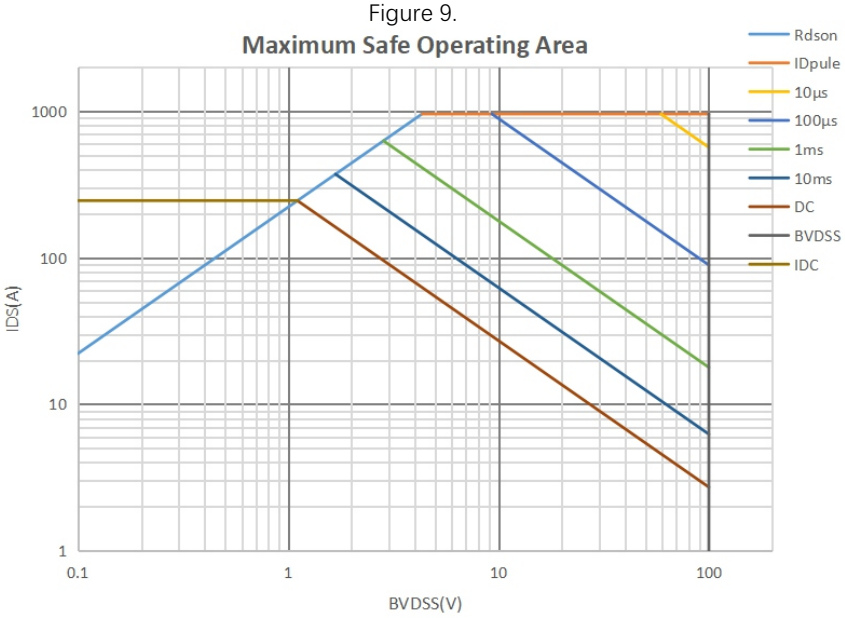
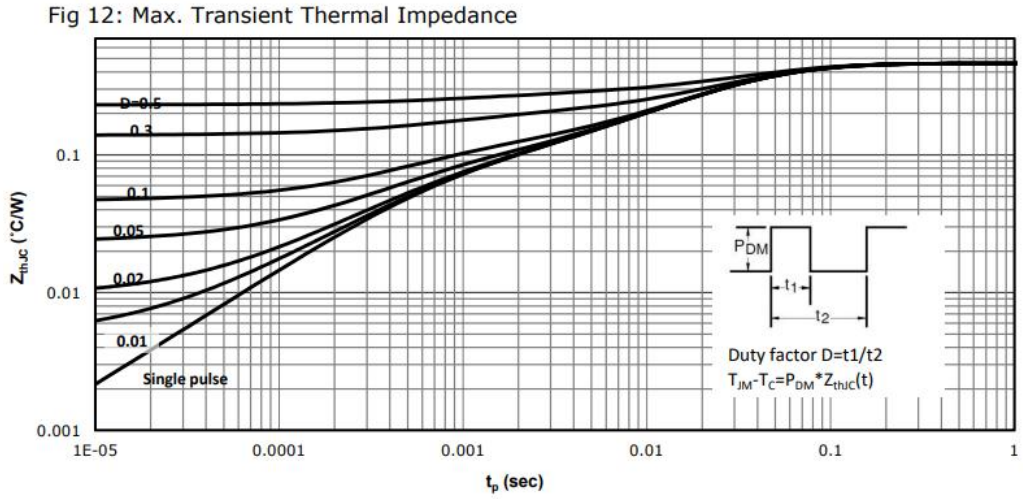
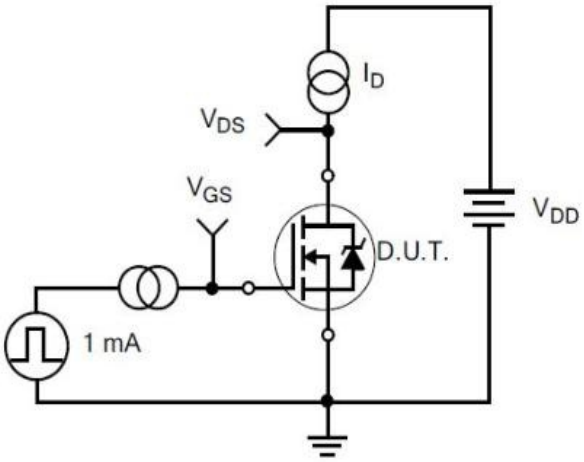


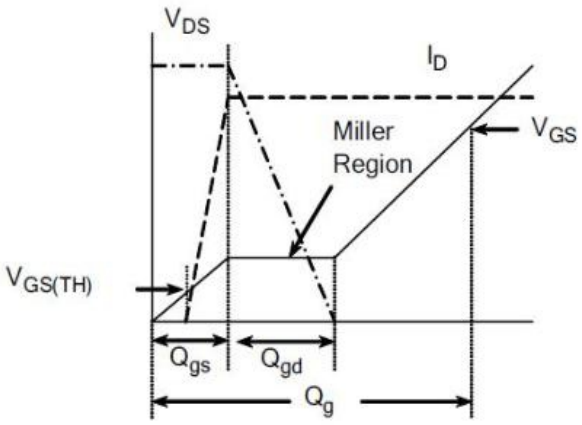
Figure 10. Maximum Transient Thermal Impedance



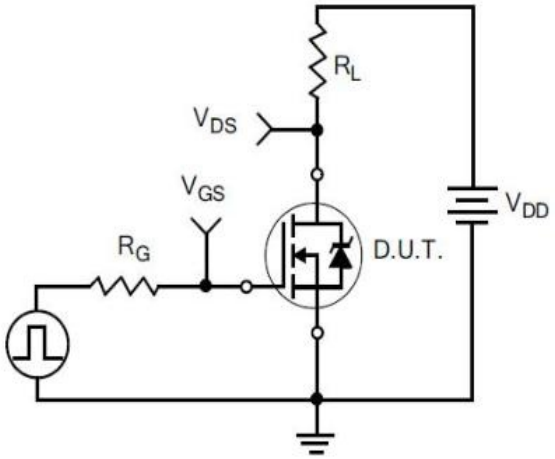
Typical Test Circuit



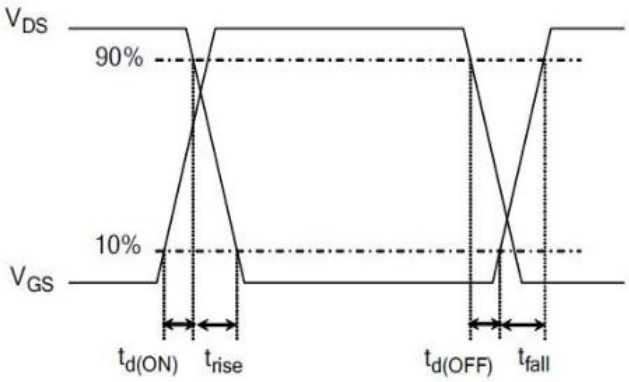
1) Gate Charge Test Circuit



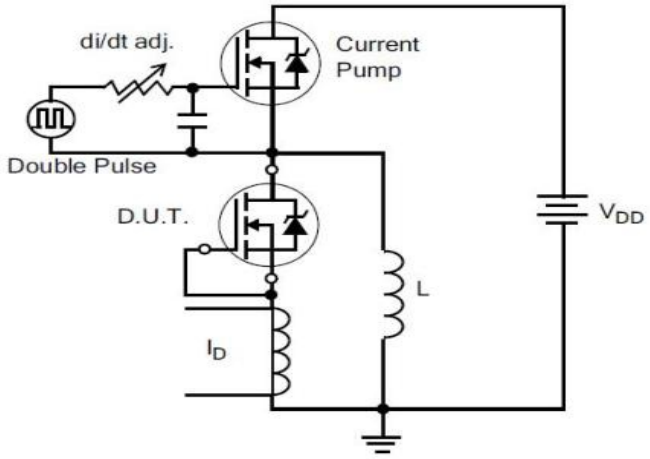
2) . Gate Charge Waveform



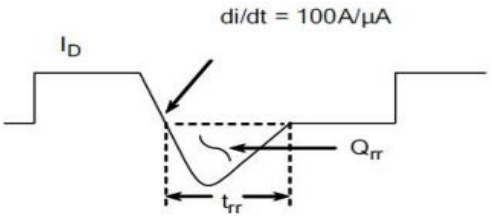
3) Resistive Switching Test Circuit



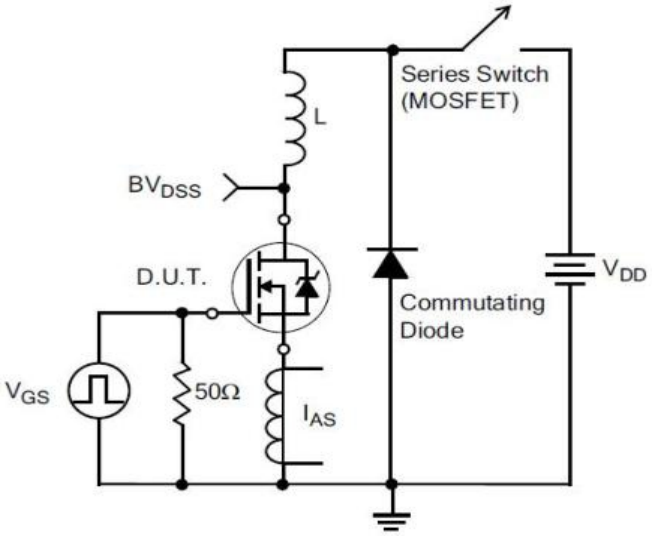
4) Resistive Switching Waveforms



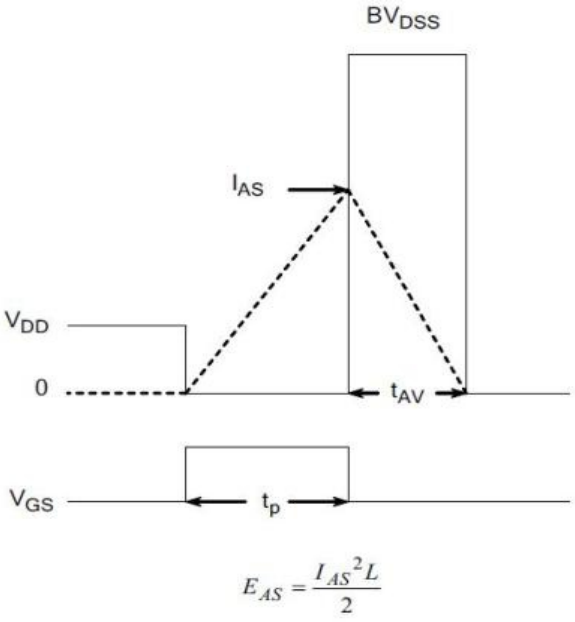
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



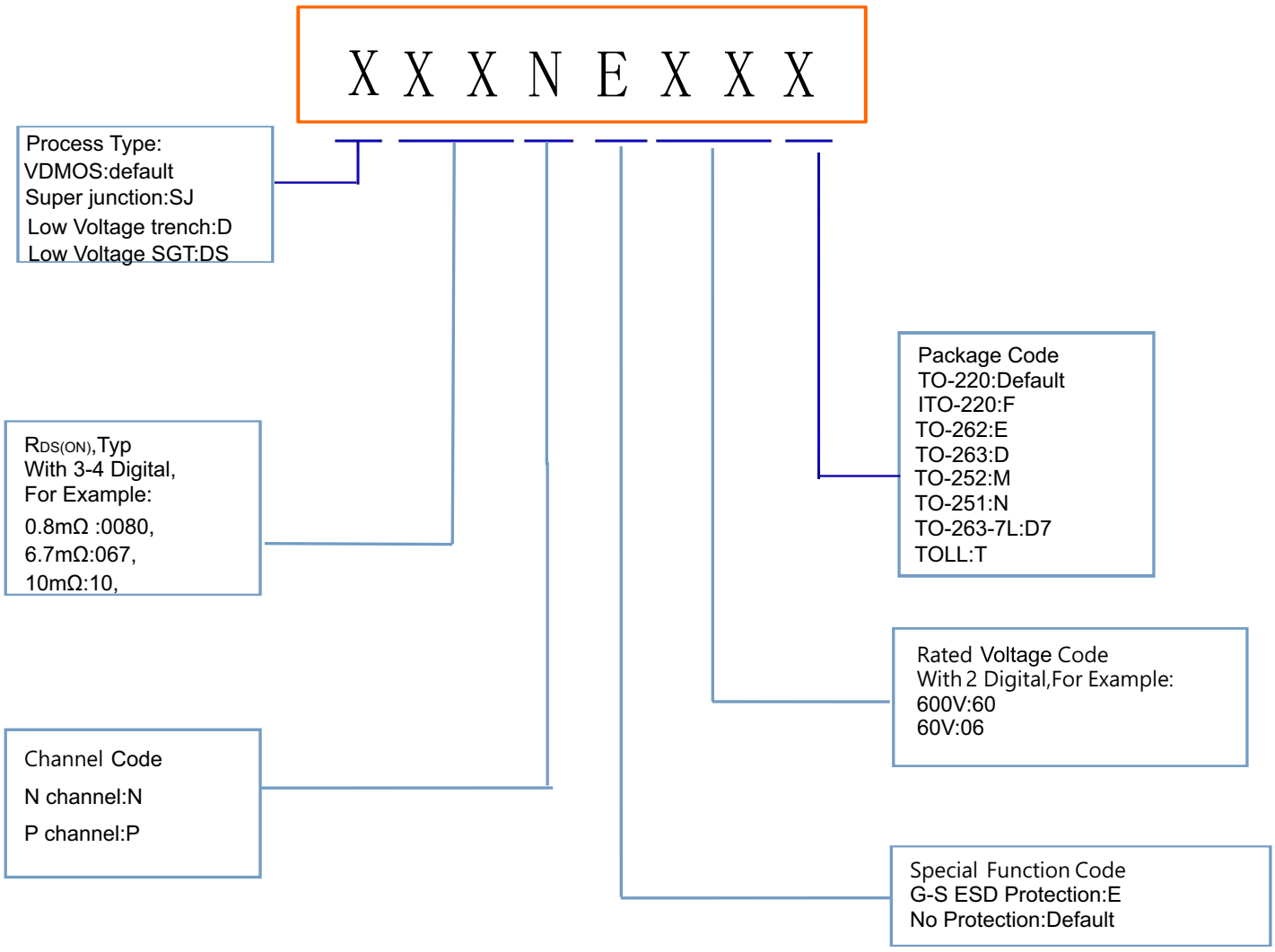
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

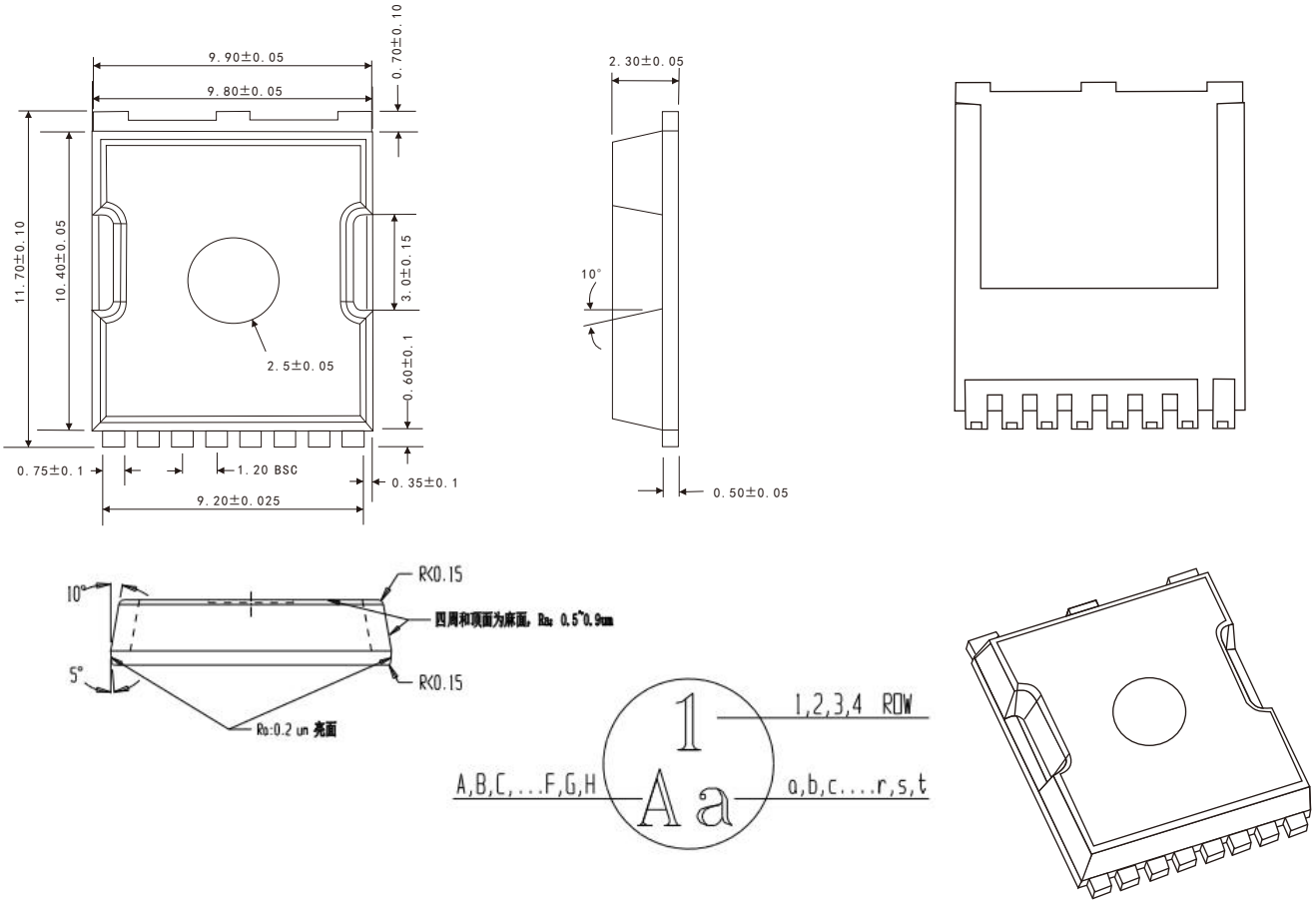
8) Unclamped Inductive Switching Waveforms

Product Names Rules

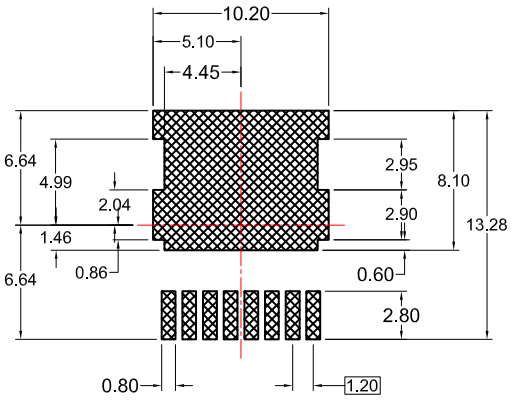


Dimensions

TOLL PACKAGE OUTLINE DIMENSIONS



Suggested Pad Layout



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