SEMICONDUCTOR

4N150P

1500V N-Channel Power MOSFET

Genaral Description

4N150P the silicon N-channel EnhancedVDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

Product Summary			
V_{DS}	$R_{DS(on)}$(Ω)Typ	I_D(A)	Qg(Typ)
1500V	3.5 @ 10V,2A	4.0	43nc

TO-247

4N150P

Features

- Low on-resistance
- Low gate charge and Fast Switching
- 100% avalanche tested
- Rohs compliant

Mechanical Data

- Case:TO-247 Package

Application

- Power switch circuit of adaptor and charger

Ordering Information

Part No.	Marking.	Package Type	Package	Quality(box)
4N150P	4N150P	TO-247	Tube	360

Pin Definition:

1.Gate
2.Drain
3.Source

Block Diagram

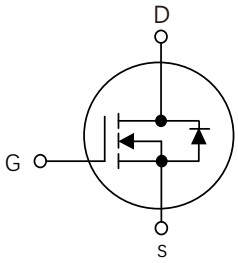


Table1 Absolute Maximum Ratings (TC=25°C, unless otherwise specified)

Parameters		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	1500	V
Gate-Source Voltage		V_{GS}	±30	V
Contionous Drain Current	TC=25°C	I_D	4	A
	TC=100°C		2.5	
Pulsed Drain Current (Note 1)		I_{DM}	16	A
Single Pulse Avalanche Energy(Note 2)		EAS	909	mJ
Reverse Diode Recovery dv/dt(Note 3)		dv/dt	5	V/ns
Power Dissipation TC=25°C		P_D	543	W
Operating Junction and Storage Temperature		TJ/TSTG	-55 ~ +150	℃

Table 2.Thermal Characteristics

Parameters	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	50	℃/W
Thermal resistance Junction to Case	$R_{\theta JC}$	0.23	℃/W

Table 3. Electrical Chatacteristics (T_J=25℃, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	1500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=1500V,V_{GS}=0V			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V			-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	3.0		5.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=2A		3.5	5.0	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz		2250		pF
Output Capacitance		C_{OSS}			132		pF
Reverse Transfer Capacitance		C_{RSS}			10		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=750V,I_D=4A, V_{GS}=10V,R_G=10Ω		126		ns
Turn-On Rise Time		tr			340		ns
Turn-Off Delay Time		td(off)			45		ns
Turn-Off Fall Time		tf			56		ns
Total Gate Charge		Q_G	V_{DS}=750V,I_D=4A, V_{GS}=10V		43		nC
Gate-Source Charge		Q_{GS}			13		nC
Gate-Drain Charge		Q_{GD}			16		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=4A			1.5	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I_S				4	A
Reverse Recovery Time		trr	V_{GS}=0V,I_S=4A dI$_F$/dt=100A/μs(Note 4)		830		ns
Reverse Recovery Charge		Q_{RR}			6.9		μC

Notes: 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=30mH,V_{DD}=150V,V_G=10V,Starting T_J=25°C
3 I_{SD}≤I_D,di/dt≤100A/μS,V_{DD}≤BV_{DSS},starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%
5 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

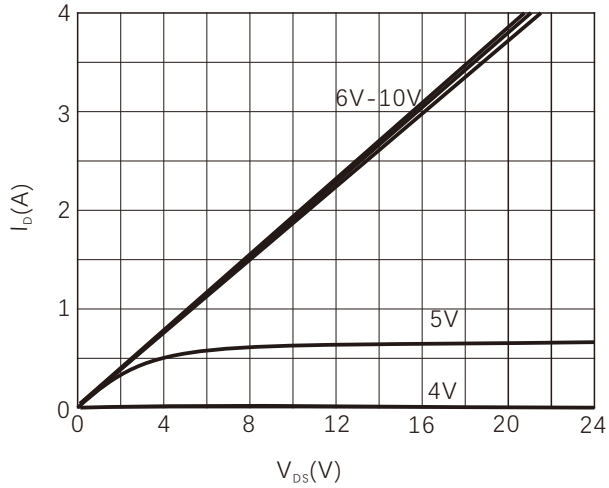


Figure 2.$R_{DS(ON)}$ vs Junction Temperature

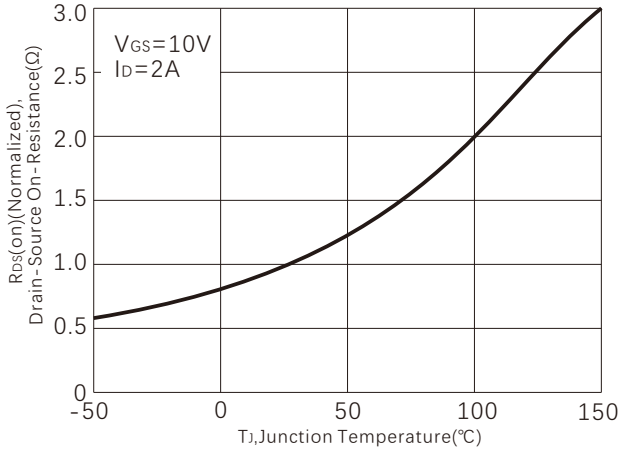


Figure 3.On-Resistance vs.Drain Current

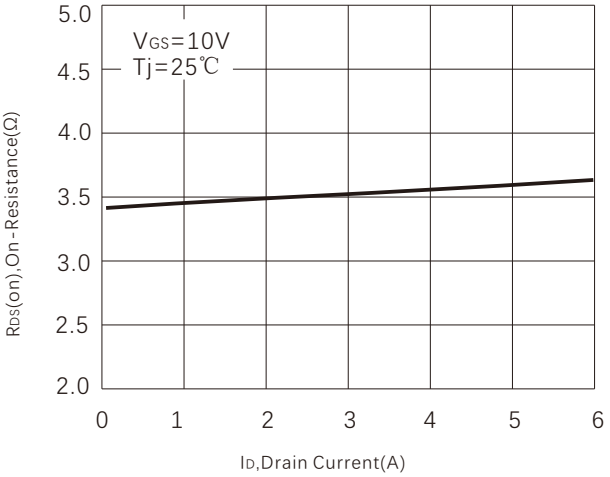


Figure 4. Capacitance

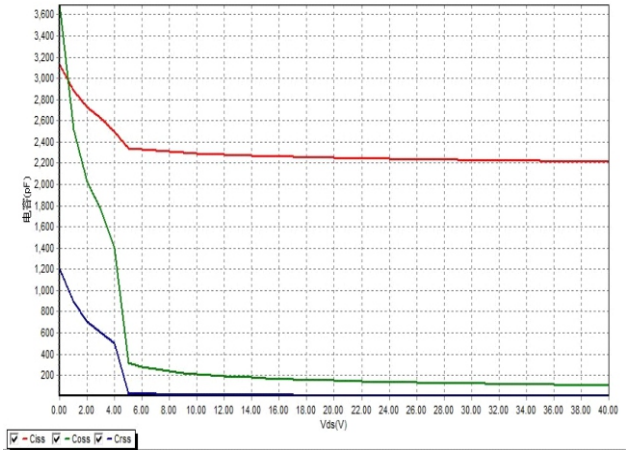


Figure 5.Gate charge

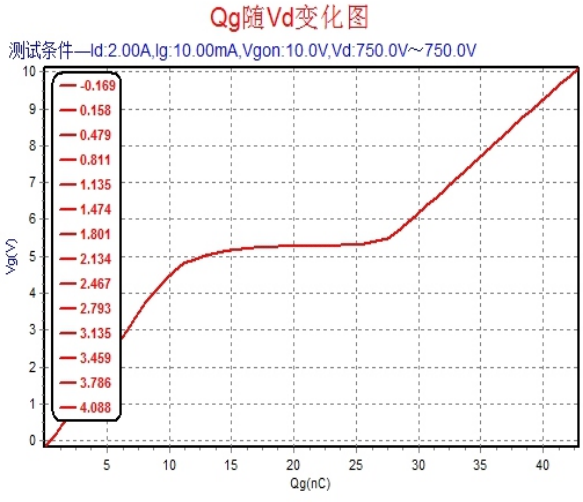


Figure 6. Typical Body Diode Transfer Characteristics

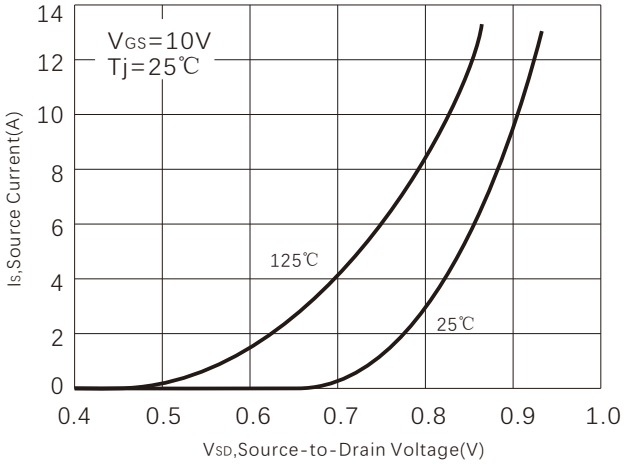


Figure 7.ID Current De-rating

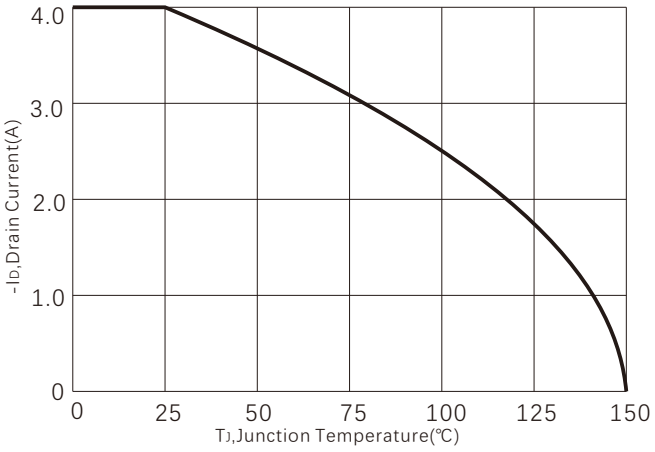


Figure 8.BVDSS vs Junction Temperature

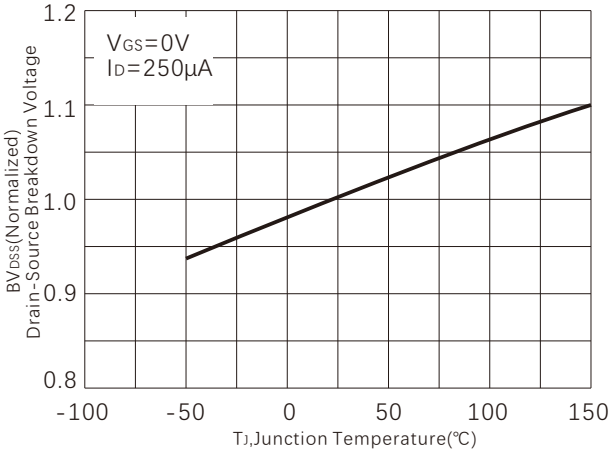


Figure 9.

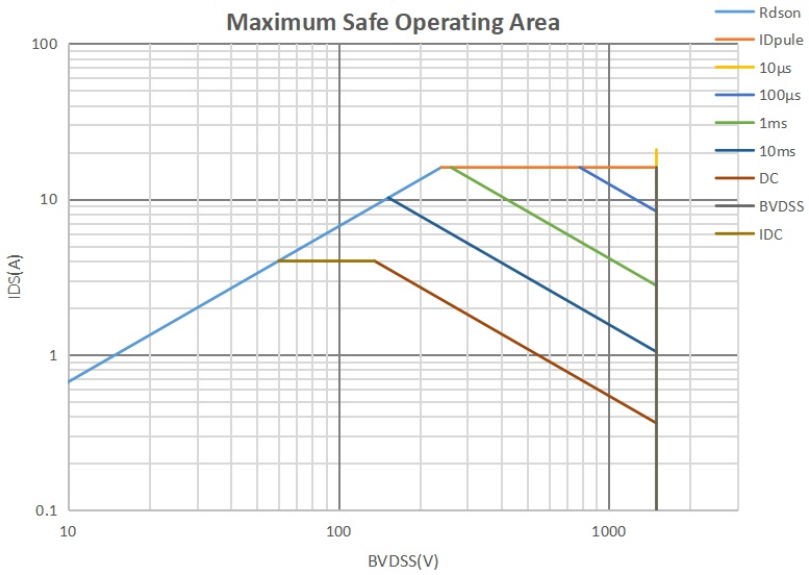
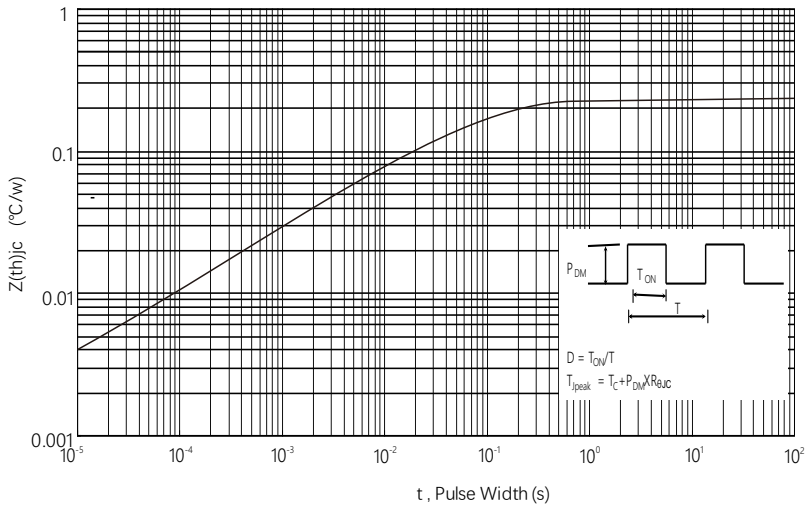
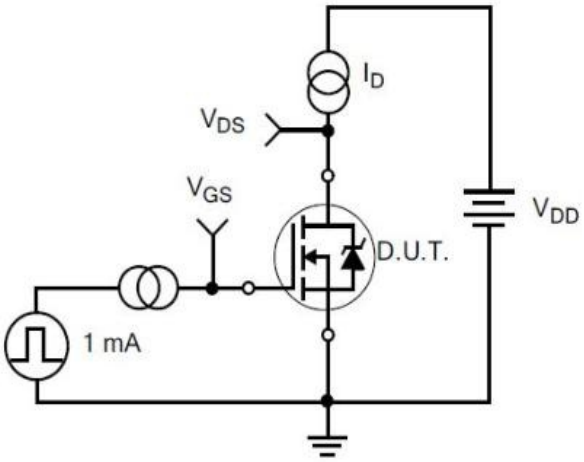


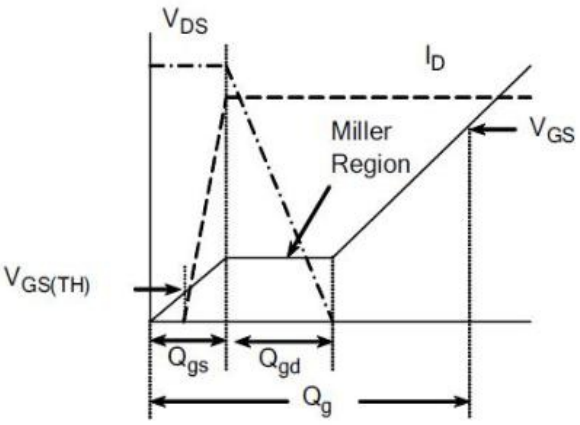
Figure 11. Maximum Transient Thermal Impedance



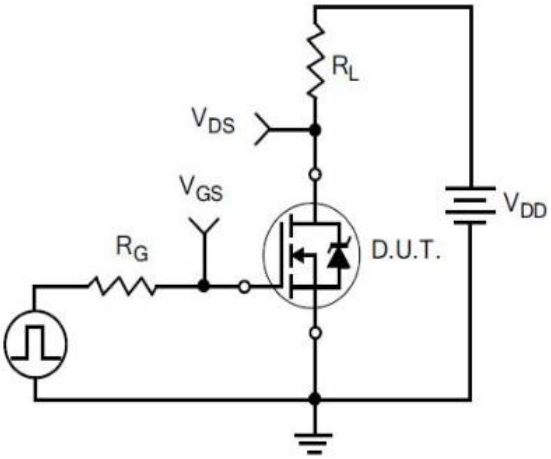
Typical Test Circuit



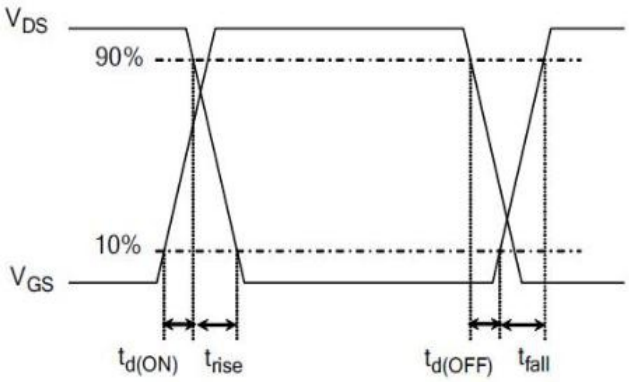
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

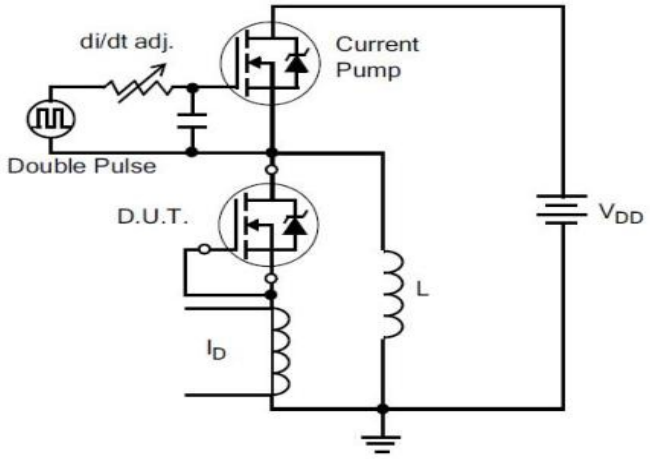


3) Resistive Switching Test Circuit

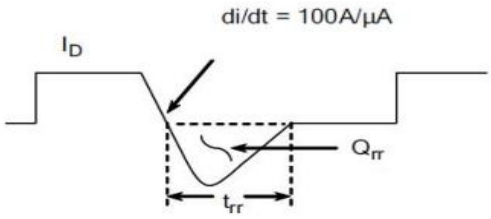


4) Resistive Switching Waveforms

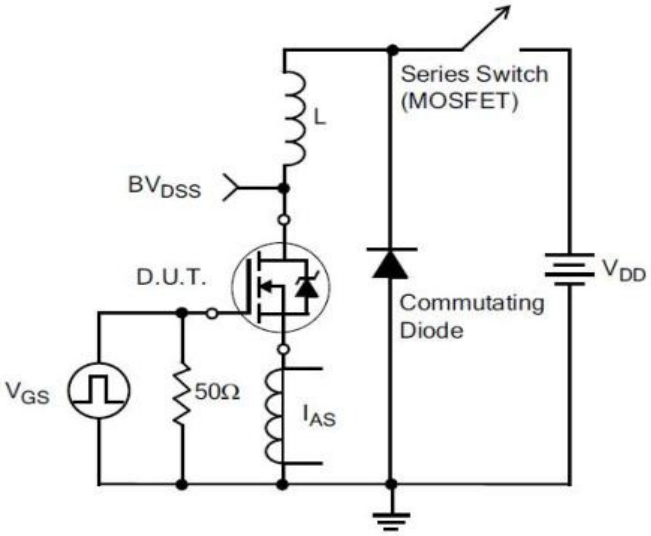
Typical Test Circuit



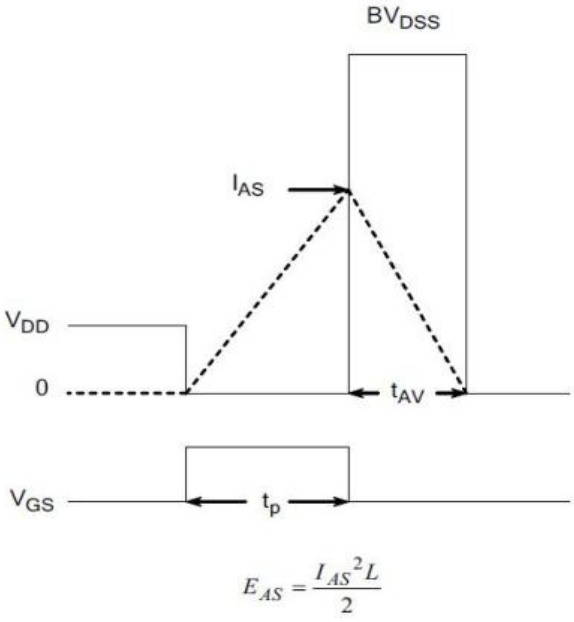
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

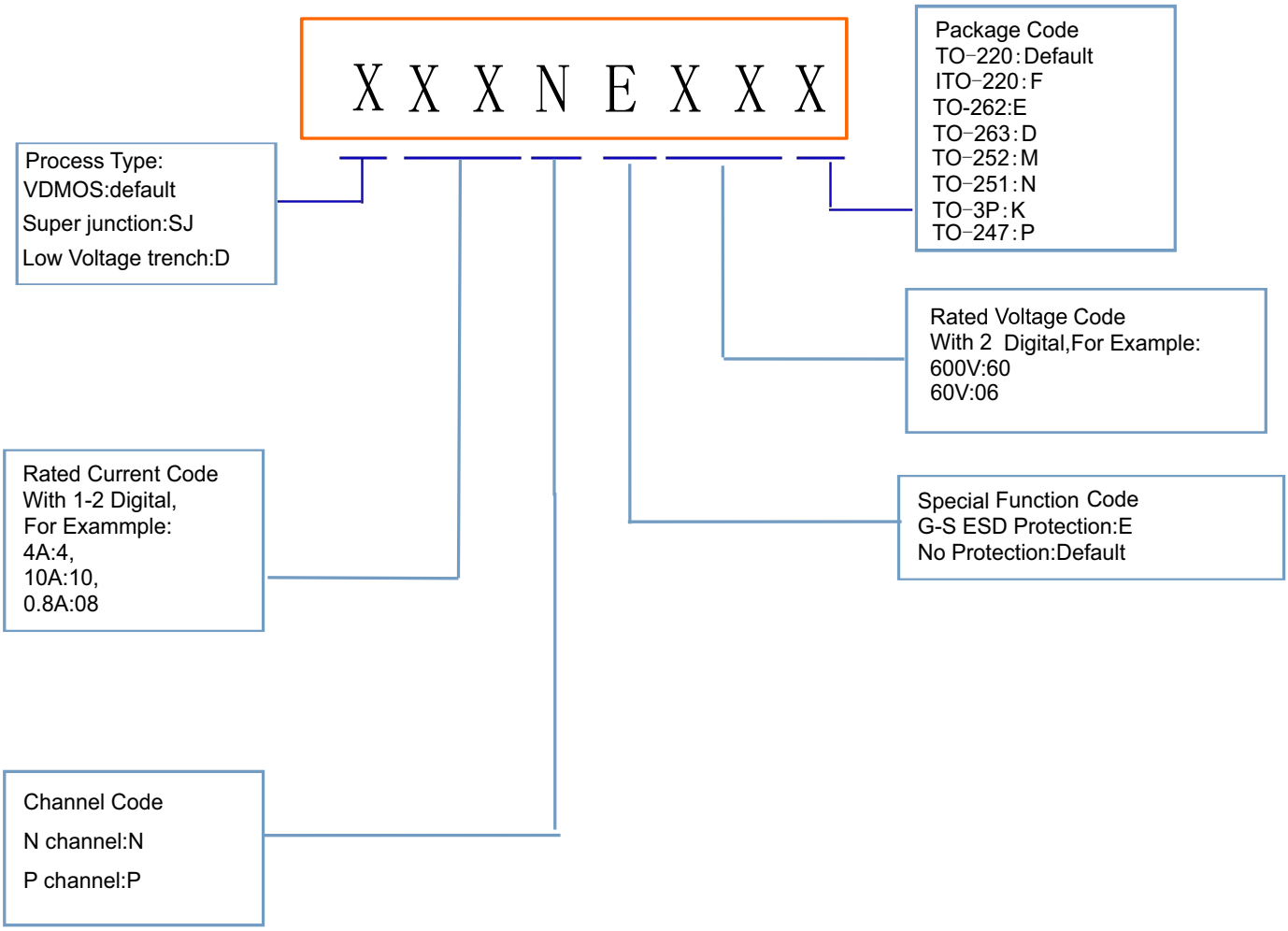


7) . Unclamped Inductive Switching Test Circuit



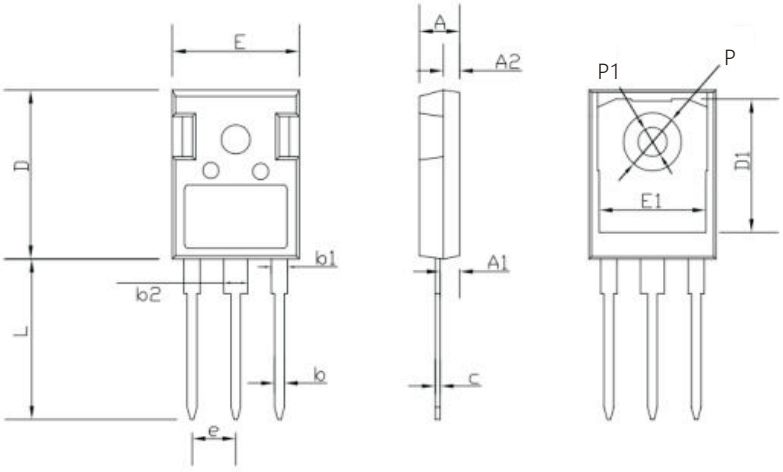
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-247 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.06	0.0772	0.0812
b2	2.96	3.06	0.117	0.121
c	0.59	0.66	0.0232	0.0260
D	20.90	21.10	0.8235	0.8313
D1	16.25	16.85	0.6403	0.6639
E	15.70	15.90	0.6186	0.6265
E1	13.10	13.50	0.5161	0.5319
e	5.44		0.2143	
L	19.80	20.10	0.7801	0.7919
ΦP	3.50	3.70	0.1379	0.1458
ΦP1	0	7.30	0	0.2876

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