SEMICONDUCTOR

DS038N08G3

100A 80V N-Channel Enhancement Mode Power MOSFET

Features

- Uses advanced SGT technology
- Extremely low on-resistance RDS(on)
- Excellent gate charge x RDS(on) product(FOM)

Product Summary			
V_{DS}	$R_{DS(on)}$ (mΩ) Typ	I_D (A)	Qg (Typ)
80V	3.8 @ 10V 50A	100	64nc

Mechanical Data

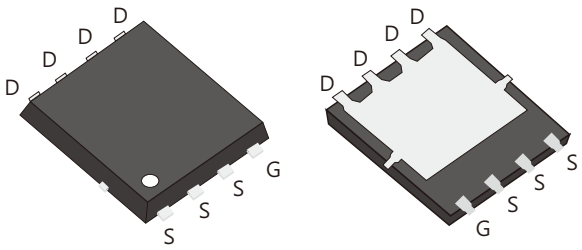
- Case:DFN5×6 Package

DFN5×6

DS038N08G3

Application

- Switching Application
- SR (Synchronous rectification)
- DC/DC converter
- General purpose applications



Ordering Information

Part No.	Package Type	Package	Quality(box)
DS038N08G3	DFN5×6	Tape & Reel	5000

Block Diagram

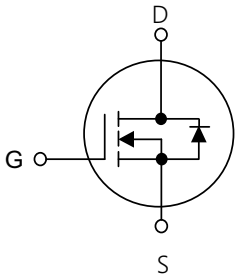


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 5)	T_C=25°C(Package limit)	I_D	100	A
	T_C=25°C(Silicon limit)		150	
	T_C=100°C(Silicon limit)		95	
Pulsed Drain Current (Note 1)		I_{DM}	400	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	812	mJ
Power Dissipation T_C=25°C		P_D	139	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient,,Max	$R_{\theta JA}$	62	°C/W
Thermal resistance Junction to Case,Max	$R_{\theta JC}$	0.9	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	80	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=80V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=50A	-	3.8	4.6	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=40V,V_{GS}=0V,f=1MHz	-	5154	-	pF
Output Capacitance		C_{OSS}		-	783	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	49	-	pF
Gate Resisitance		R_G	f=1MHz	-	1.5	-	Ω
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DS}=42.5V,R_L=3.5Ω V_{GS}=10V	-	26	-	ns
Turn-On Rise Time		t_R		-	47	-	ns
Turn-Off Delay Time		td(off)		-	54	-	ns
Turn-Off Fall Time		tf		-	28	-	ns
Total Gate Charge		Q_G	V_{DS}=40V,I_D=50A, V_{GS}=10V	-	64	-	nC
Gate-Source Charge		Q_{GS}		-	19.9	-	nC
Gate-Drain Charge		Q_{GD}		-	17	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=50A	-	-	1.2	V
Reverse Recovery Time		trr	V_{GS}=0V, I_F=20A dI$_F$/dt=500A/μs	-	66	-	ns
Reverse Recovery Charge		Q_{RR}		-	79	-	nC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=0.5mH, R_G=25Ω,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
4 Guaranteed by design,not subject to production
5 The maximum current is limited by the package.

Typical Characteristics Diagrams

Figure 1.Output Characteristics

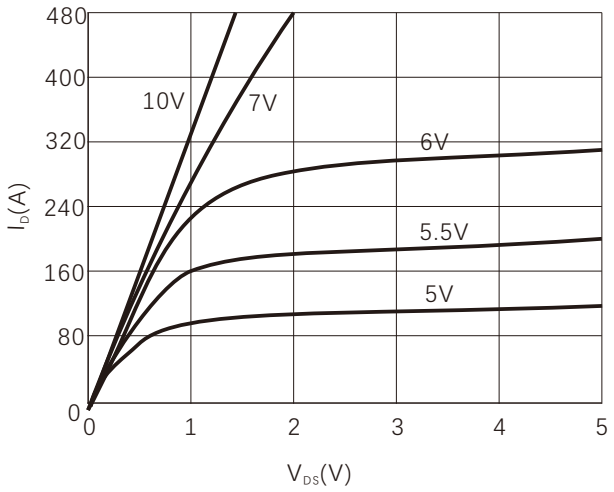


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

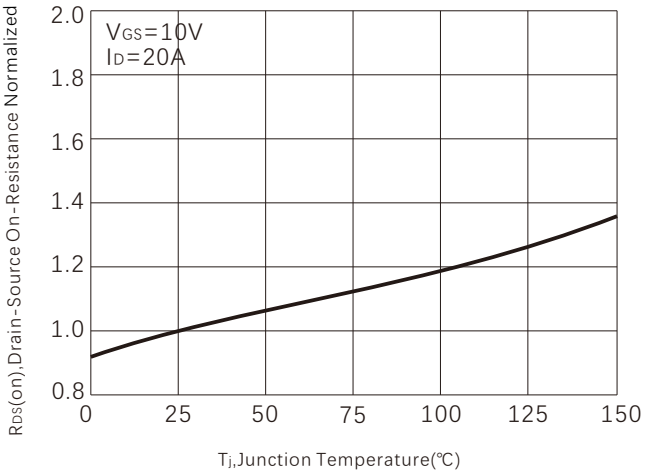


Figure 3.On-Resistance vs.Drain Current

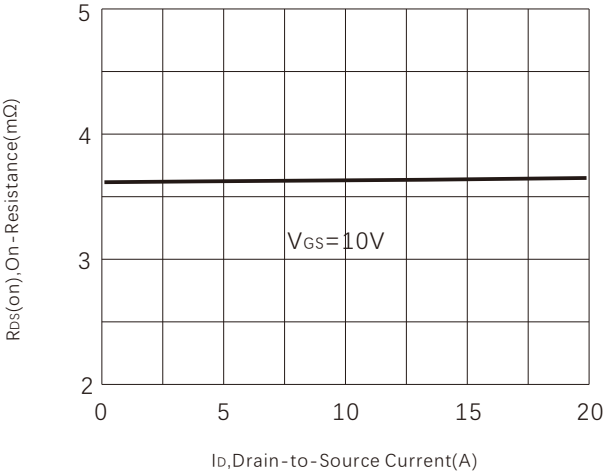


Figure 4. Capacitance

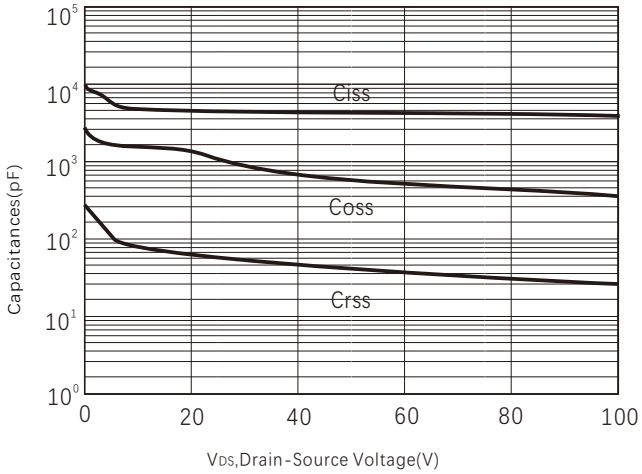


Figure 5.$V_{GS(TH)}$ Vs Tj Temperature

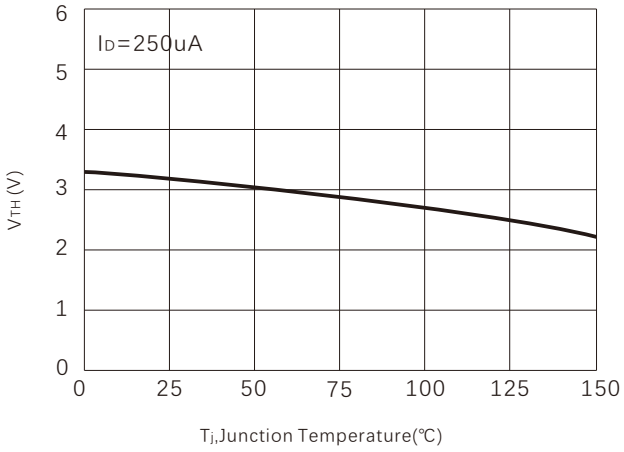


Figure 6.Source-Drain Diode Forward Voltage

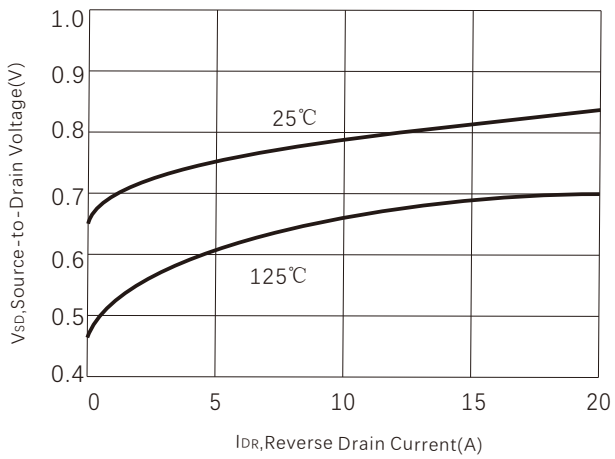


Figure 8. Power dissipation

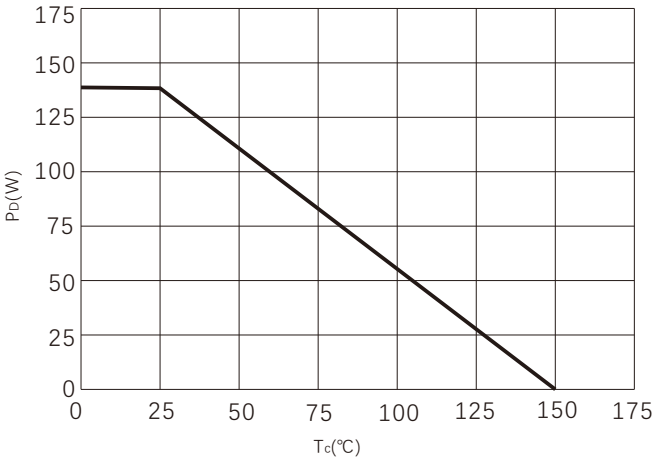


Figure 9. Transfer Characteristics

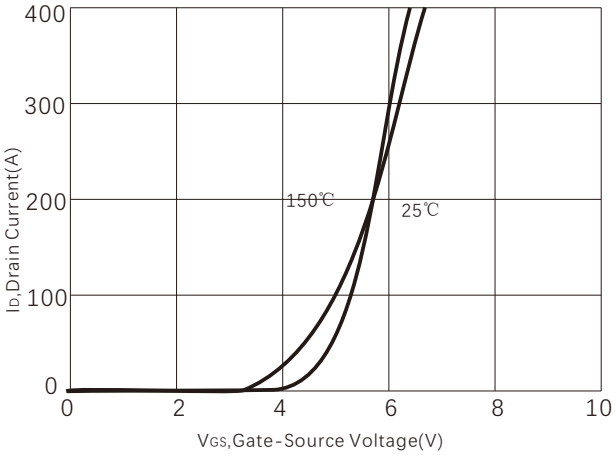


Figure 9. Safe operating area

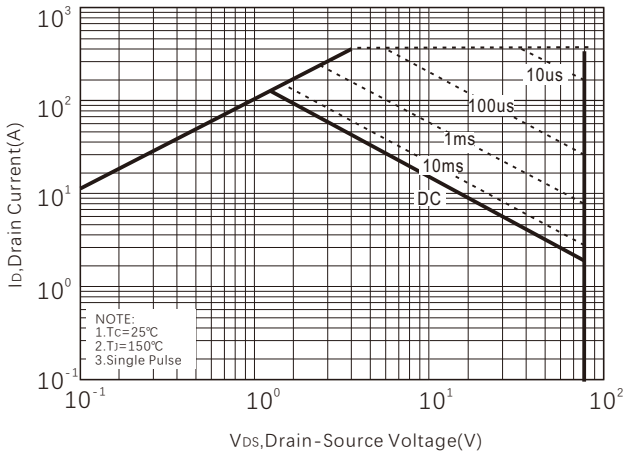
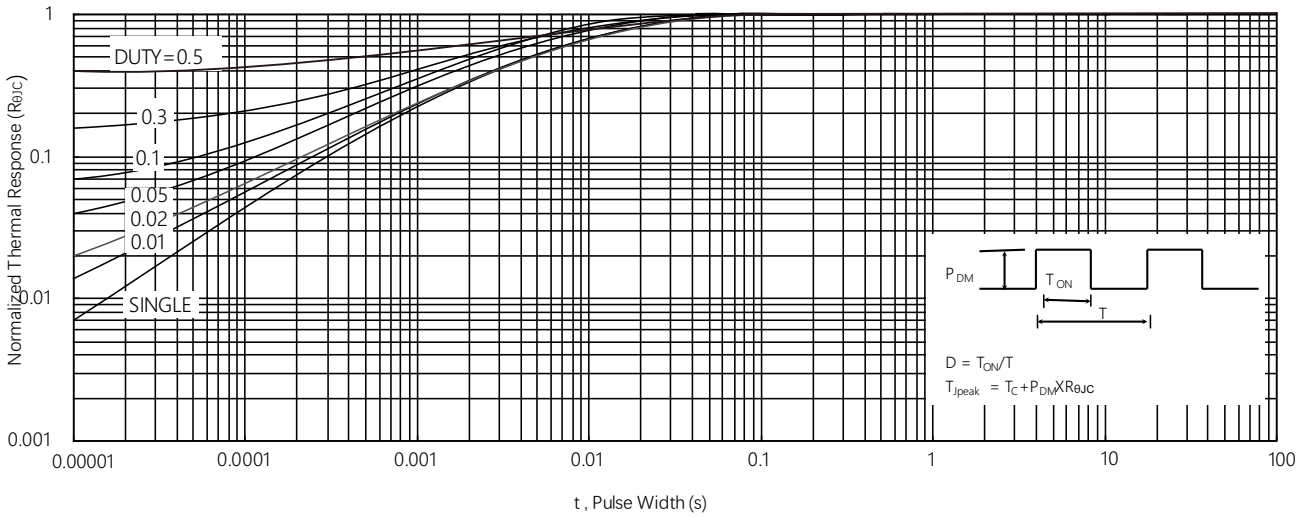
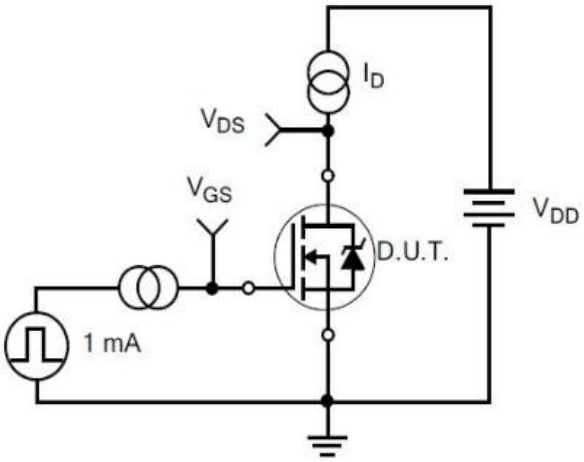


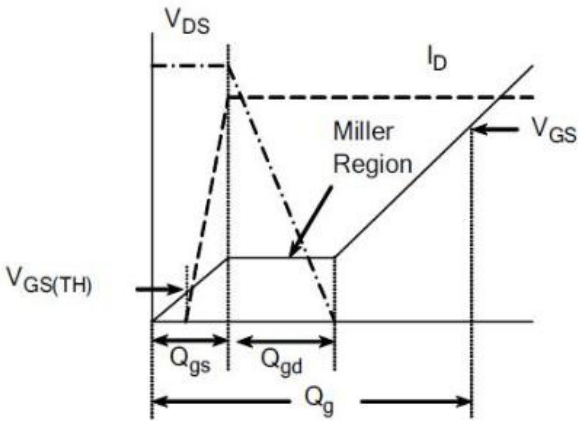
Figure 10.Normalized Maximum Transient Thermal Impedance



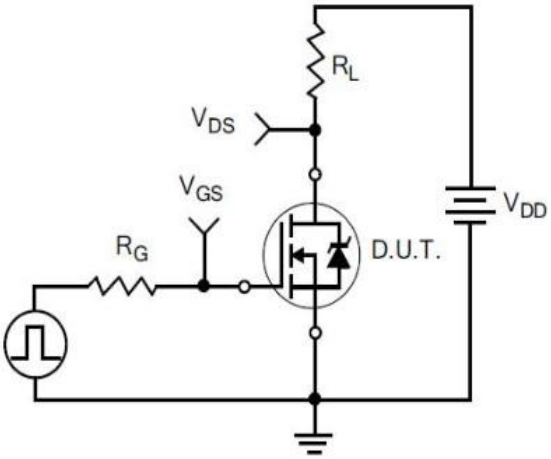
Typical Test Circuit



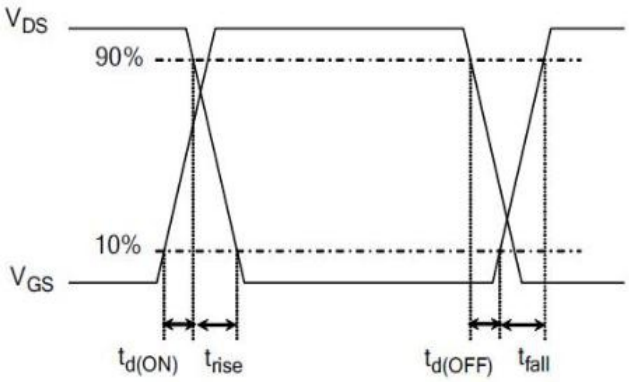
1) Gate Charge Test Circuit



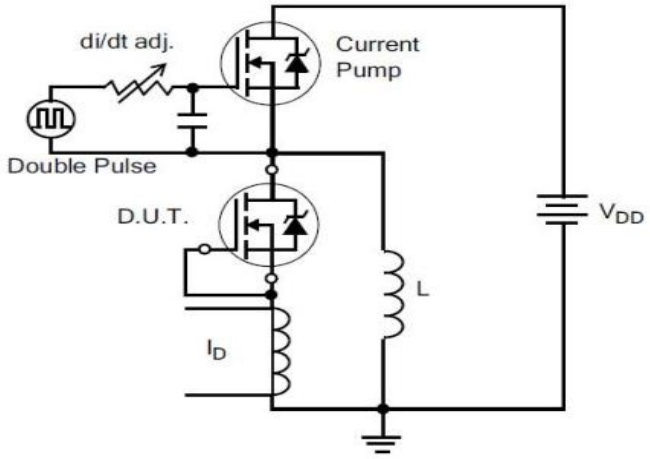
2) . Gate Charge Waveform



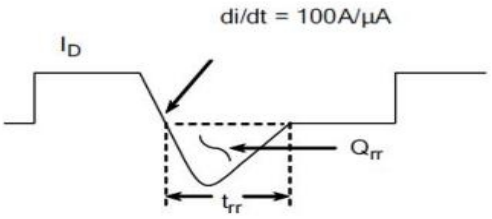
3) Resistive Switching Test Circuit



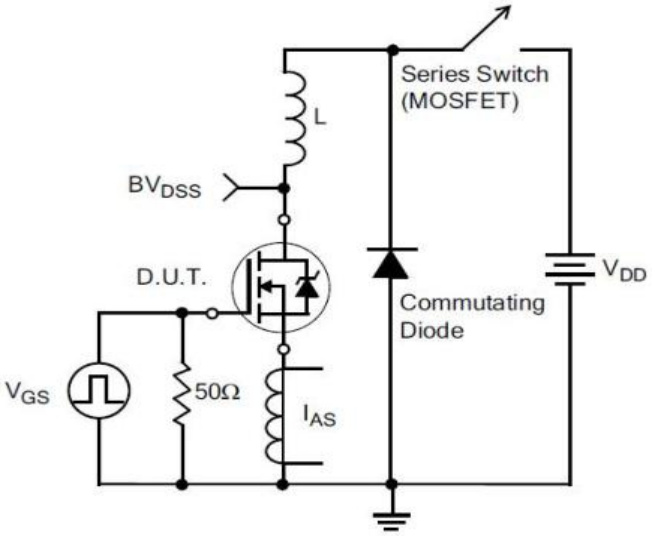
4) Resistive Switching Waveforms



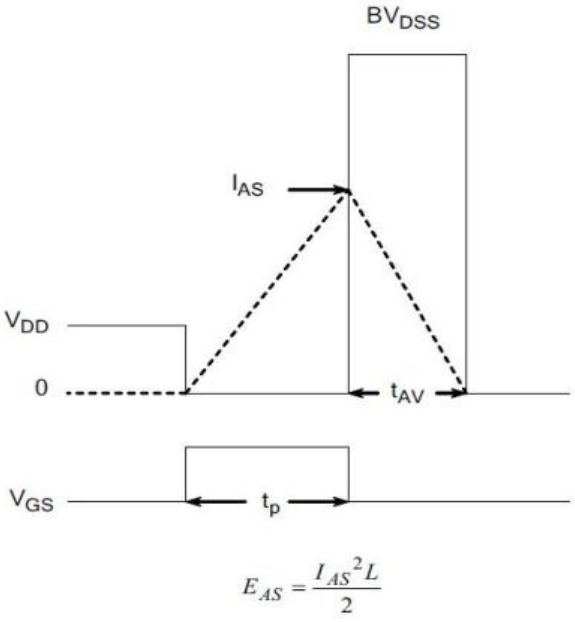
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



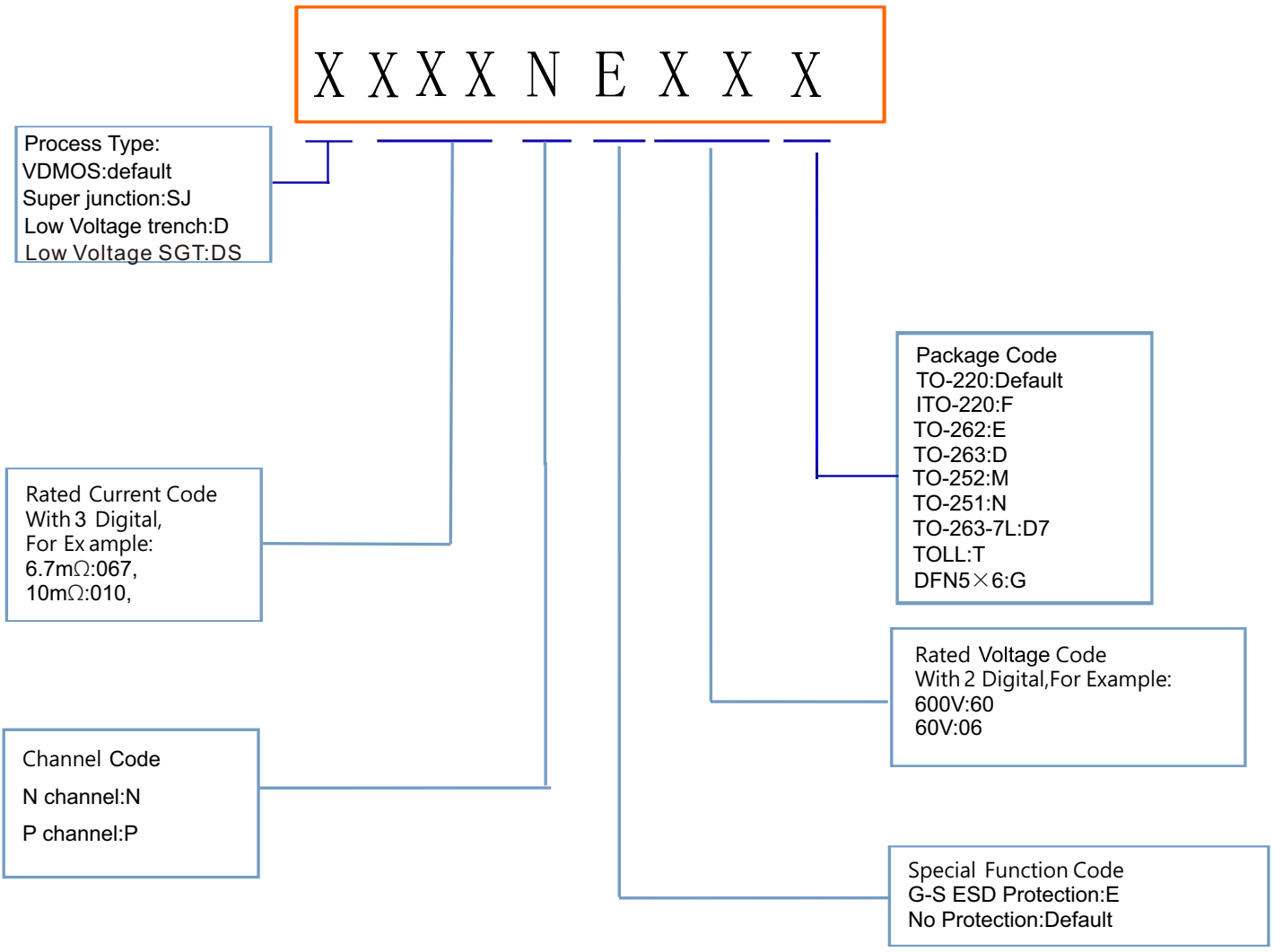
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

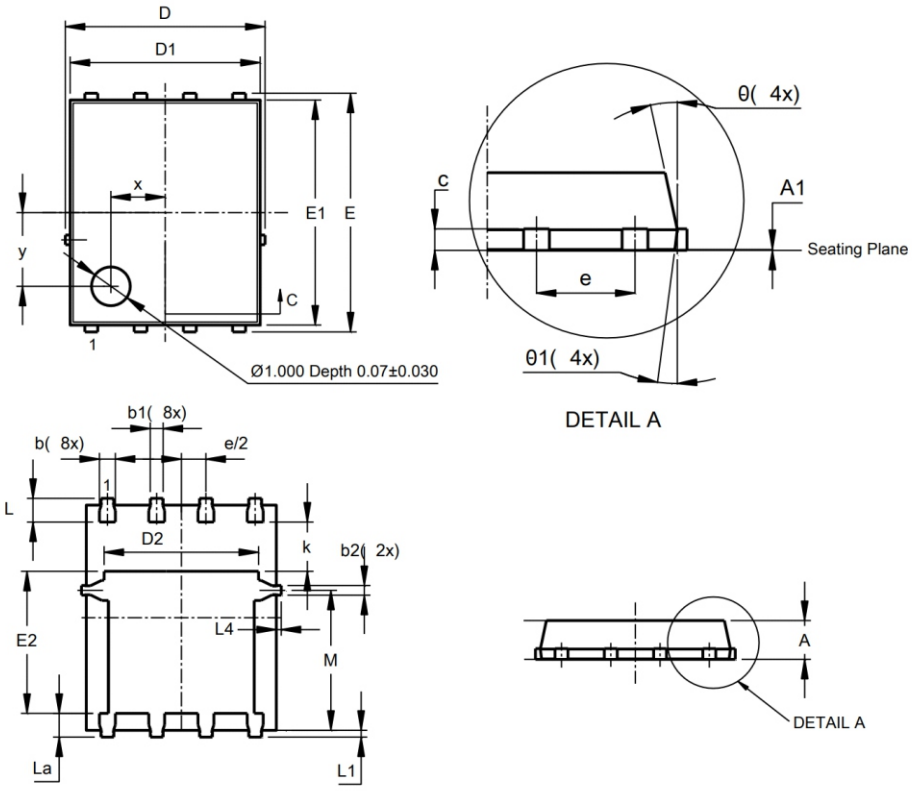
8) Unclamped Inductive Switching Waveforms

Product Names Rules



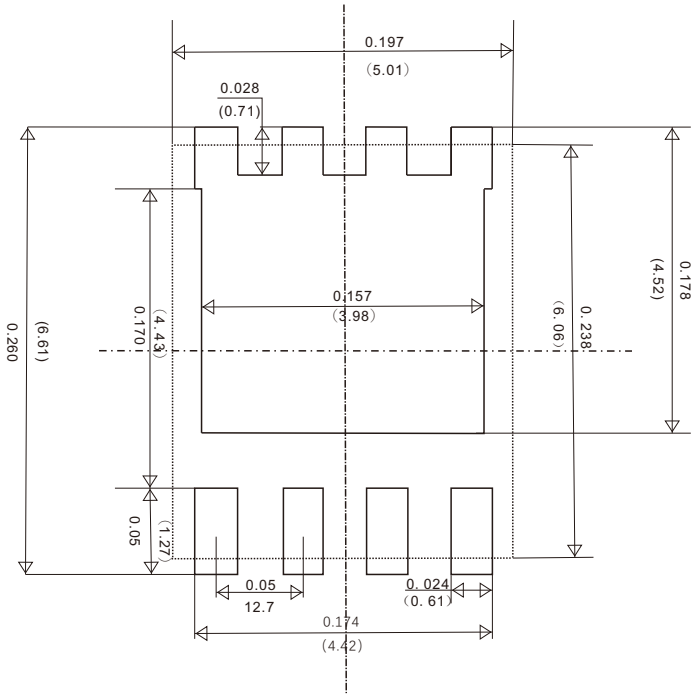
Dimensions

DFN5×6 PACKAGE OUTLINE DIMENSIONS



Dim	Min	Max	Type
A	0.90	1.10	1.00
b	0.23	0.41	0.32
b1	0.24	0.30	0.27
b2	0.16	0.32	0.23
c	0.17	0.27	0.22
D	-	-	5.01
D1	4.80	4.95	4.88
D2	-	-	3.98
E	-	-	6.06
E1	5.72	5.82	5.77
E2	3.42	3.52	3.47
k	-	-	1.33
L	0.56	0.66	0.61
La	0.57	0.67	0.63
L1	0.06	0.15	0.11
L4	-	-	0.06
M	3.00	3.20	3.08
Φ	10	11	10.39

Suggested Pad Layout



Friendship Reminder

■ JiNan JingHeng（hereinafter referred to as JH） reserves the right to make changes to this document and its products and specifications at anytime without notice.

■ Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

■ JH makes no warranty, representation or guarantee regarding the suitability ofi ts products for any particular purpose, nor does JH assume any liability for application assistance or customer product design.

■ JH does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

■ No license is granted by implication or otherwise under any intellectual property rights of JH.

■ JH's products are not authorized for use as critical components in life support devices or systems without express written approval of JH.