

### Features

- Advanced high cell density Trench technology
- Low Gate Charge for fast switching
- Low RDS(ON)to minimize Conductive loss

Product Summary			
V <sub>DS</sub>	R <sub>DS(on)</sub> (mΩ) Typ	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)
100V	1.25 @ 10V 50A	400	157nc

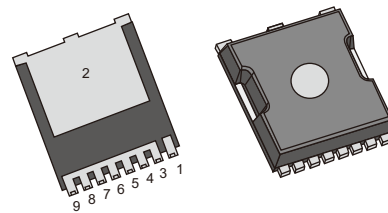
### Mechanical Data

- Case:TOLL Package

TOLL  
D017N10T

### Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications



### Ordering Information

Part No.	Package Type	Package	Quality(box)
D017N10T	TOLL	Tape & Reel	2000

### Block Diagram

Pin Definition:  
1. Gate  
2. Drain  
3/4/5/6/7/8/9. Source

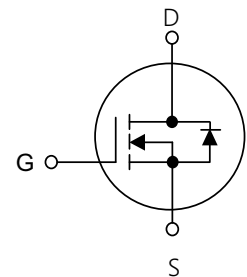


Table1 Absolute Maximum Ratings (T<sub>c</sub>=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	T <sub>c</sub> =25°C	400
		T <sub>c</sub> =100°C	282
Pulsed Drain Current (Note 1)	I <sub>DM</sub>	1200	A
Single Pulse Avalanche Energy(Note 2)	E <sub>AS</sub>	2800	mJ
Power Dissipation T <sub>c</sub> =25°C	P <sub>D</sub>	600	W
Operating Junction and Storage Temperature	T <sub>J</sub> /T <sub>STG</sub>	-55~+175	°C

Table 2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	40	$^{\circ}\text{C}/\text{W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	0.25	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	100	-	-	V	
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	1	$\mu\text{A}$	
Gate- Source Leakage Current	Forward	$I_{GSS}$	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Reverse	$I_{GSS}$	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.0	-	4.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$	-	1.25	1.7	m $\Omega$	
		$V_{GS}=6V, I_D=50A$	-	2.2	4.0		
Dynamic Characteristics(Note 4)							
Input Capacitance	$C_{ISS}$	$V_{DS}=50V, V_{GS}=0V, f=1\text{MHz}$	-	11074	-	pF	
Output Capacitance	$C_{OSS}$		-	1736	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	176	-	pF	
Switching Characteristics (Note 4)							
Turn-On Delay Time	$t_d(\text{on})$	$V_{DS}=50V, I_D=50A$	-	40	-	ns	
Turn-On Rise Time	$t_r$		-	122	-	ns	
Turn-Off Delay Time	$t_d(\text{off})$	$V_{GS}=10V, R_G=4.5\Omega,$	-	144	-	ns	
Turn-Off Fall Time	$t_f$		-	127	-	ns	
Total Gate Charge	$Q_G$	$V_{DD}=50V, I_D=50A,$ $V_{GS}=10V$	-	157	-	nC	
Gate-Source Charge	$Q_{GS}$		-	70	-	nC	
Gate-Drain Charge	$Q_{GD}$		-	62	-	nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=50A$	-	-	1.3	V	
Reverse Recovery Time	$t_{rr}$	$V_{GS}=0V, I_F=50A$ $di_F/dt=100A/\mu\text{s}$	-	120	-	ns	
Reverse Recovery Charge	$Q_{RR}$		-	347	-	nC	

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature

2 L = 0.5mH,  $V_{DD} = 20V,$  Starting  $T_J=25^{\circ}\text{C}$ 

3 Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ 

4 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

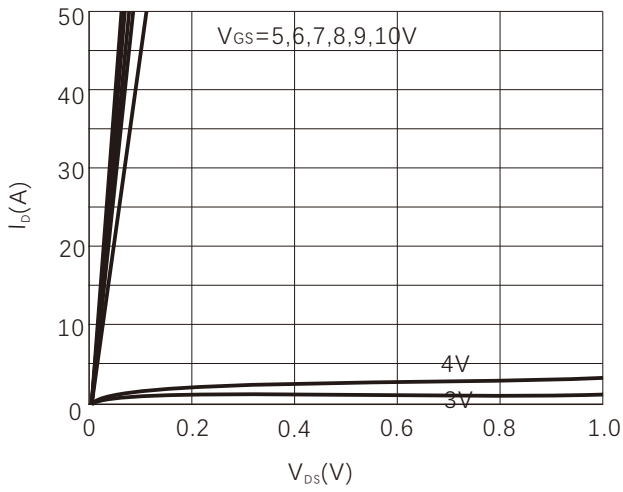


Figure 2. Normalized  $R_{DS(ON)}$  vs Temperature

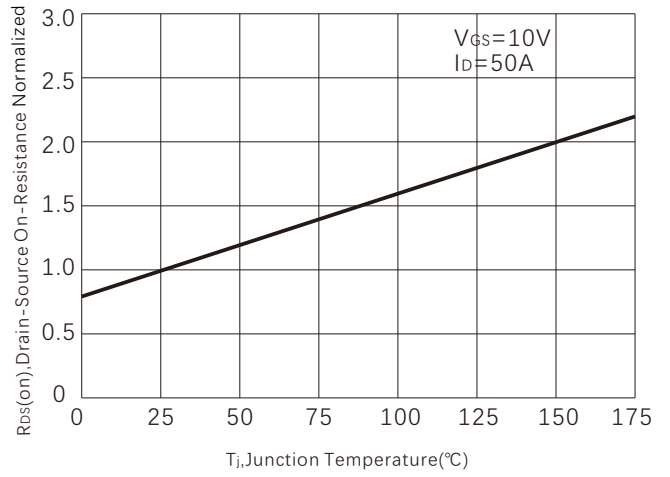


Figure 3. On-Resistance vs. Drain Current

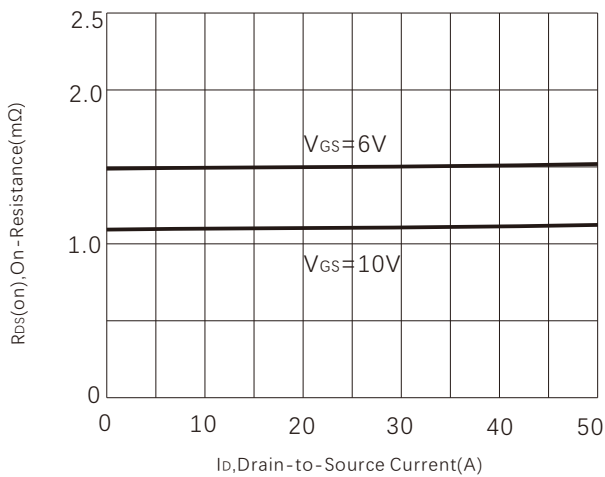


Figure 4. Capacitance

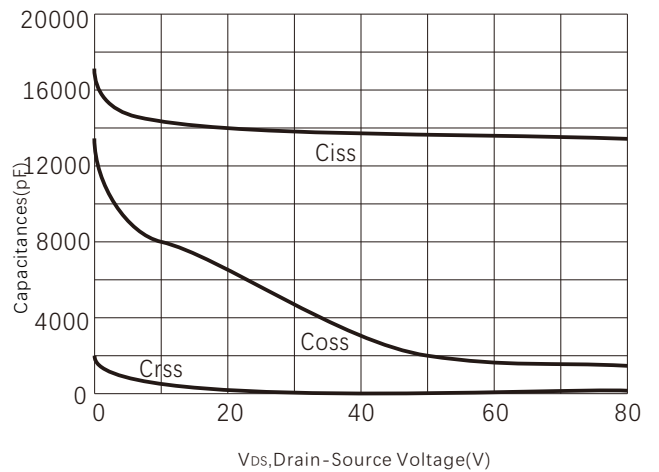


Figure 5. Gate charge

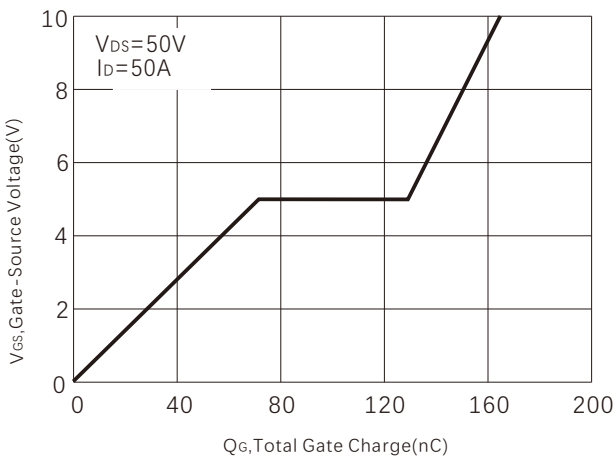


Figure 6. Source-Drain Diode Forward Voltage

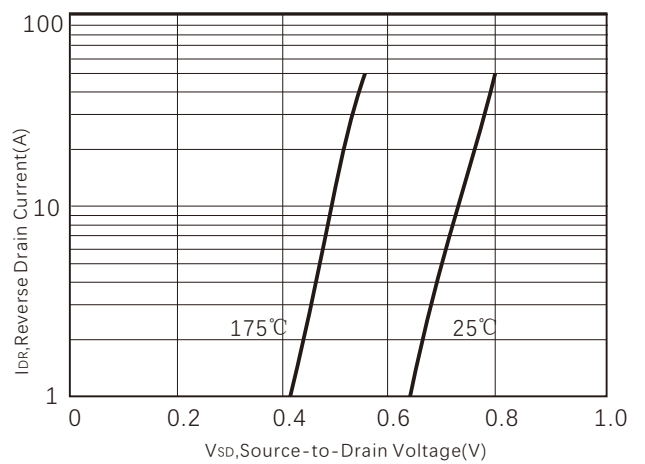


Figure 7. Maximum Drain Current vs Temperature

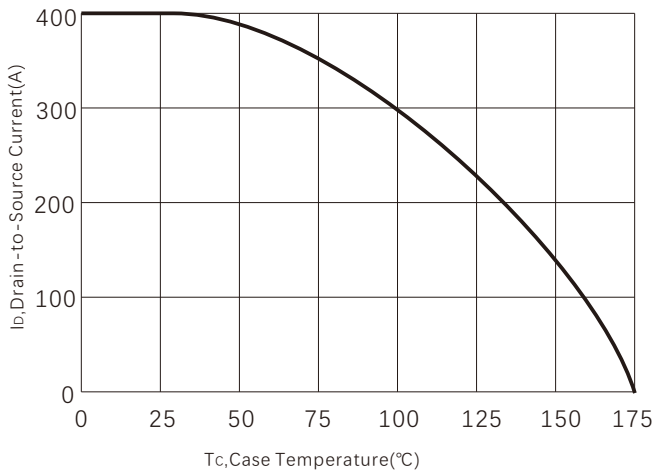


Figure 8. Power dissipation

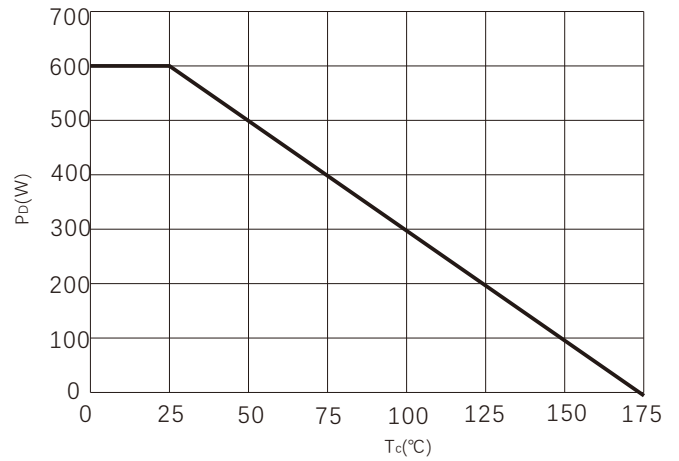


Figure 9. Safe operating area

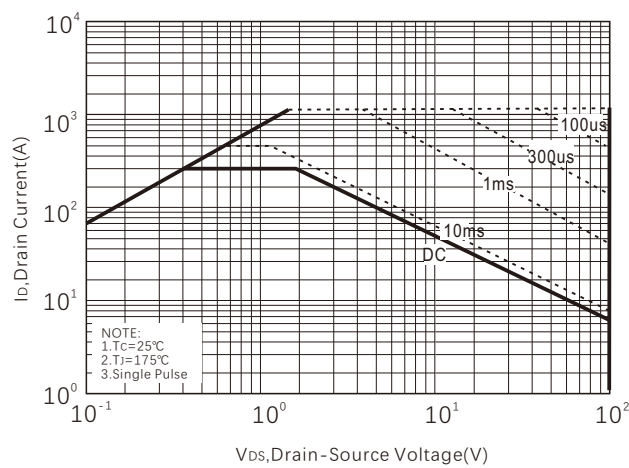
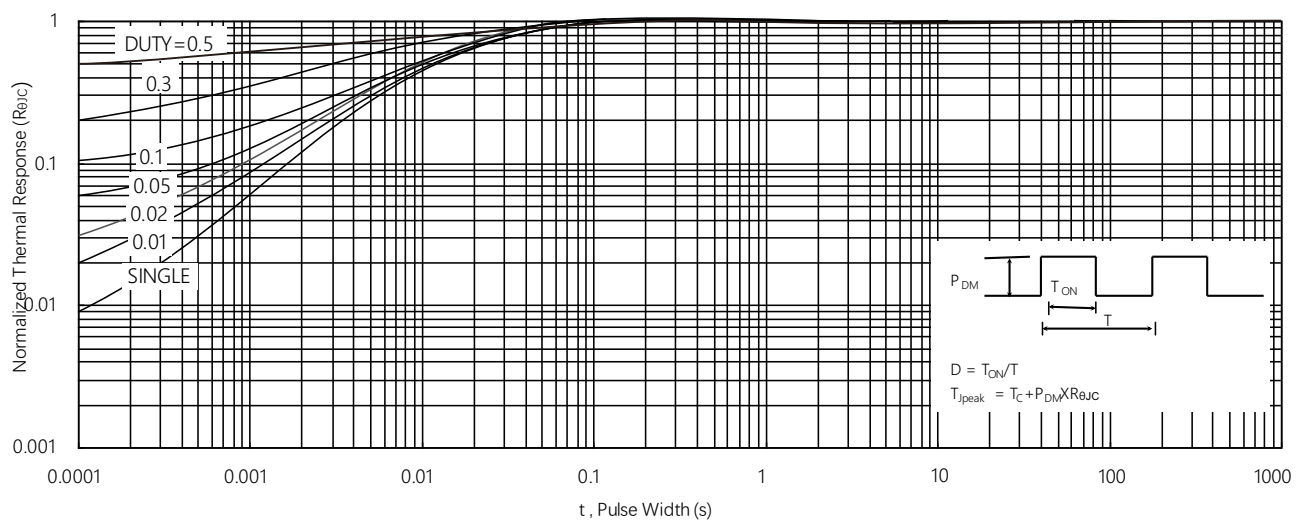
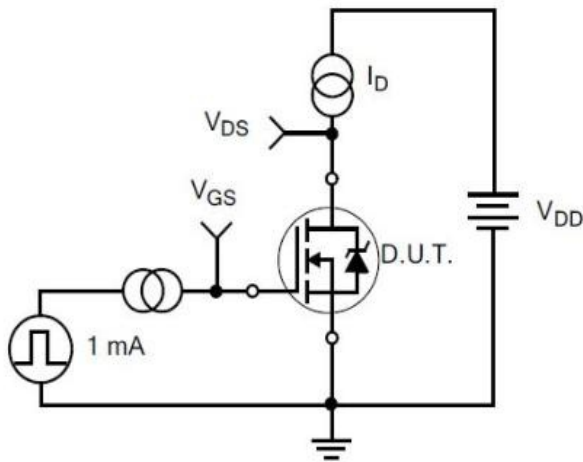


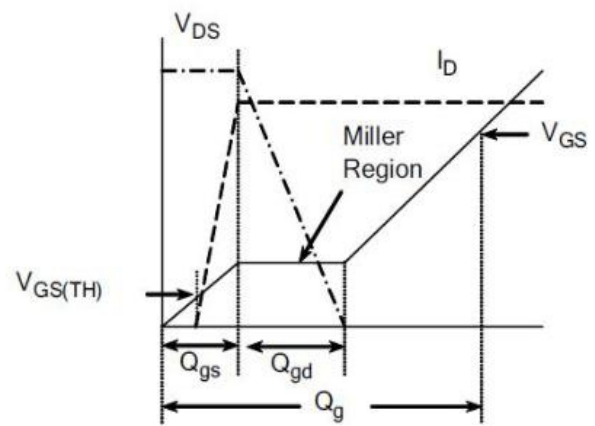
Figure 10. Normalized Maximum Transient Thermal Impedance



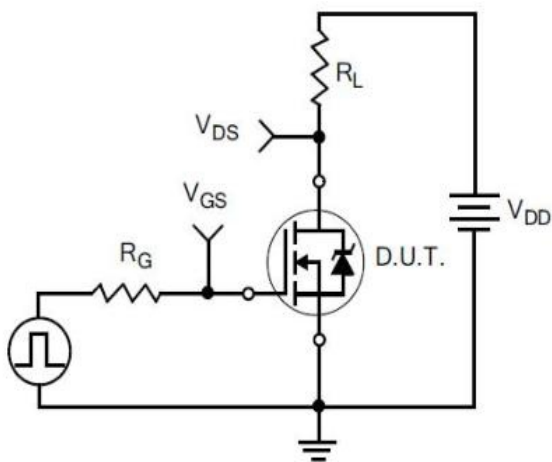
Typical Test Circuit



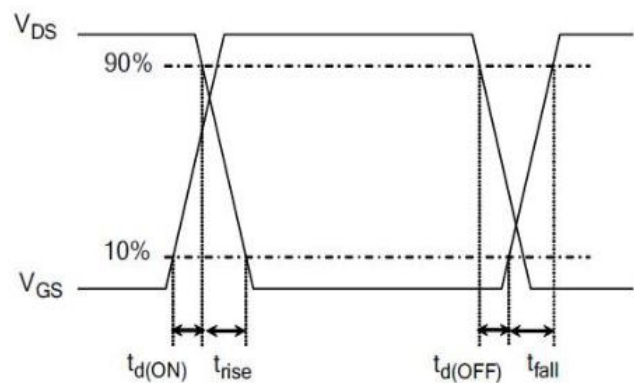
1) Gate Charge Test Circuit



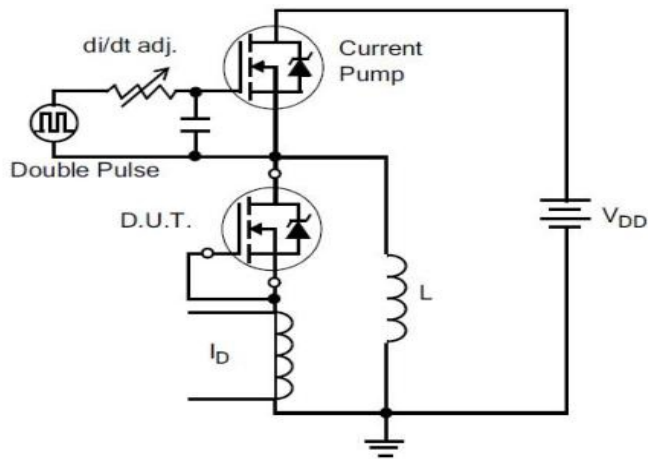
2) Gate Charge Waveform



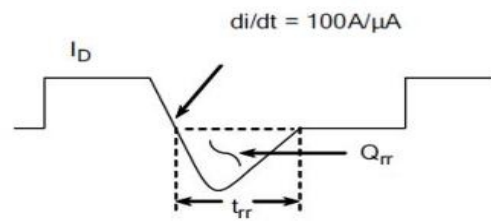
3) Resistive Switching Test Circuit



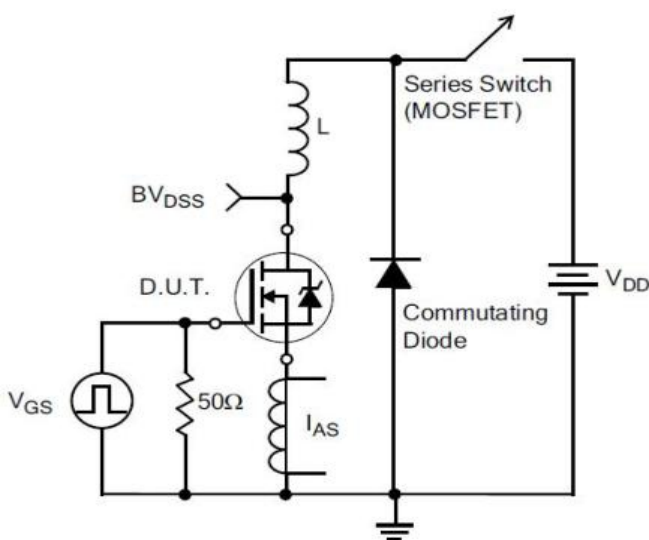
4) Resistive Switching Waveforms



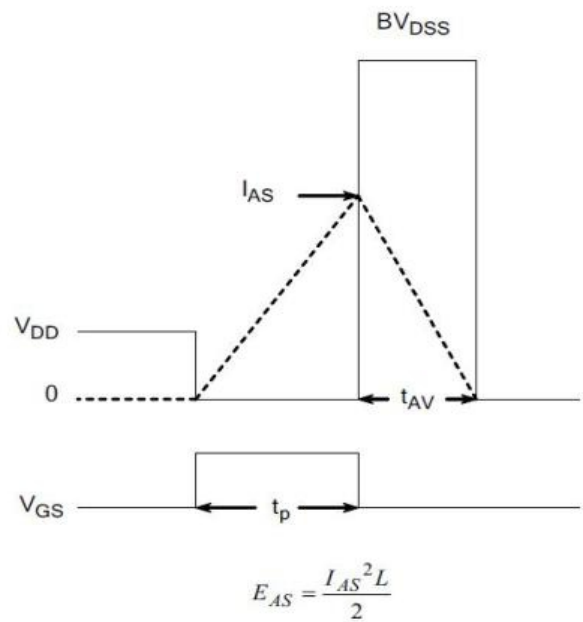
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



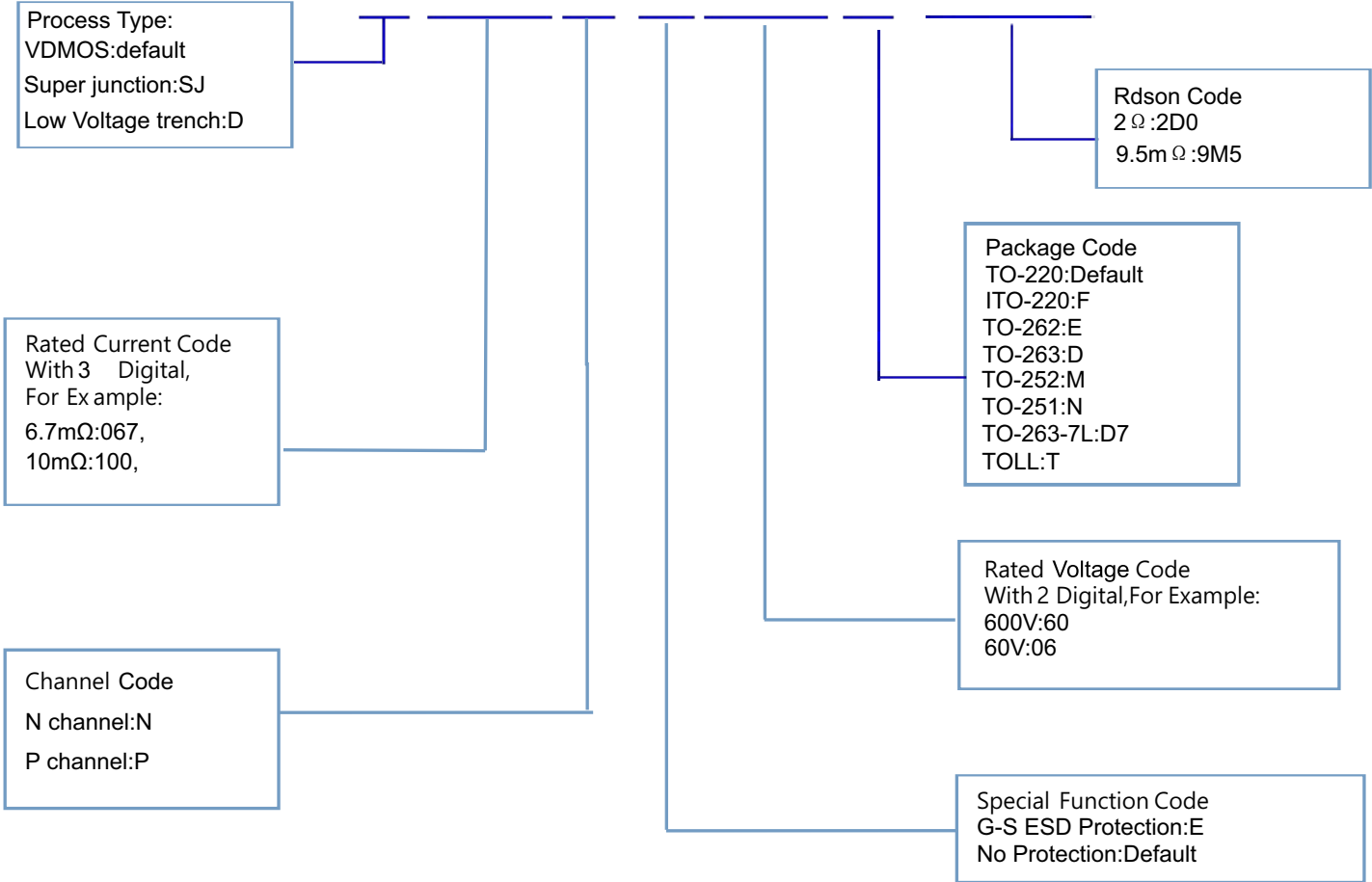
7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

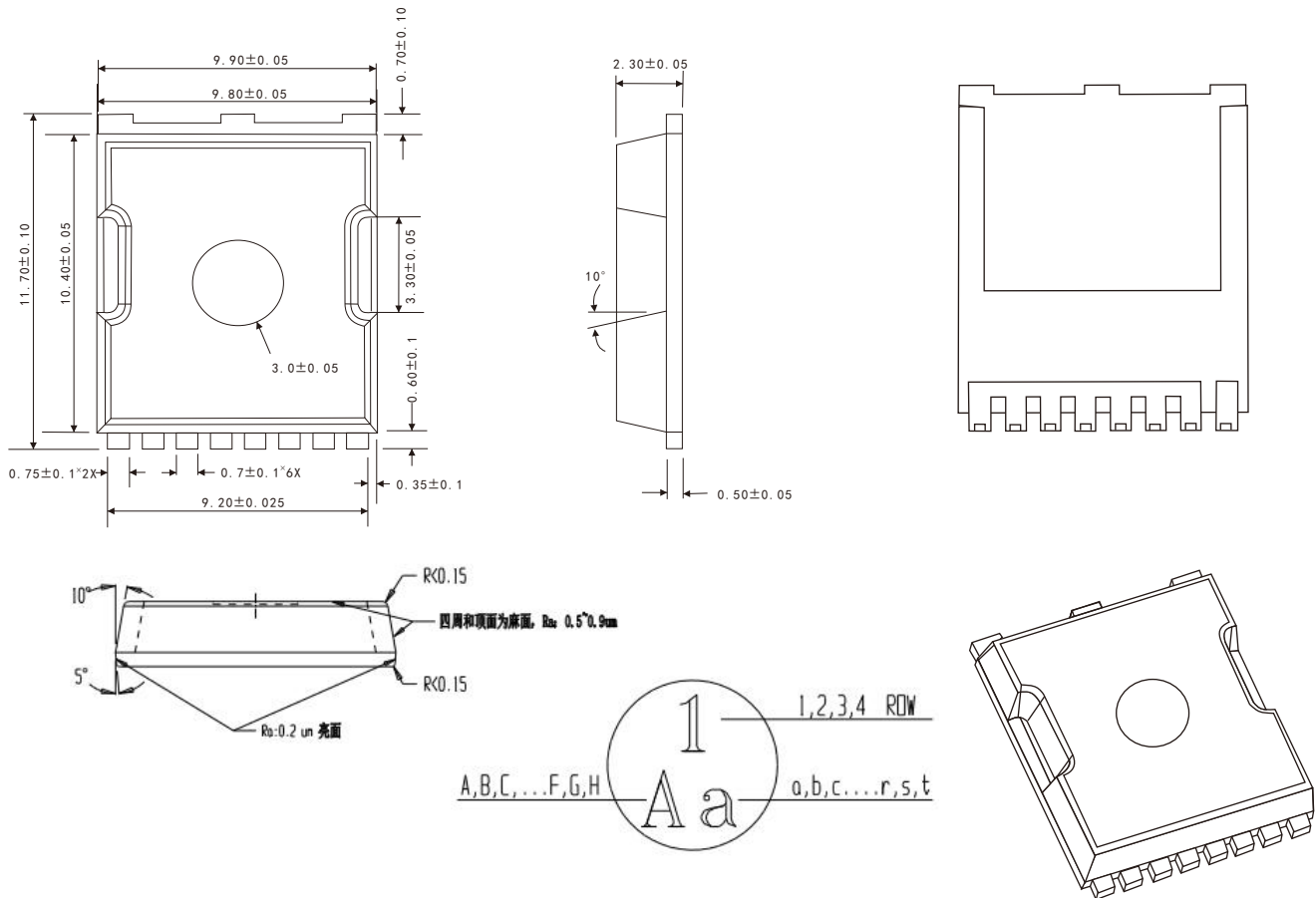
Product Names Rules

X X X N E X X X-X X X

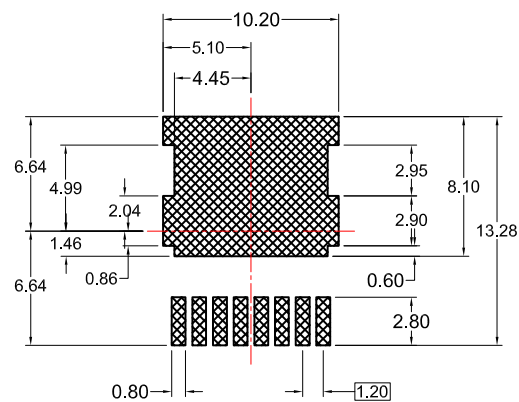


Dimensions

TOLL PACKAGE OUTLINE DIMENSIONS



Suggested Pad Layout





## Friendship Reminder

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