

Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

Product Summary			
V_{DS}	$R_{DS(on)}$ (m Ω) Typ	I_D (A)	Q_g (Typ)
100V	1.1 @ 10V 100A	330	258nc

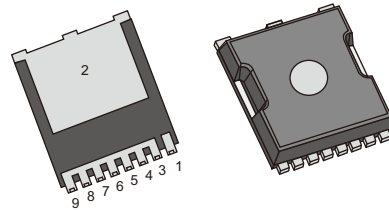
Mechanical Data

- Case:TOLL Package

TOLL
D013N10T

Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications



Ordering Information

Part No.	Package Type	Package	Quality(box)
D013N10T	TOLL	Tape & Reel	2000

Block Diagram

Pin Definition:

- 1. Gate
- 2. Drain
- 3/4/5/6/7/8/9. Source

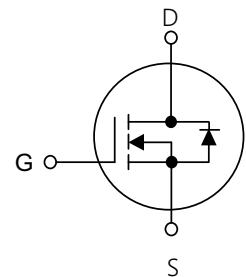


Table1 Absolute Maximum Ratings ($T_c=25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_c=25^\circ\text{C}$	330
		$T_c=100^\circ\text{C}$	248
Pulsed Drain Current (Note 1)	I_{DM}	1320	A
Single Pulse Avalanche Energy(Note 2)	E_{AS}	1750	mJ
Power Dissipation $T_c=25^\circ\text{C}$	P_D	431	W
Operating Junction and Storage Temperature	T_J/T_{STG}	-55~+150	$^\circ\text{C}$

Table 2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient. Max	$R_{\theta JA}$	46	$^{\circ}C/W$
Thermal resistance Junction to Case. Max	$R_{\theta JC}$	0.29	$^{\circ}C/W$

Table 3. Electrical Characteristics ($T_J=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA	
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Reverse	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.2	-	3.8	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=100A$	-	1.1	1.3	m Ω	
Dynamic Characteristics(Note 4)							
Input Capacitance	C_{ISS}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	15650	-	pF	
Output Capacitance	C_{OSS}		-	2100	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	80	-	pF	
Switching Characteristics (Note 4)							
Turn-On Delay Time	$t_d(on)$	$V_{DS}=50V, I_D=100A,$ $V_{GS}=10V, R_G=3\Omega,$	-	28	-	ns	
Turn-On Rise Time	t_r		-	73	-	ns	
Turn-Off Delay Time	$t_d(off)$		-	86	-	ns	
Turn-Off Fall Time	t_f		-	33	-	ns	
Total Gate Charge	Q_G	$V_{DS}=50V, I_D=100A,$ $V_{GS}=10V$	-	258	-	nC	
Gate-Source Charge	Q_{GS}		-	68	-	nC	
Gate-Drain Charge	Q_{GD}		-	74	-	nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=100A$	-	-	1.1	V	
Reverse Recovery Time	t_{rr}	$I_F=100A, dI_F/dt=100A/\mu s$	-	115	-	ns	
Reverse Recovery Charge	Q_{RR}	$I_F=100A, dI_F/dt=100A/\mu s$	-	320	-	nC	

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature

2 $L = 0.3mH, V_{DS} = 75V, V_{GS} = 10V, Starting T_J=25^{\circ}C$

3 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$

4 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

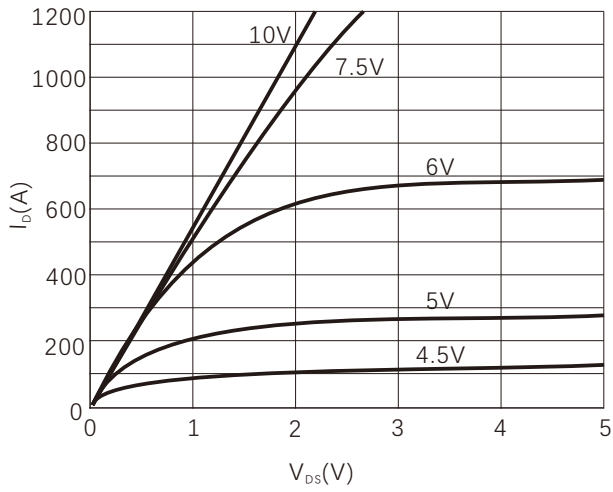


Figure 2. Normalized $R_{DS(ON)}$ vs Temperature

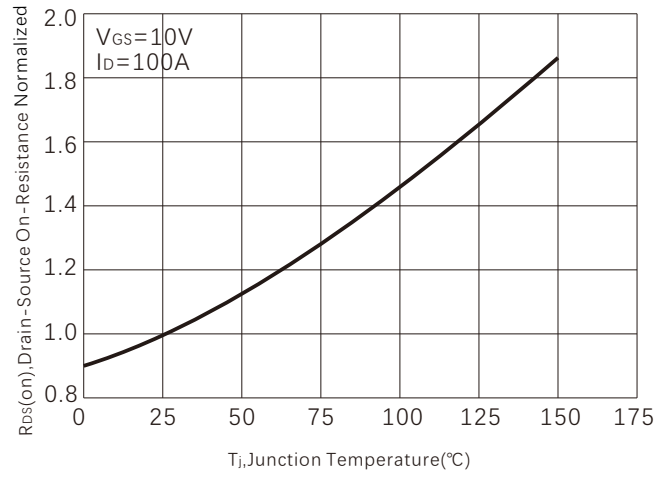


Figure 3. On-Resistance vs. Drain Current

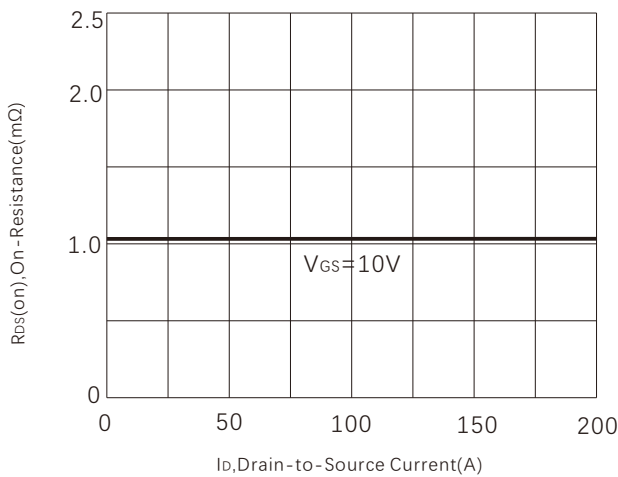


Figure 4. Capacitance

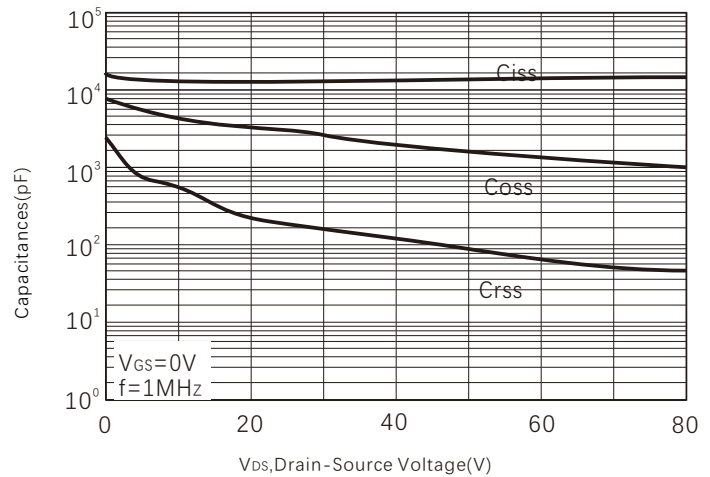


Figure 5. Gate charge

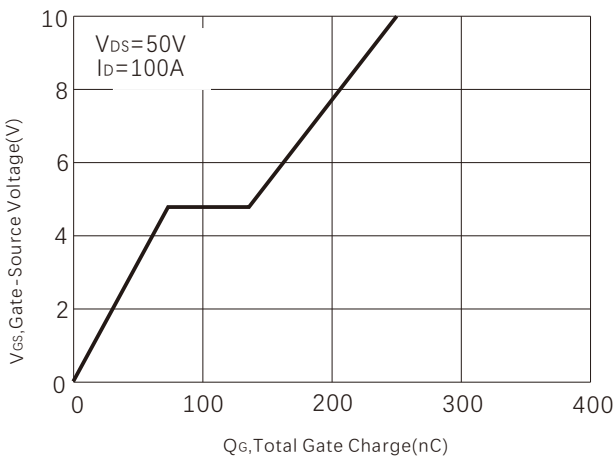


Figure 6. Source-Drain Diode Forward Voltage

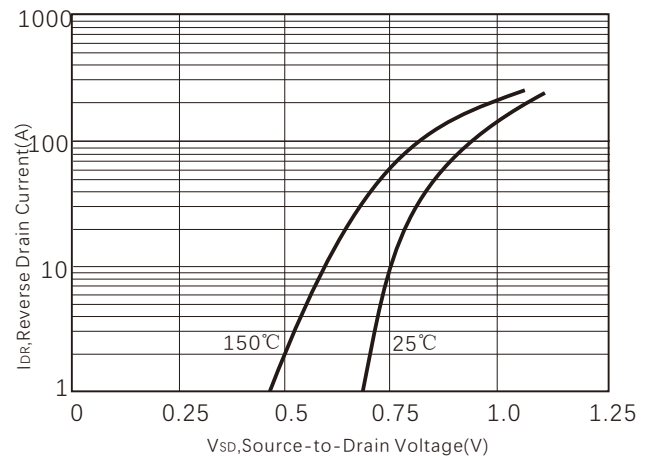


Figure 7. Maximum Drain Current vs Temperature

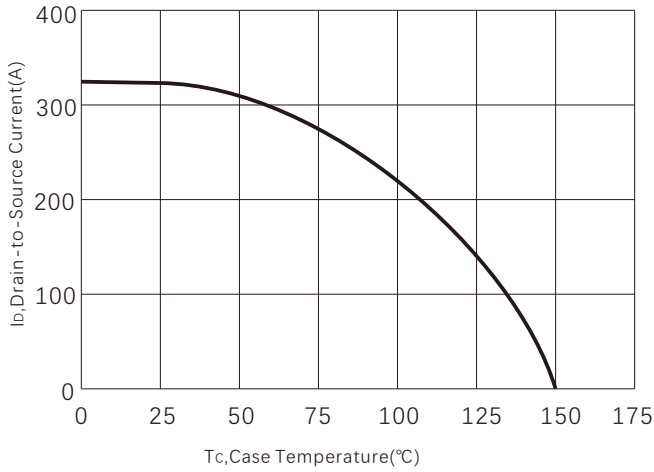


Figure 8. Power dissipation

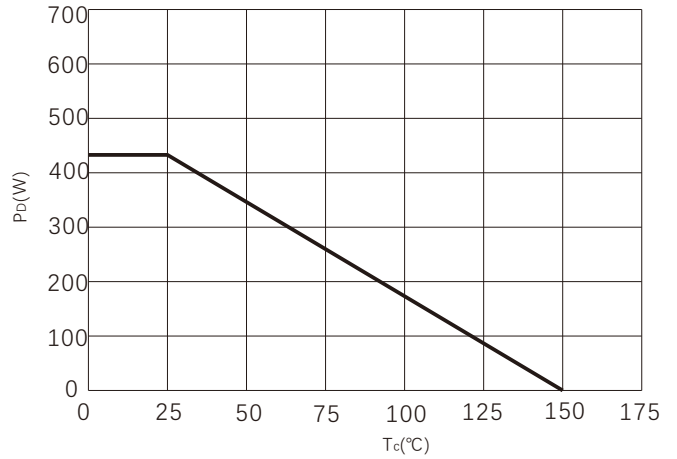


Figure 9. Safe operating area

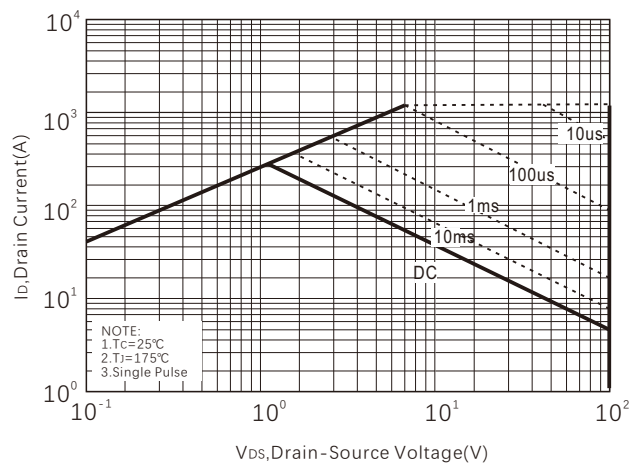
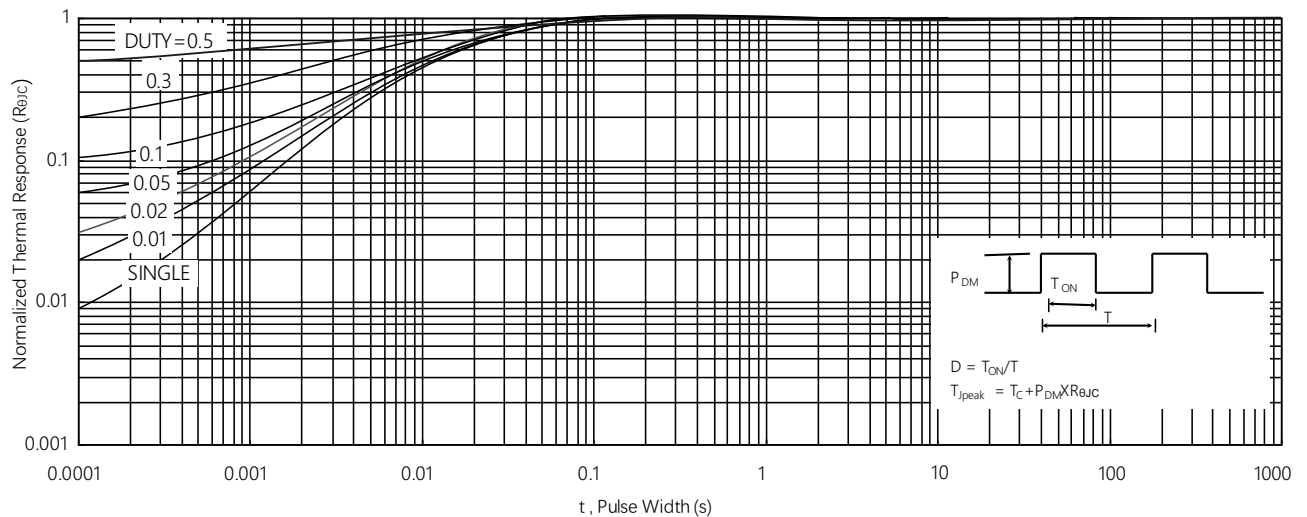
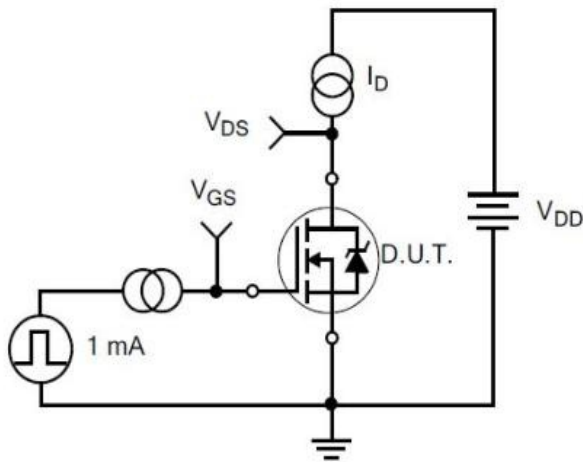


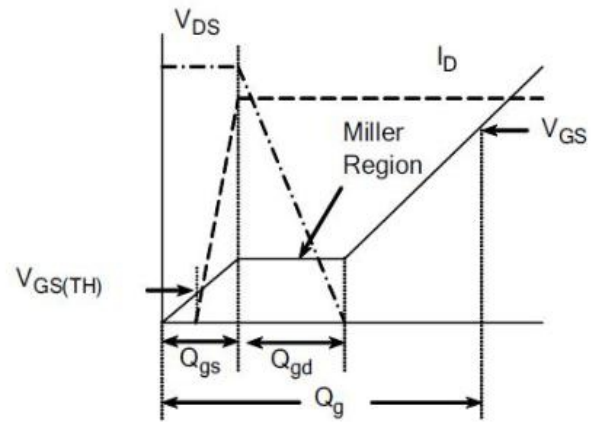
Figure 10. Normalized Maximum Transient Thermal Impedance



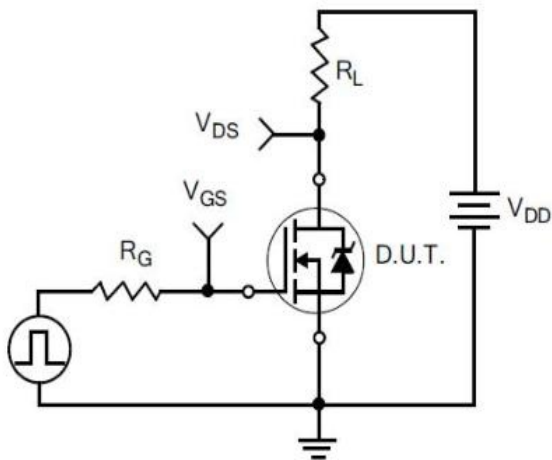
Typical Test Circuit



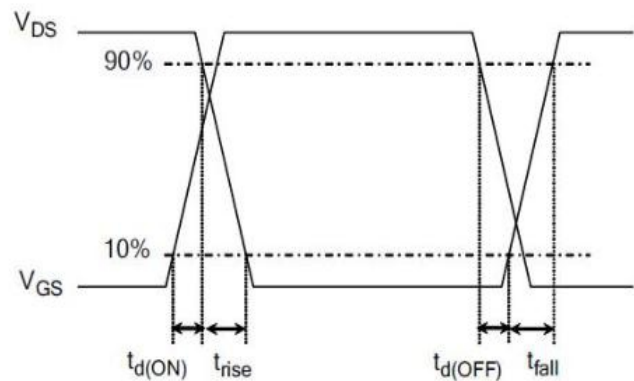
1) Gate Charge Test Circuit



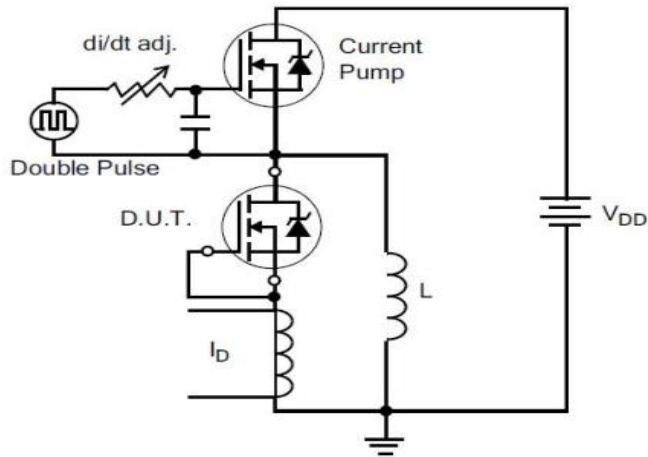
2) Gate Charge Waveform



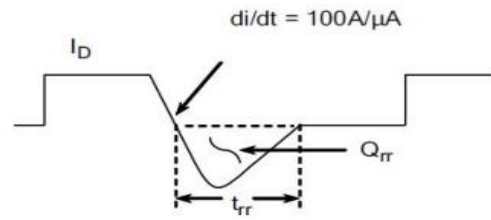
3) Resistive Switching Test Circuit



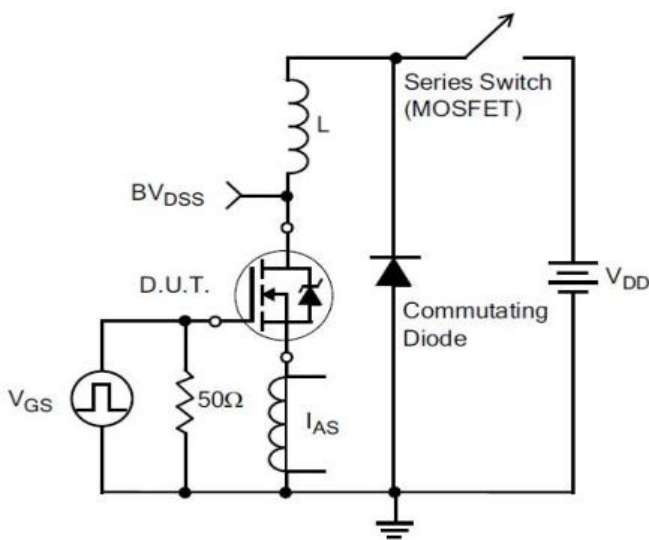
4) Resistive Switching Waveforms



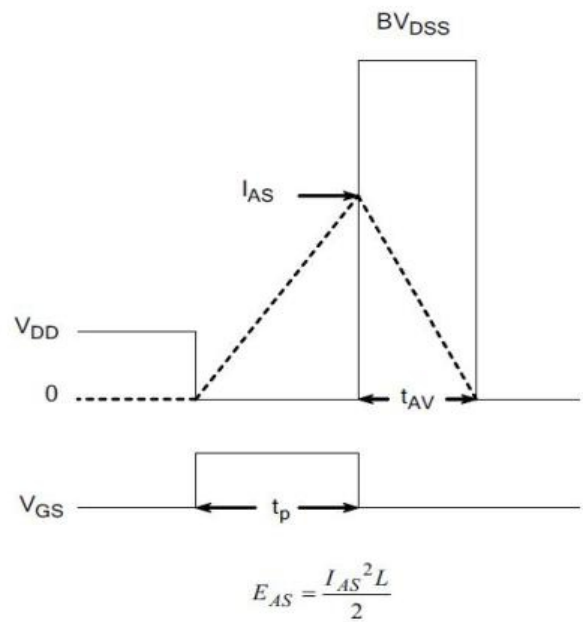
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



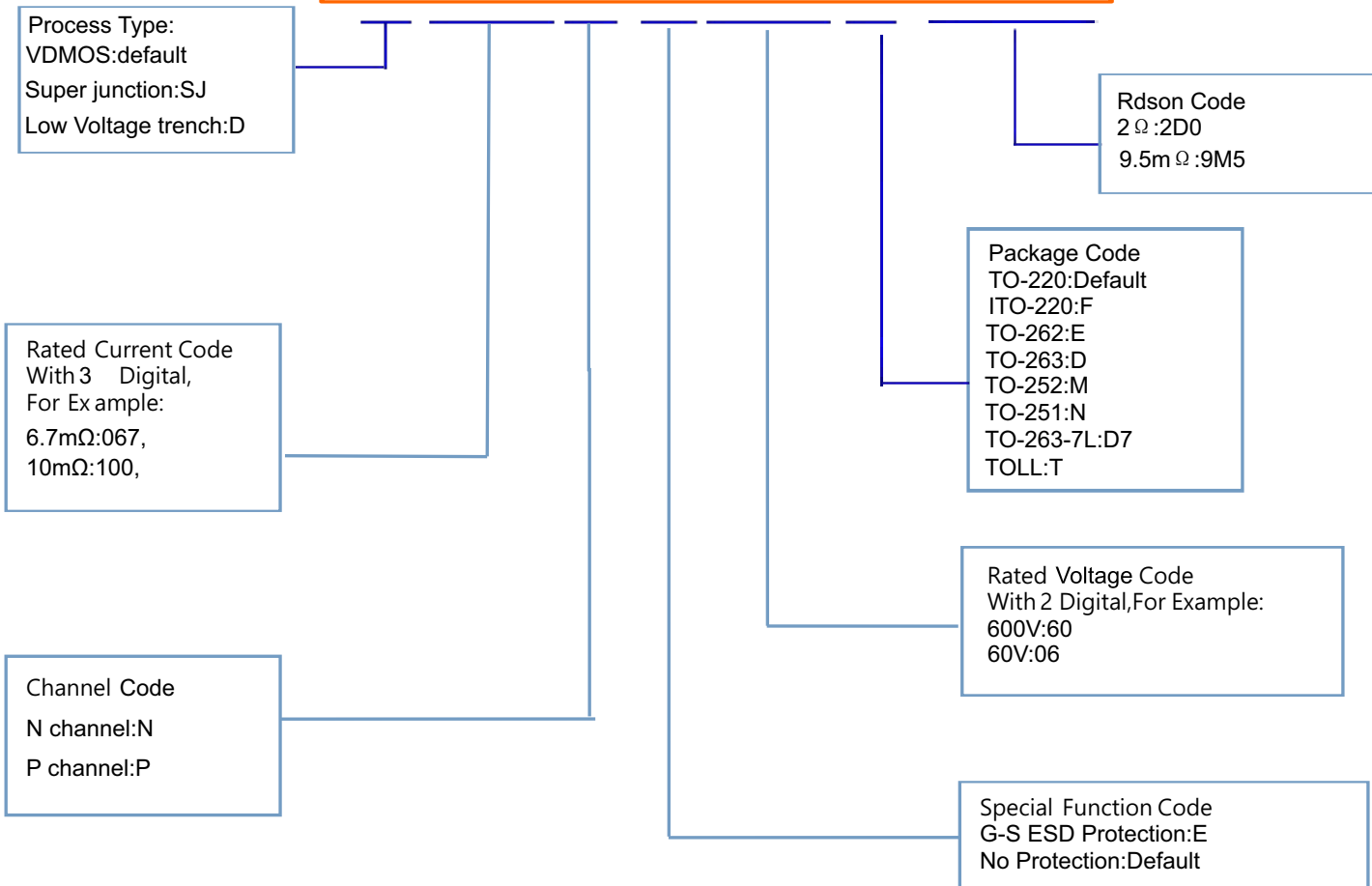
7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

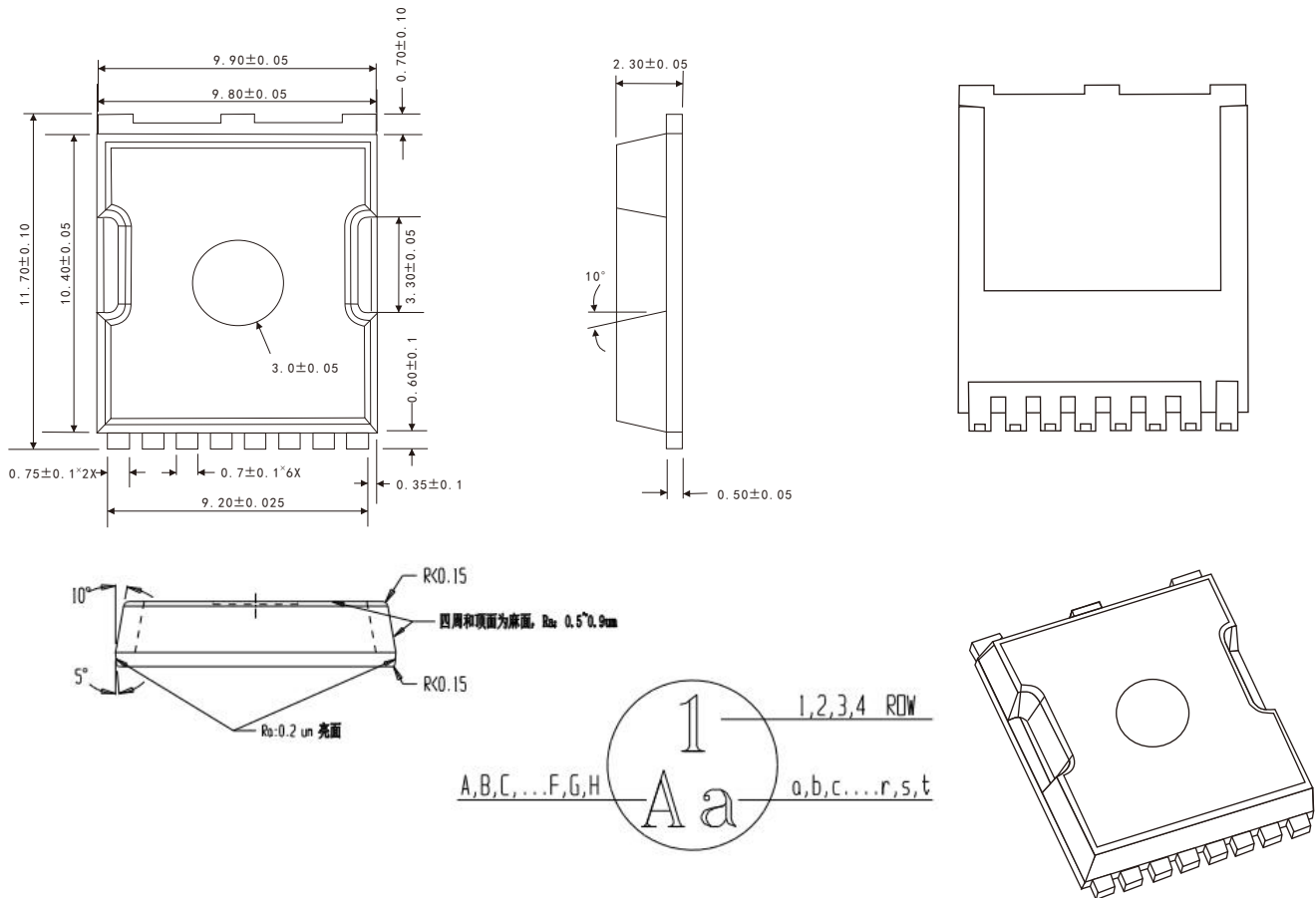
Product Names Rules

X X X N E X X X-X X X

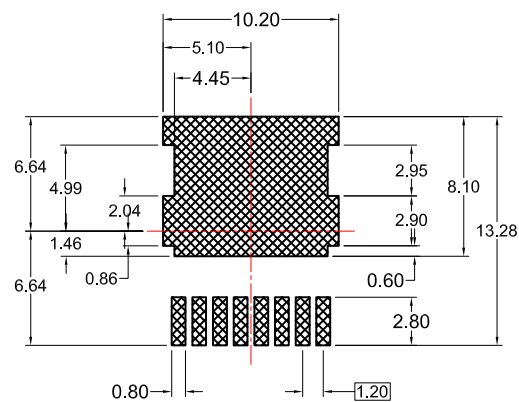


Dimensions

TOLL PACKAGE OUTLINE DIMENSIONS



Suggested Pad Layout



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