

Features

- Advanced Trench MOS Technology
- Low $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

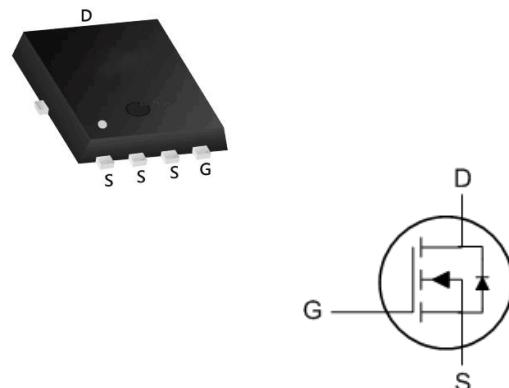
Product Summary

BVDSS	RDS(on)	ID
40V	2.7mΩ	112A

Applications

- SMPS Synchronous Rectification
- DC/DC Converters
- Or-ing

DFN5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	112	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	71	A
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	22.8	A
$I_D @ T_A=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	14.4	A
I_{DM}	Pulsed Drain Current ²	400	A
EAS	Single Pulse Avalanche Energy ³	162	mJ
I_{AS}	Avalanche Current	57	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	50	W
$P_D @ T_A=25^\circ C$	Total Power Dissipation ⁴	2.1	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	2.2	2.7	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=20\text{A}$	---	3.3	4.0	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	1.8	2.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	45.8	---	nC
Q_{gs}	Gate-Source Charge		---	8	---	
Q_{gd}	Gate-Drain Charge		---	10.6	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=1\Omega$, $I_D=1\text{A}$	---	15.8	---	ns
T_r	Rise Time		---	9.5	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	35.6	---	
T_f	Fall Time		---	36.3	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	2643	---	pF
C_{oss}	Output Capacitance		---	861	---	
C_{rss}	Reverse Transfer Capacitance		---	81	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	85	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=57\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 85A.

Typical Characteristics

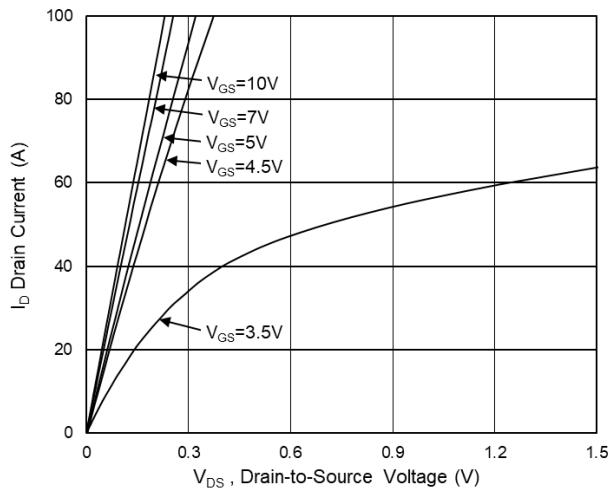


Fig.1 Typical Output Characteristics

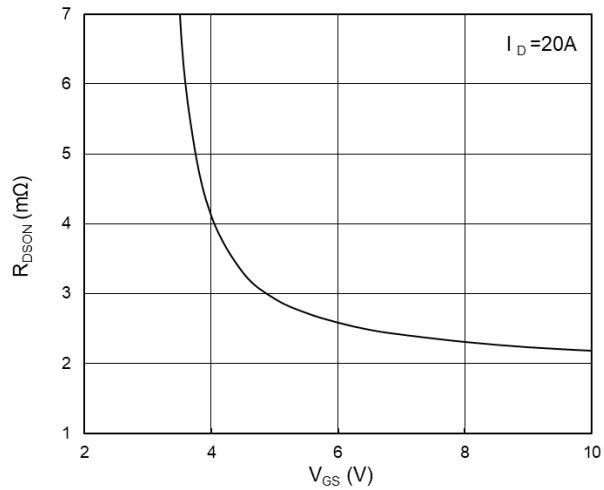


Fig.2 On-Resistance vs G-S Voltage

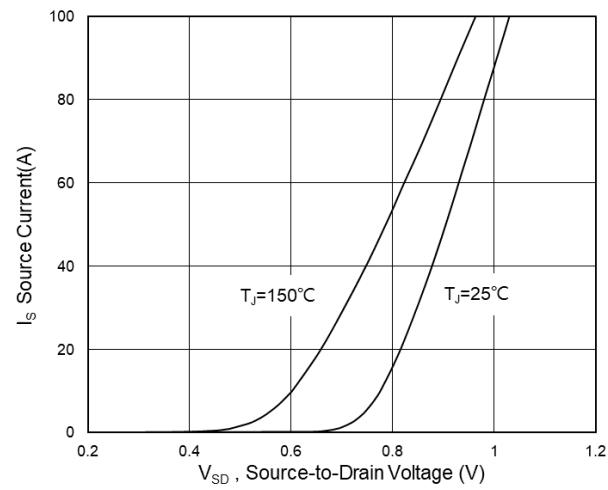


Fig.3 Source Drain Forward Characteristics

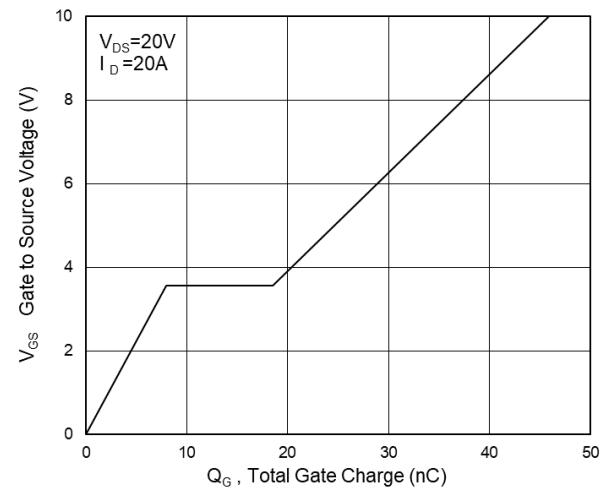


Fig.4 Gate-Charge Characteristics

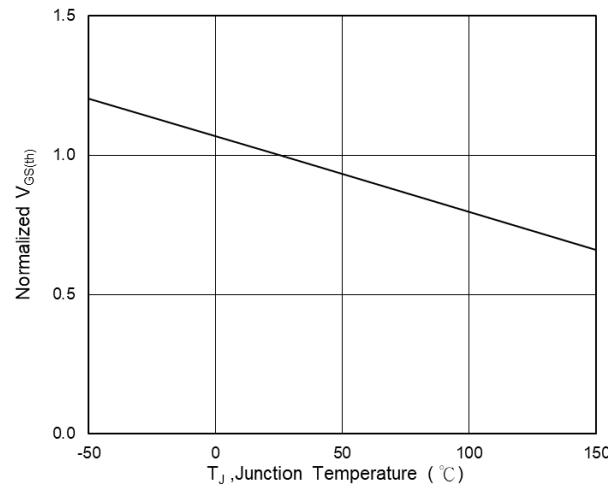


Fig.5 Normalized $V_{GS(th)}$ vs T_J

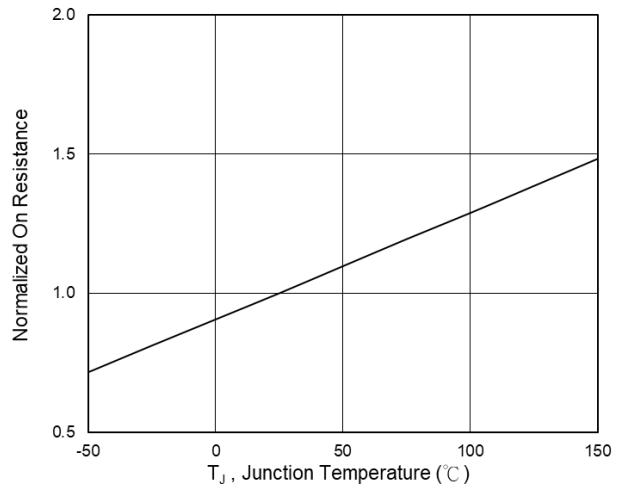
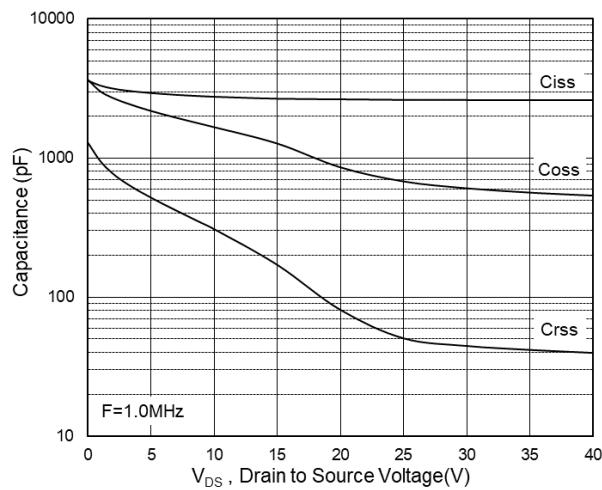
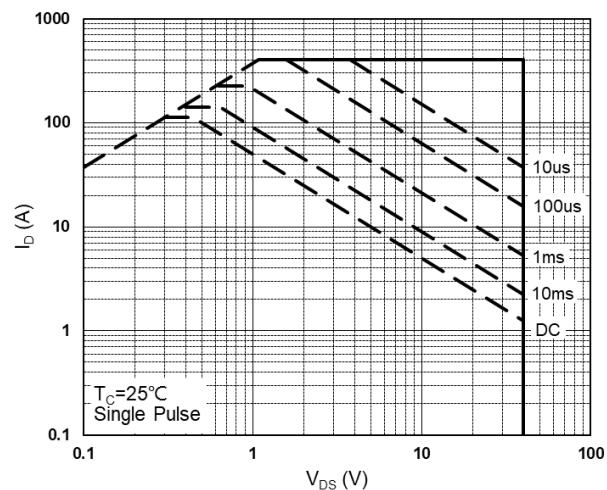
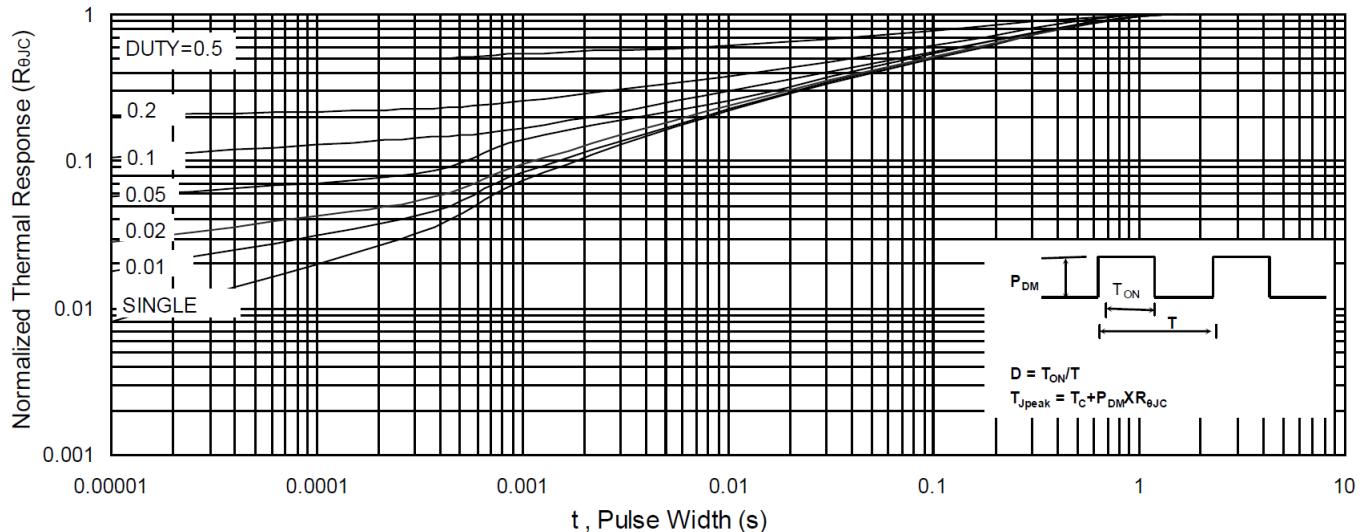
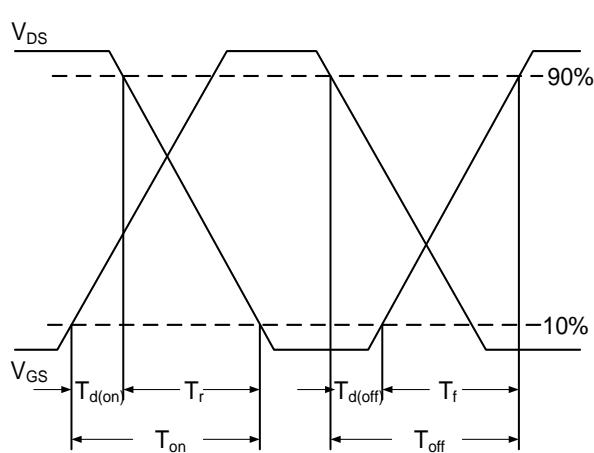
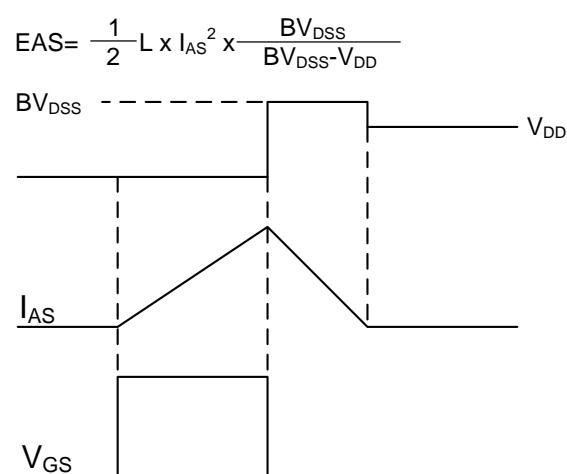
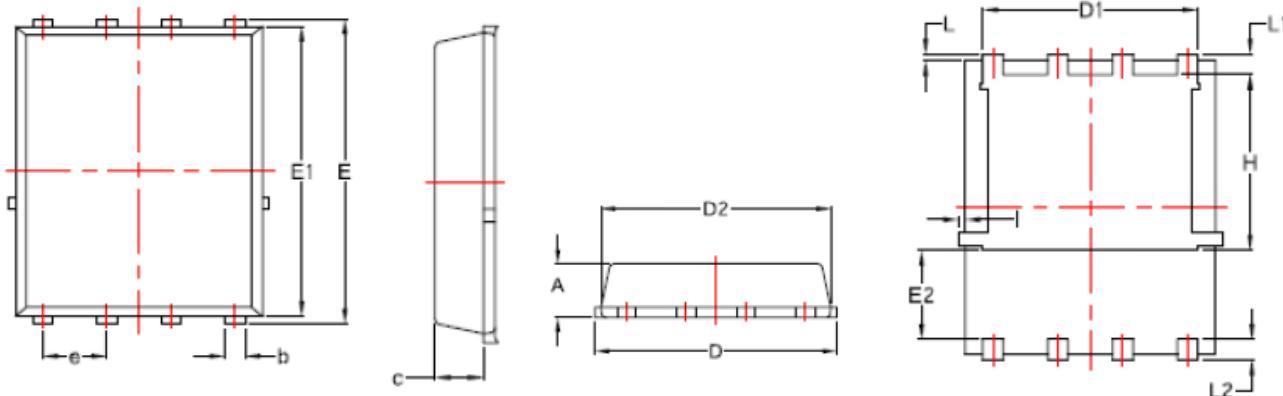


Fig.6 Normalized $R_{DS(on)}$ vs T_J

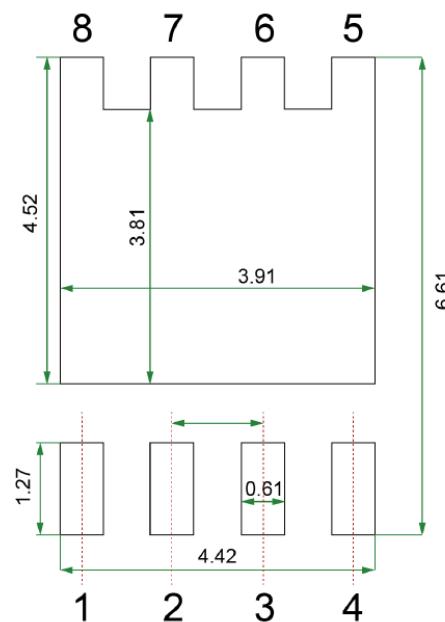

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

DFN5×6 Outline



Land Pattern (Only for Reference)
Unit : mm

SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.20	0.0354	0.0474
b	0.30	0.51	0.0118	0.0200
c	0.60	1.046	0.0236	0.0412
D	4.80	5.45	0.1890	0.2146
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.20	0.1890	0.2047
E	5.90	6.35	0.2323	0.2500
E1	5.65	6.06	0.2224	0.2386
E2	1.10	-	0.0433	-
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.61	0.0150	0.0240
L2	0.30	0.71	0.0118	0.0280
H	3.30	3.92	0.1300	0.1543
I	-	0.18	-	0.0070



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