

## Features

- Advanced Trench MOS Technology
- Low Gate Charge
- Low  $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

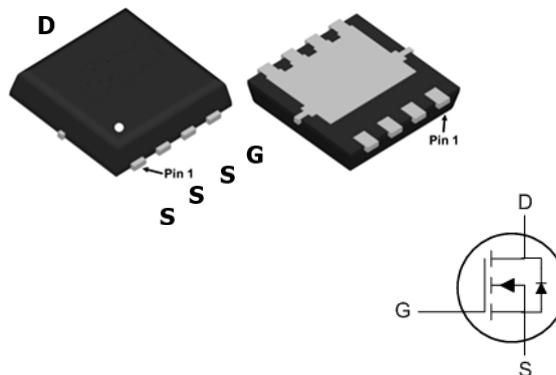
## Product Summary

<b>BVDSS</b>	<b>RDS(on)</b>	<b>ID</b>
30V	3.8mΩ	40

## Applications

- Power Management in Desktop Computer or DC/DC Converters.
- Isolated DC/DC Converters in Telecom and Industrial.

## DFN 3X3 Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	40	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1.6}$	40	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	100	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	140	mJ
$I_{AS}$	Avalanche Current	53	A
$P_D @ T_c = 25^\circ C$	Total Power Dissipation <sup>4</sup>	26	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	4.8	°C/W

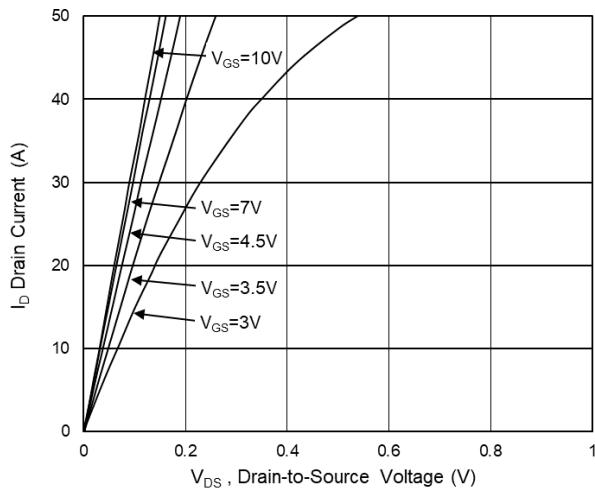
**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$ , $I_D=250\mu\text{A}$	30	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=10\text{V}$ , $I_D=15$	---	---	3.8	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$ , $I_D=12$	---	---	5.8	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$ , $I_D=250\mu\text{A}$	1.2	---	2.5	V
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=30\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $T_J=25^{\circ}\text{C}$	---	---	1	$\text{uA}$
		$V_{\text{DS}}=30\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $T_J=55^{\circ}\text{C}$	---	---	5	
$I_{\text{GSS}}$	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$ , $V_{\text{DS}}=0\text{V}$	---	---	$\pm 100$	nA
$R_g$	Gate Resistance	$V_{\text{DS}}=0\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $f=1\text{MHz}$	---	1.7	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{\text{DS}}=20\text{V}$ , $V_{\text{GS}}=4.5\text{V}$ , $I_D=15\text{A}$	---	23.4	---	$\text{nC}$
$Q_{\text{gs}}$	Gate-Source Charge		---	11.4	---	
$Q_{\text{gd}}$	Gate-Drain Charge		---	8.2	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}$ , $V_{\text{GS}}=10\text{V}$ , $R_G=1.5\Omega$	---	12.6	---	$\text{ns}$
$T_r$	Rise Time		---	9.6	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	55	---	
$T_f$	Fall Time		---	5.6	---	
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}}=15\text{V}$ , $V_{\text{GS}}=0\text{V}$ , $f=1\text{MHz}$	---	2461	---	$\text{pF}$
$C_{\text{oss}}$	Output Capacitance		---	383	---	
$C_{\text{rss}}$	Reverse Transfer Capacitance		---	261	---	
<b>Diode Characteristics</b>						
$I_s$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0\text{V}$ , Force Current	---	---	40	A
$V_{\text{SD}}$	Diode Forward Voltage <sup>2</sup>	$V_{\text{GS}}=0\text{V}$ , $I_s=1\text{A}$ , $T_J=25^{\circ}\text{C}$	---	---	1	V

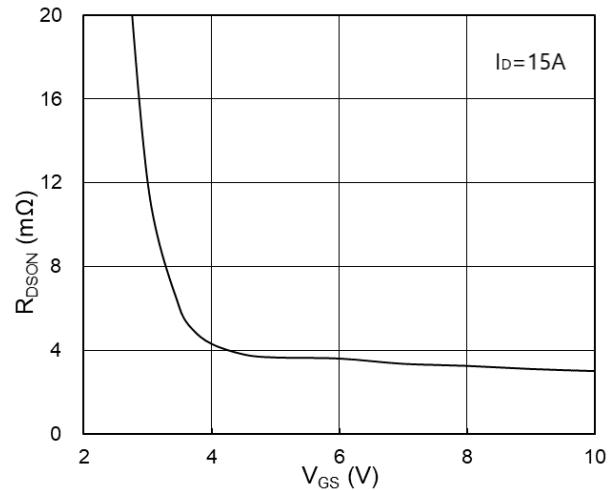
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{\text{DD}}=25\text{V}$ , $V_{\text{GS}}=10\text{V}$ , $L=0.1\text{mH}$ , $I_{\text{AS}}=53\text{A}$
- 4.The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_b$  and  $I_s$  , in real applications , should be limited by total power dissipation.
- 6.The maximum current rating is package limited.

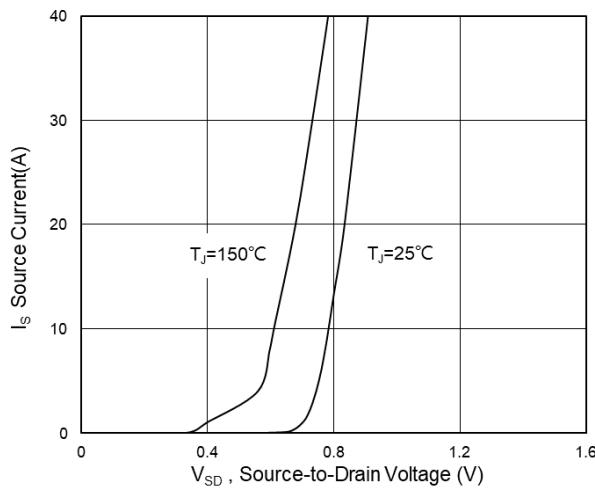
### Typical Characteristics



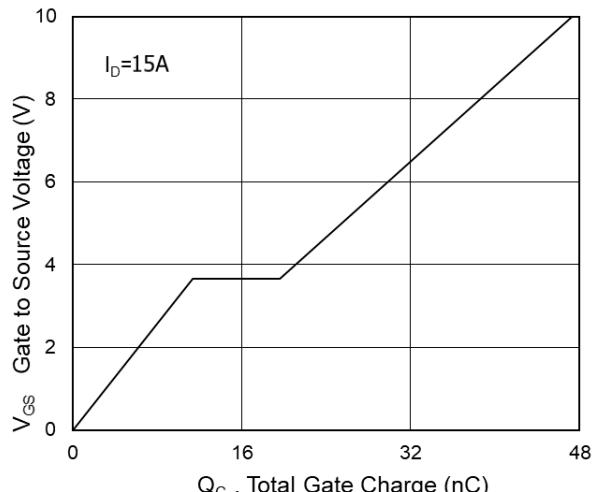
**Fig.1 Typical Output Characteristics**



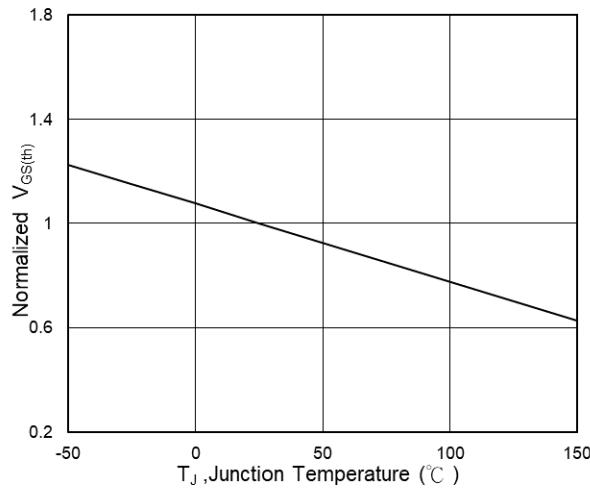
**Fig.2 On-Resistance vs G-S Voltage**



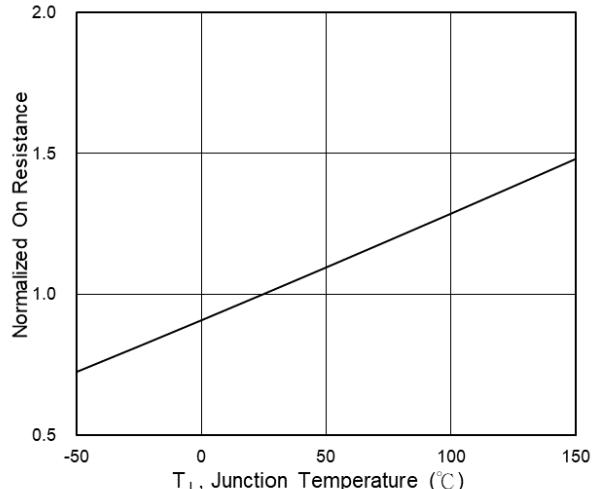
**Fig.3 Source Drain Forward Characteristics**



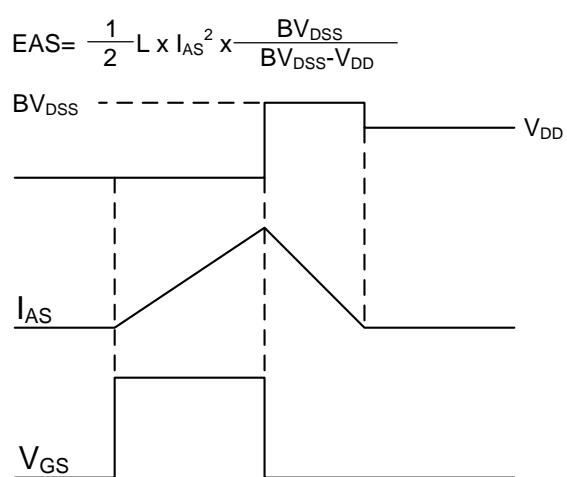
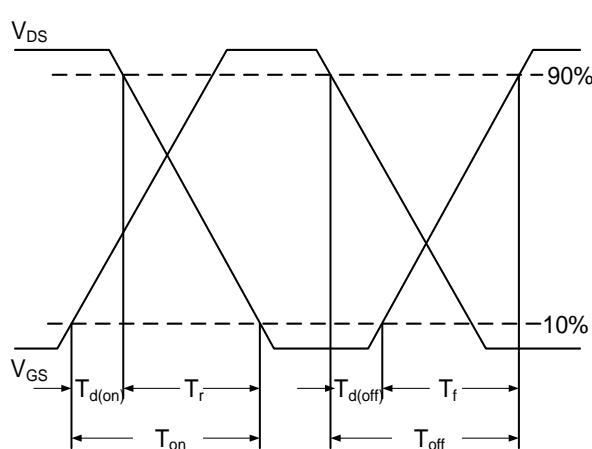
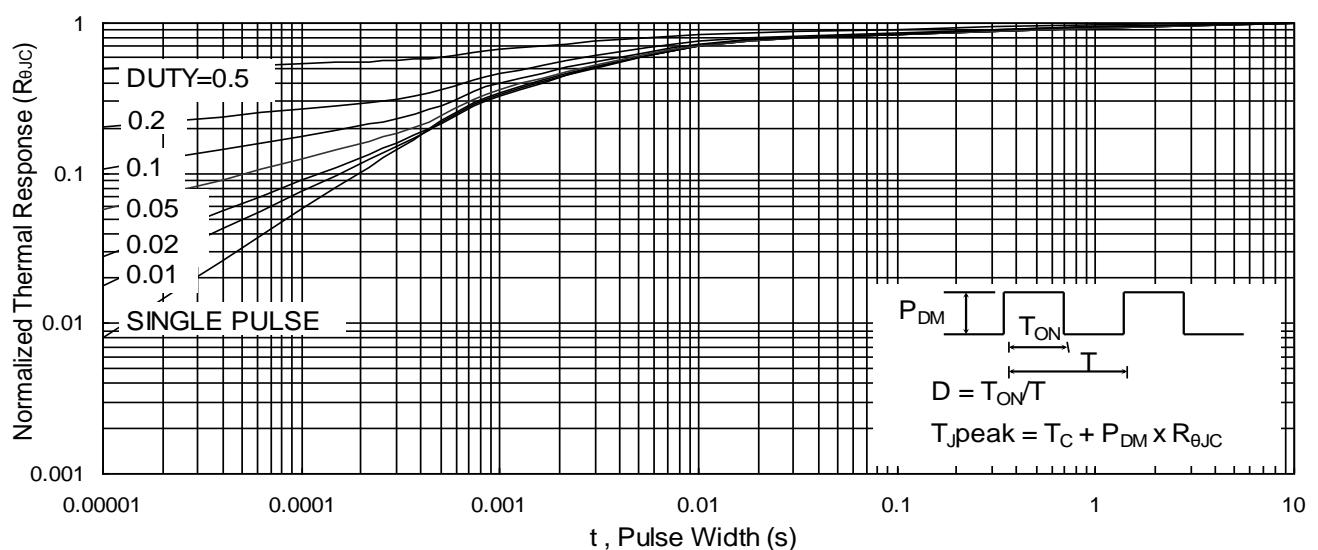
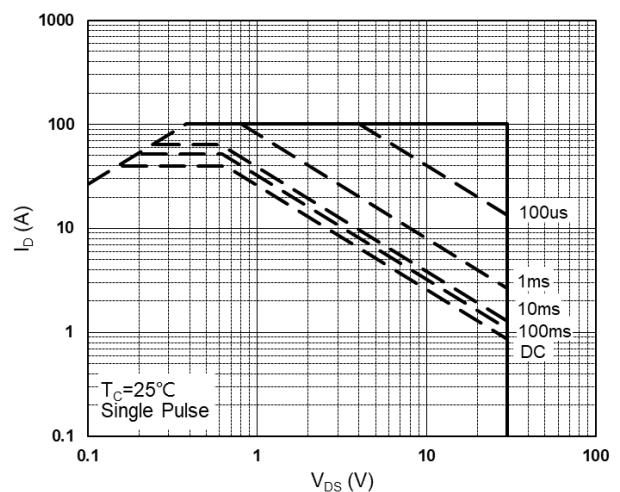
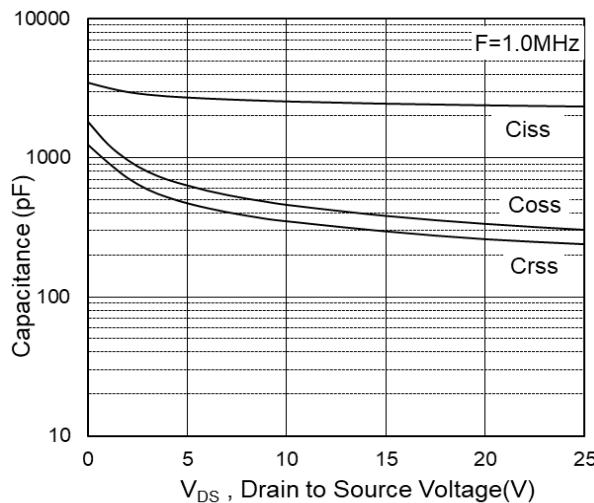
**Fig.4 Gate-Charge Characteristics**



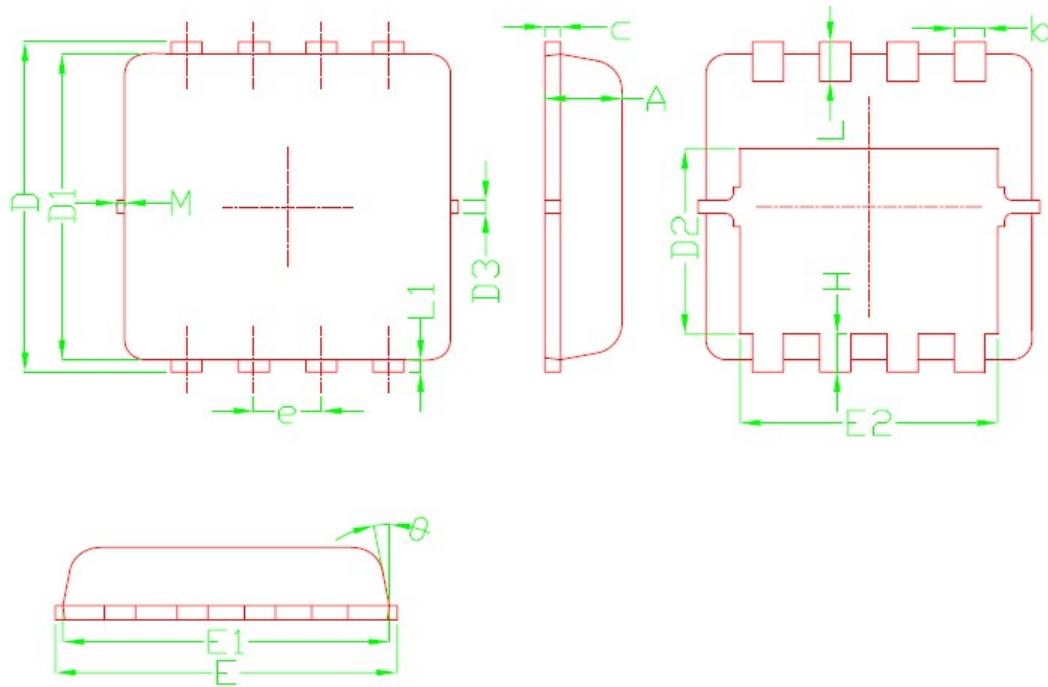
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



## DFN3x3-8L Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.85	0.027	0.034
b	0.20	0.40	0.007	0.016
c	0.10	0.25	0.004	0.010
D	3.15	3.45	0.124	0.136
D1	2.90	3.20	0.114	0.126
D2	1.54	1.98	0.060	0.080
D3	0.10	0.30	0.004	0.012
E	3.15	3.45	0.124	0.136
E1	3.00	3.25	0.118	0.128
E2	2.29	2.65	0.090	0.104
e	0.65 BSC		0.025 BSC	
H	0.28	0.65	0.011	0.026
$\Theta$	$0^\circ$	$14^\circ$	$0^\circ$	$14^\circ$
L	0.30	0.50	0.012	0.020
L1	0.13		0.005	
M	---	0.15	---	0.006

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