

Features

- Advanced Trench MOS Technology
- Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available

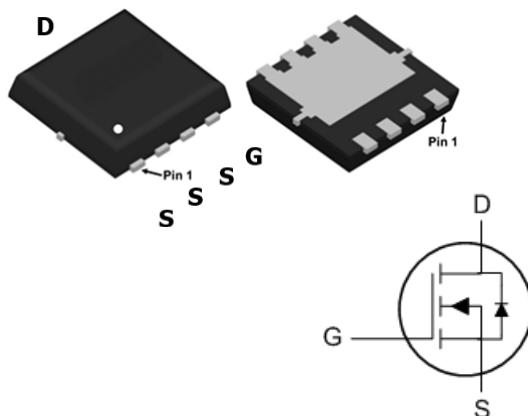
Product Summary

BVDSS	RDS(ON)	ID
40V	6.5mΩ	45A

DFN 3X3 Pin Configuration

Applications

- SMPS Synchronous Rectification
- DC/DC Converters
- Or-ing



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	40	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	45	A
I _D @T _c =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	29	A
I _{DM}	Pulsed Drain Current ²	90	A
EAS	Single Pulse Avalanche Energy ³	68	mJ
I _{AS}	Avalanche Current	37	A
P _D @T _c =25°C	Total Power Dissipation ⁴	20.8	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	65	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_D=250\mu\text{A}$	40	---	---	V
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=15\text{A}$	---	---	6.5	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}$, $\text{I}_D=15\text{A}$	---	---	10.5	
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}$, $\text{I}_D=250\mu\text{A}$	1.2	1.9	2.2	V
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=32\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $\text{T}_J=25^\circ\text{C}$	---	---	1	uA
		$\text{V}_{\text{DS}}=32\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $\text{T}_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}$, $\text{V}_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$\text{V}_{\text{DS}}=0\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.9	---	Ω
Q_g	Total Gate Charge	$\text{V}_{\text{DS}}=20\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{I}_D=15\text{A}$	---	19.8	---	nC
Q_{gs}	Gate-Source Charge		---	3.9	---	
Q_{gd}	Gate-Drain Charge		---	4.7	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=20\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{R}_G=3\Omega$, $\text{I}_D=15\text{A}$	---	11.5	---	ns
T_r	Rise Time		---	9.2	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	23.8	---	
T_f	Fall Time		---	15.4	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=20\text{V}$, $\text{V}_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1078	---	pF
C_{oss}	Output Capacitance		---	483	---	
C_{rss}	Reverse Transfer Capacitance		---	49	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,6}	$\text{V}_G=\text{V}_D=0\text{V}$, Force Current	---	---	40	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}$, $\text{I}_s=1\text{A}$, $\text{T}_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $\text{V}_{\text{DD}}=25\text{V}$, $\text{V}_{\text{GS}}=10\text{V}$, $\text{L}=0.1\text{mH}$, $\text{I}_{\text{AS}}=37\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 40A.

Typical Characteristics

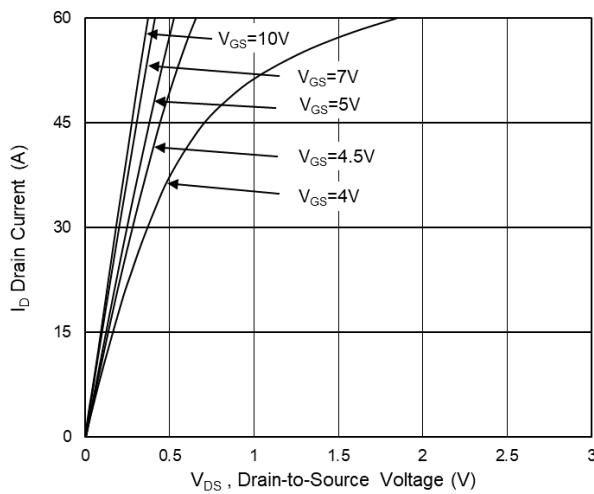


Fig.1 Typical Output Characteristics

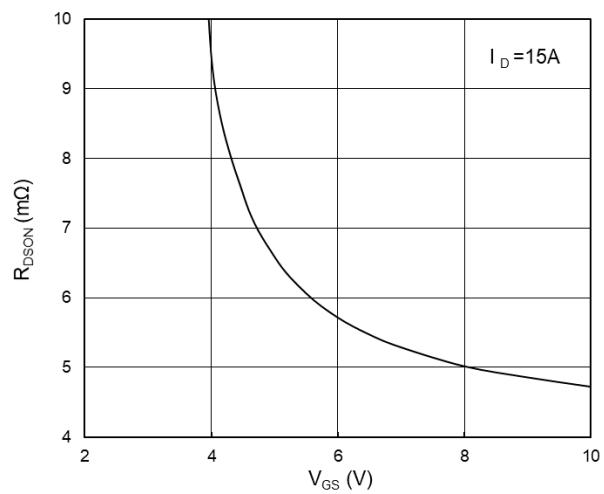


Fig.2 On-Resistance vs G-S Voltage

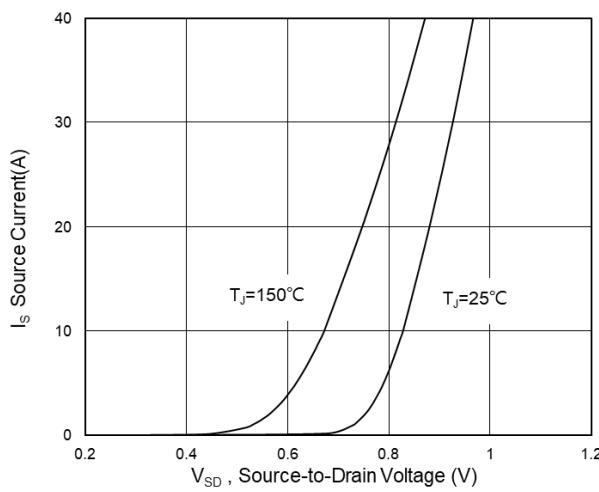


Fig.3 Source Drain Forward Characteristics

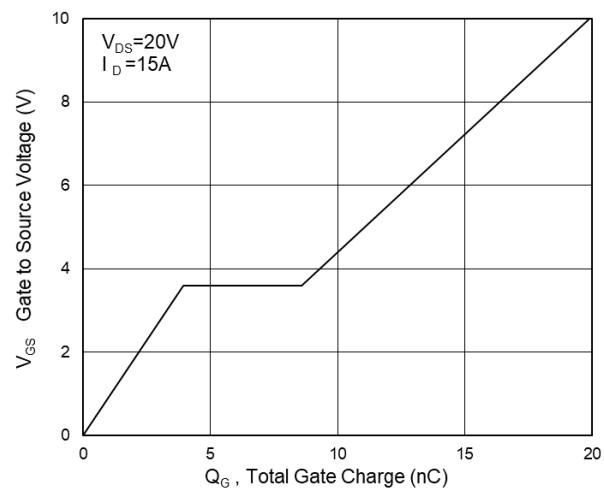


Fig.4 Gate-Charge Characteristics

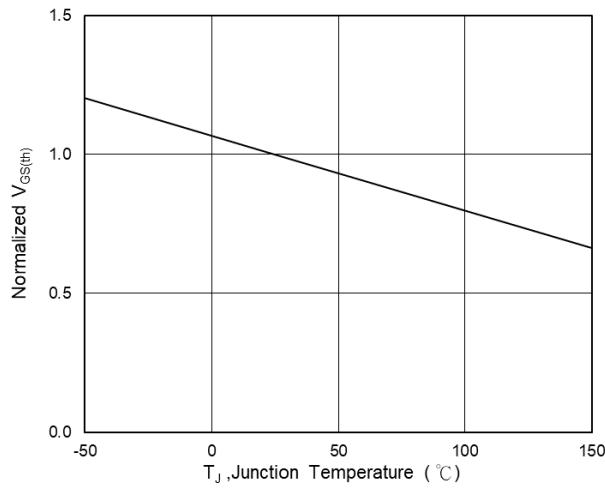


Fig.5 Normalized $V_{GS(th)}$ vs T_J

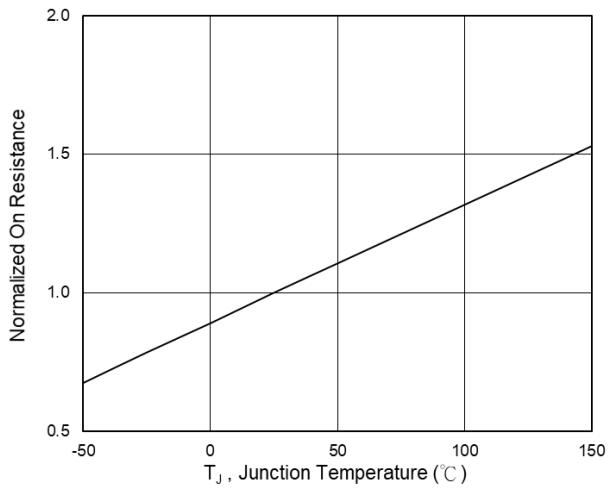
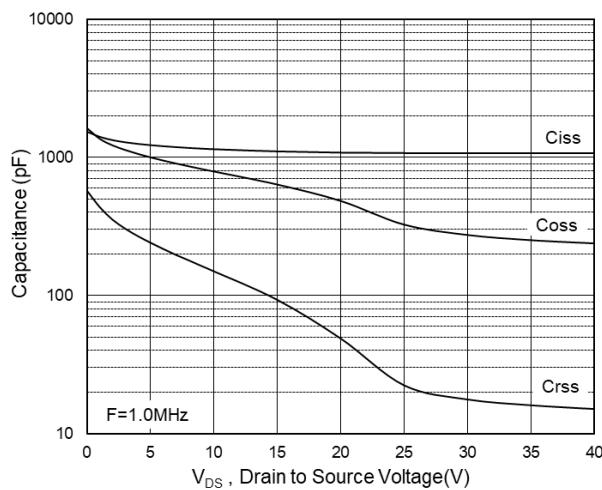
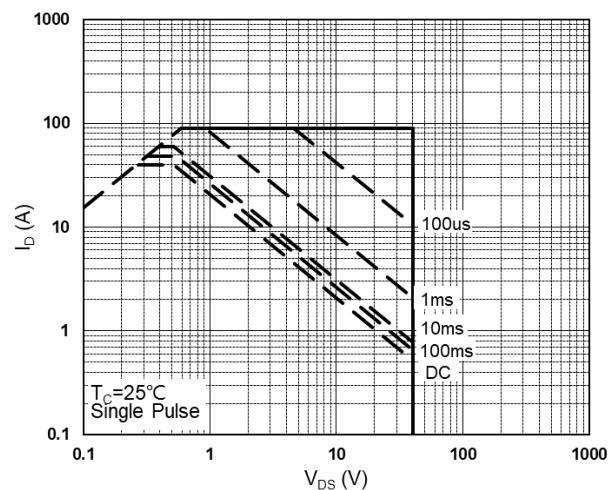
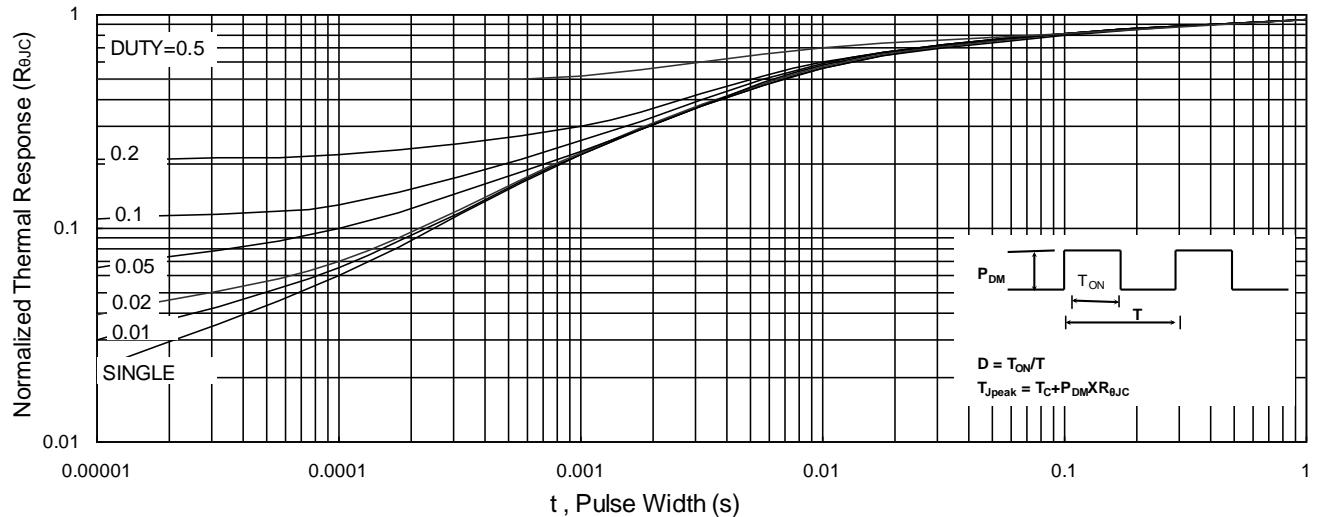
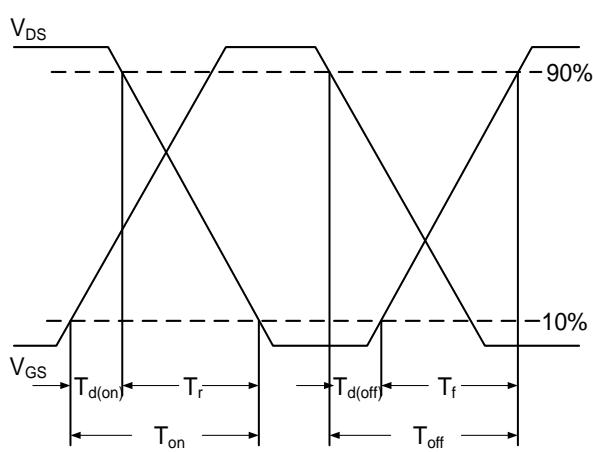
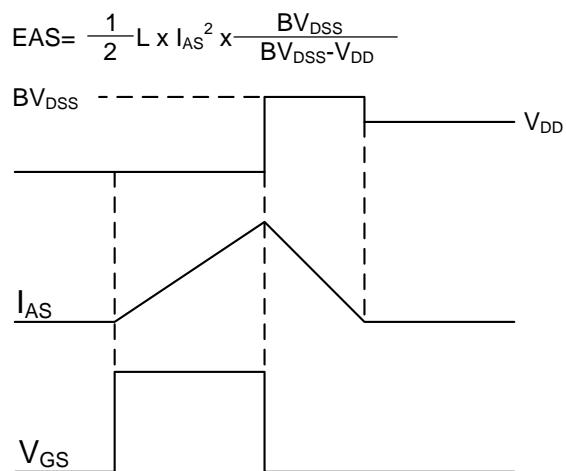
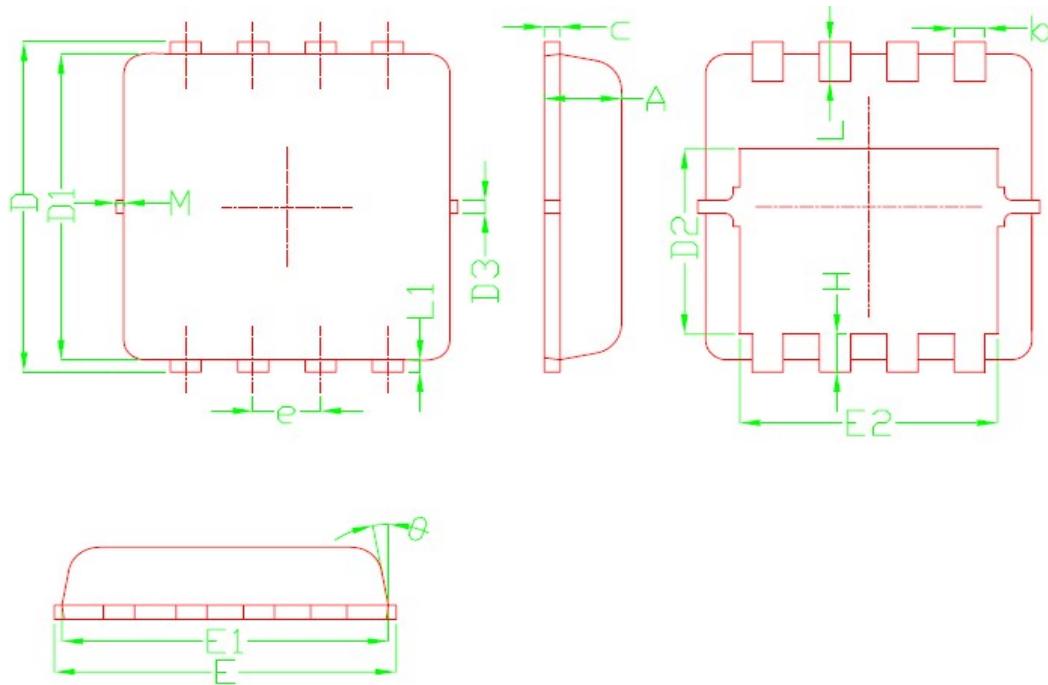


Fig.6 Normalized $R_{DS(on)}$ vs T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

DFN3*3 Package Outline Dimensions



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.85	0.027	0.034
b	0.20	0.40	0.007	0.016
c	0.10	0.25	0.004	0.010
D	3.15	3.45	0.124	0.136
D1	2.90	3.20	0.114	0.126
D2	1.54	1.98	0.060	0.080
D3	0.10	0.30	0.004	0.012
E	3.15	3.45	0.124	0.136
E1	3.00	3.25	0.118	0.128
E2	2.29	2.65	0.090	0.104
e	0.65 BSC		0.025 BSC	
H	0.28	0.65	0.011	0.026
Θ	0°	14°	0°	14°
L	0.30	0.50	0.012	0.020
L1	0.13		0.005	
M	---	0.15	---	0.006

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