

General Description

This series of power MOSFET use N channel Multi-EPI Super-Junction technology and design to provide better characteristics, such as fast switching time, low Ciss and Crss, low on resistance and excellent avalanche characteristics, making it especially suitable for applications which require superior power density and outstanding efficiency.

Features

- Ultra low on-resistance
- New revolutionary high voltage technology
- Ultra low gate charge and input capacitance
- 100% avalanche tested
- Rohs compliant

Mechanical Data

- Case: TO-247 Package

Application

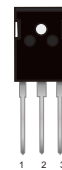
- Electronic switch in
Switcing power supply
UPS
PV & wind power inverter
Lighting

Ordering Information

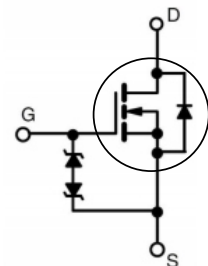
Part No.	Package Type	Package	Quality(box)
SJ90NE65PR	TO-247	Tube	360

Product Summary			
V _{DS}	R _{DS(on)} (mΩ)Typ	I _D (A)	Q _g (Typ)
650V	28 @ 10V,30A	90	183nc

TO-247
SJ90NE65PR



Block Diagram



Pin Definition:

1. Gate
2. Drain
3. Source

Table1 Absolute Maximum Ratings (T_c=25°C, unless otherwise specified)

Parameters	Symbol	SJ90NE65PR	Unit
Drain-Source Voltage	V _{DS}	650	V
Gate-Source Voltage	V _{GS}	±30	V
Contionous Drain Current	I _D	T _C =25°C	90
		T _C =100°C	60
Pulsed Drain Current (Note 2)	I _{DM}	350	A
Single Pulse Avalanche Energy(Note 3)	E _{AS}	2430	mJ
Avalanche Current(Note 1)	I _{AR}	7	A
Repetitive Avalanche Energy(Note 1)	E _{AR}	1.4	mJ
Power Dissipation T _C =25°C	P _D	460	W
Operating Junction and Storage Temperature	T _J /T _{STG}	-55 ~ +150	°C

Table 2. Thermal Characteristics

Parameters	Symbol	SJ90NE65PR	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	0.27	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$			60	μA
Gate- Source Leakage Current	Forward	$V_{GS}=30V, V_{DS}=0V$			10	μA
	Reverse	$V_{GS}=-30V, V_{DS}=0V$			-10	μA
On Characteristics(Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$		28	33	m Ω
Dynamic Characteristics(Note 5)						
Input Capacitance	C_{ISS}	$V_{DS}=100V, V_{GS}=0V, f=1\text{MHz}$		9380		pF
Output Capacitance	C_{OSS}			300		pF
Reverse Transfer Capacitance	C_{RSS}			8.2		pF
Switching Characteristics (Note 5)						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=300V, I_D=30A,$ $V_{GS}=10V, R_G=25\Omega$		123		ns
Turn-On Rise Time	t_r			125		ns
Turn-Off Delay Time	$t_{d(off)}$			625		ns
Turn-Off Fall Time	t_f			143		ns
Total Gate Charge	Q_G	$V_{DS}=480V, I_D=30A,$ $V_{GS}=10V$		190		nC
Gate-Source Charge	Q_{GS}			46		nC
Gate-Drain Charge	Q_{GD}			73		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Voltage(Note 4)	V_{SD}	$V_{GS}=0V, I_S=30A$			1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I_S	$T_J \leq T_{J,max}$			90	A
Reverse Recovery Time	t_{rr}	$V_R=50V, I_F=30A$		230		ns
Reverse Recovery Charge	Q_{RR}	$di/dt=100A/\mu\text{s}$		3.9		μC

- Notes: 1 Repetitive Rating:Pulse width limited by maximum junction temperature
 2 Pulse width t_p limited by $T_{J,max}$
 3 $V_{DD}=200V, I_{AS}=9A, L=60\text{mH}, R_G=25\Omega, \text{starting } T_J=25^{\circ}\text{C}$
 4 Pulse Test: Pulse width $\leq 300\mu\text{s}, \text{Duty cycle} \leq 2\%$
 5 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

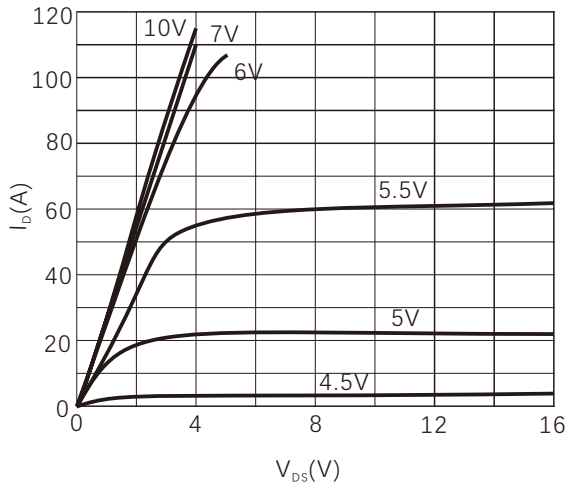


Figure 2. Transfer Characteristics

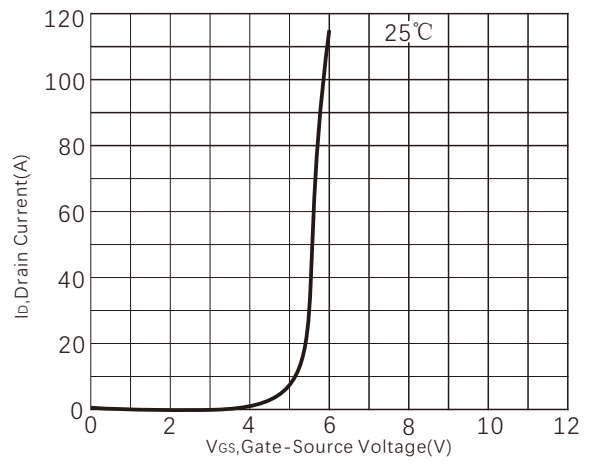


Figure 3. On-Resistance vs. Drain Current

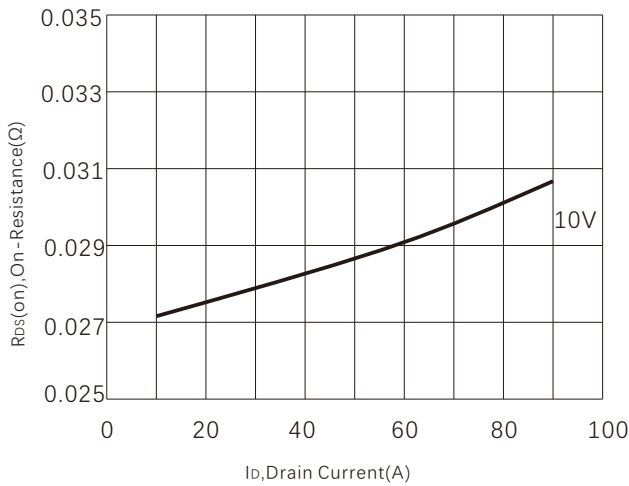


Figure 4. Capacitance

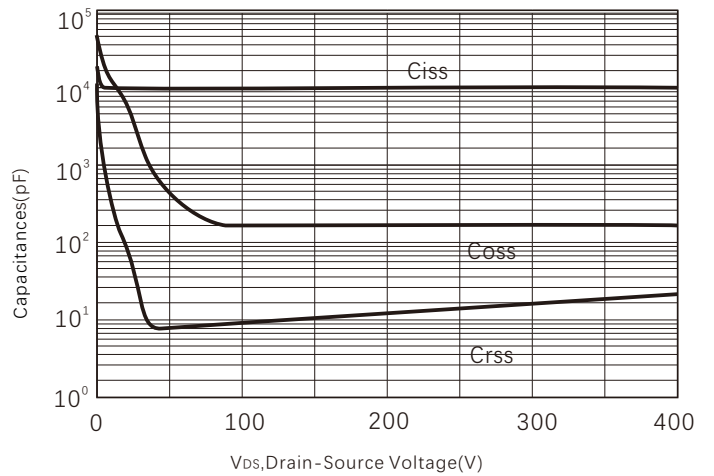


Figure 5. Gate charge

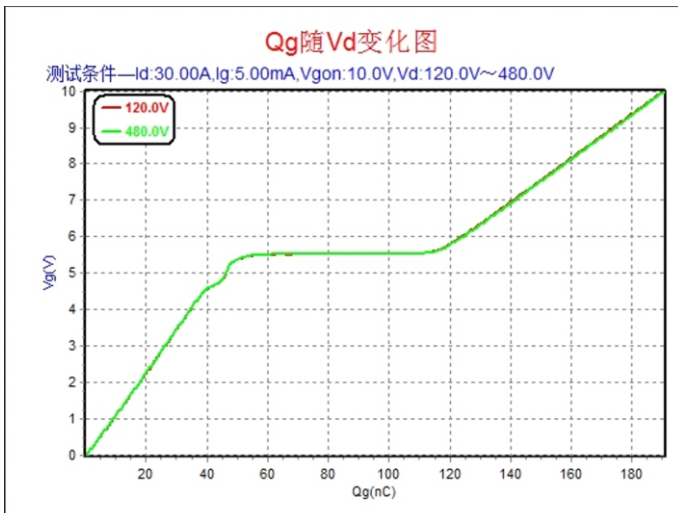


Figure 6. Source-Drain Diode Forward Voltage

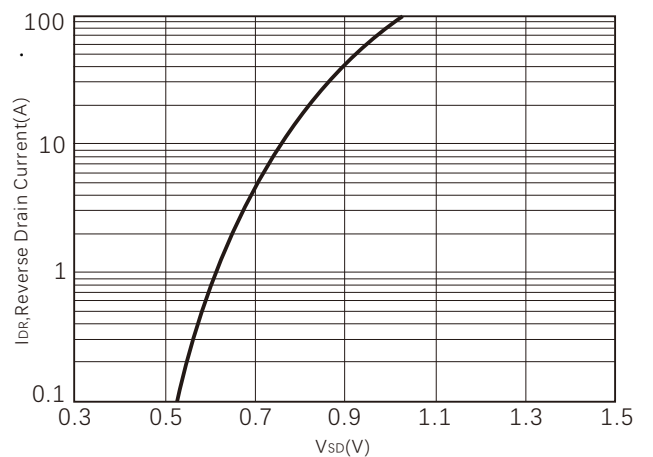


Figure 7. Normalized $R_{DS(ON)}$ vs Junction Temperature

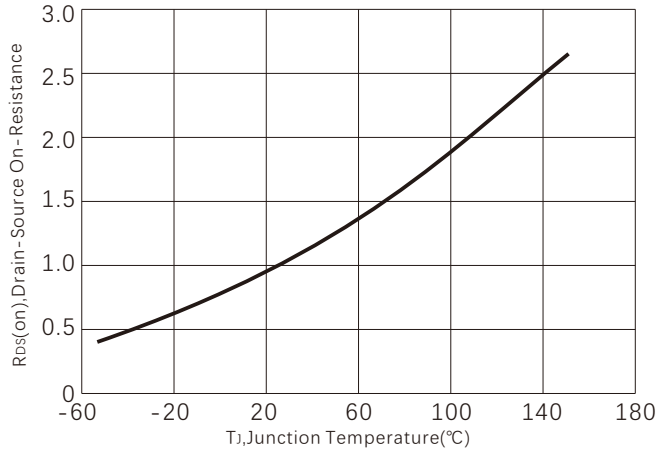


Figure 8. BV_{DSS} vs Junction Temperature

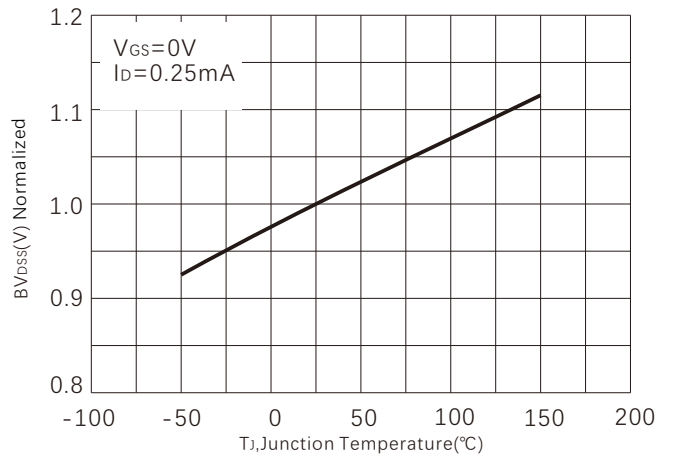


Figure 9. Safe operating area

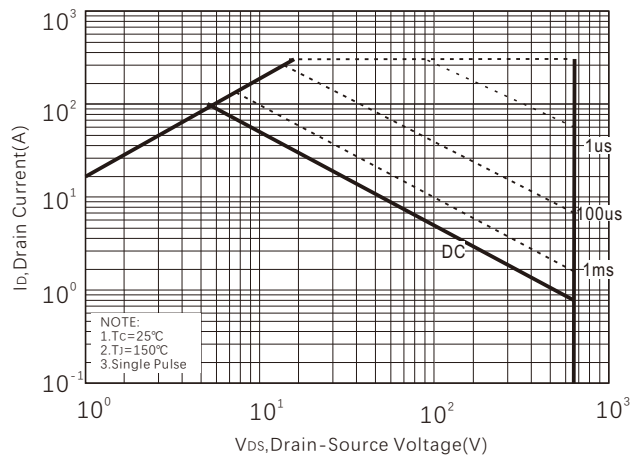


Figure 10. Power dissipation

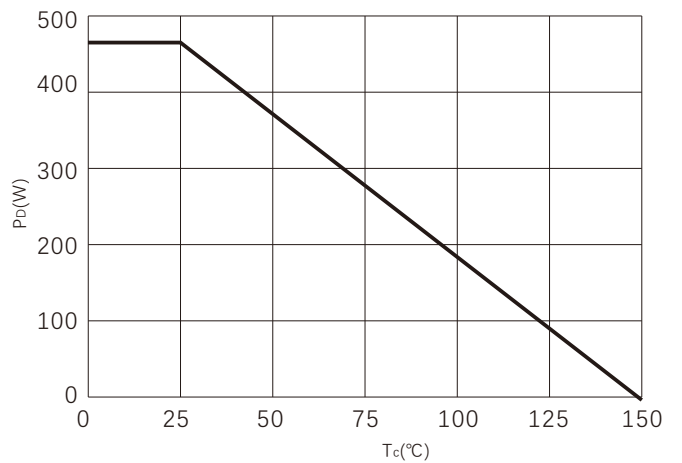
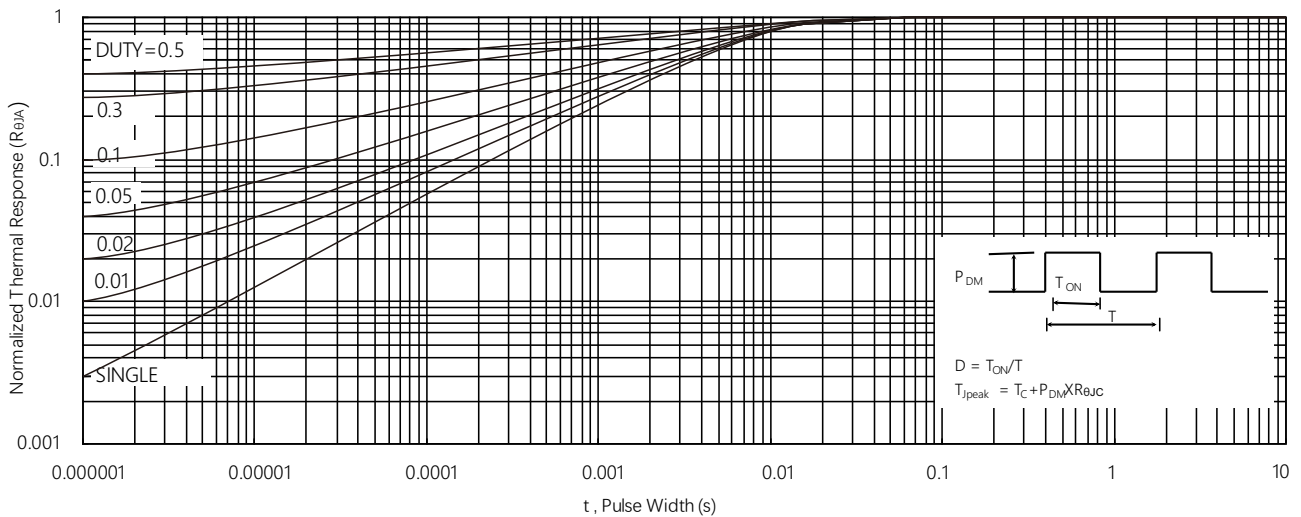
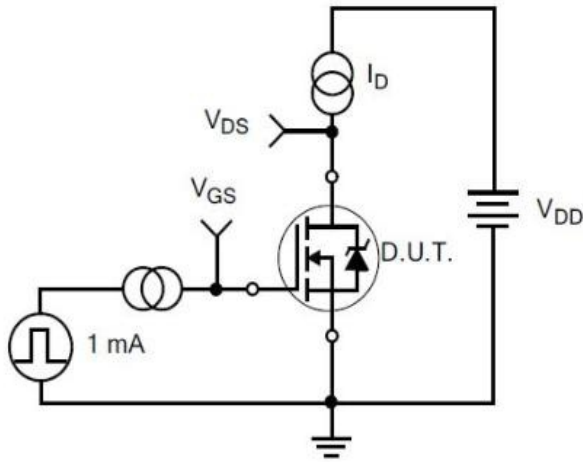


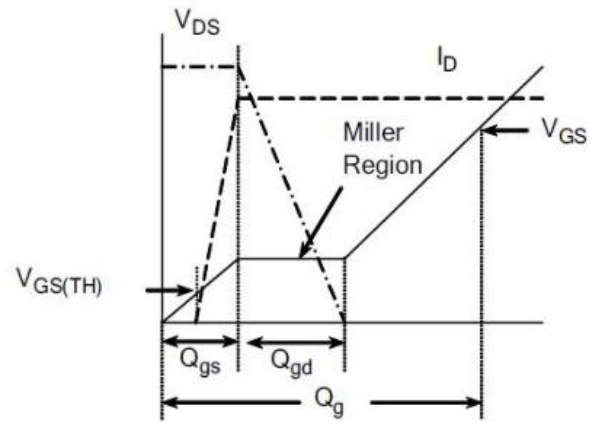
Figure 11. Normalized Maximum Transient Thermal Impedance



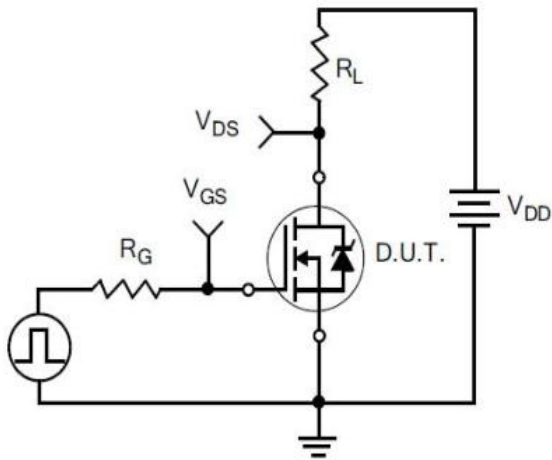
Typical Test Circuit



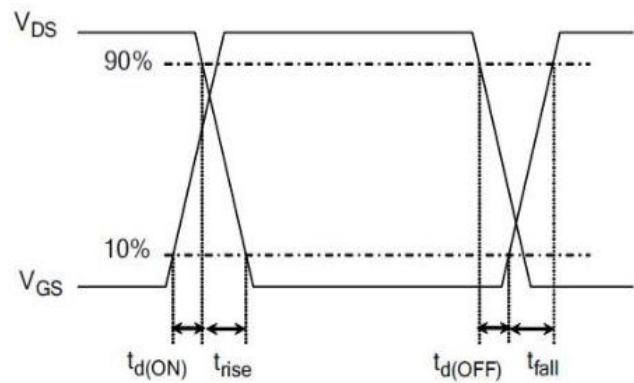
1) Gate Charge Test Circuit



2) Gate Charge Waveform

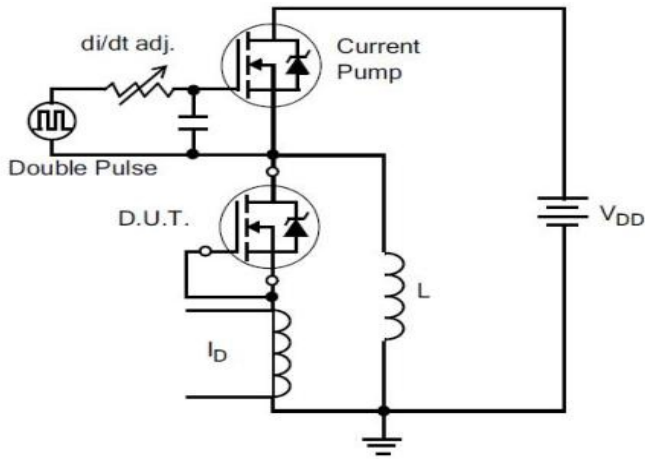


3) Resistive Switching Test Circuit

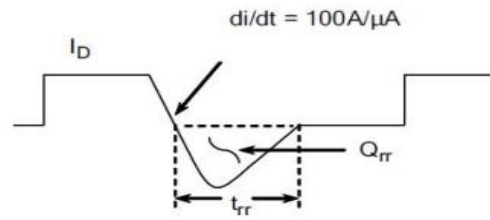


4) Resistive Switching Waveforms

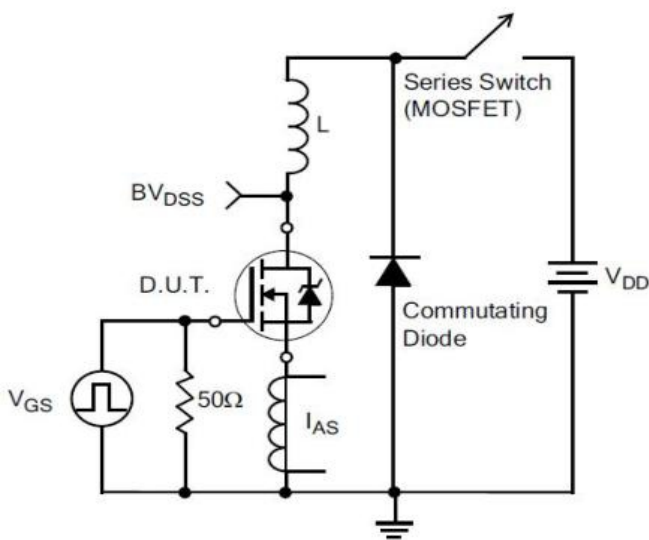
Typical Test Circuit



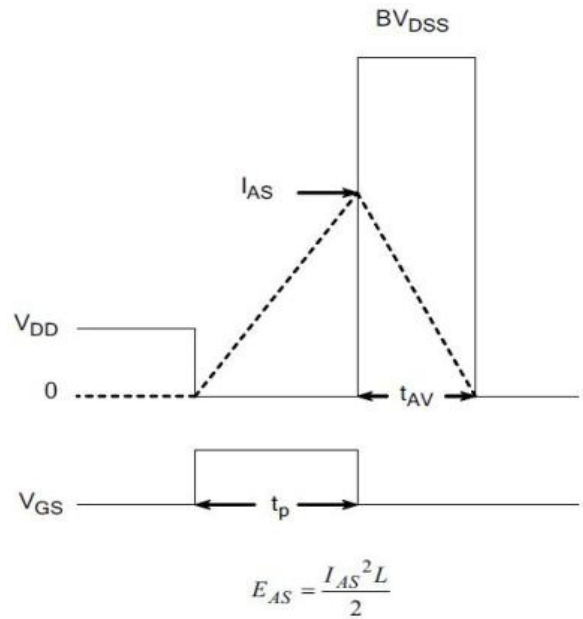
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

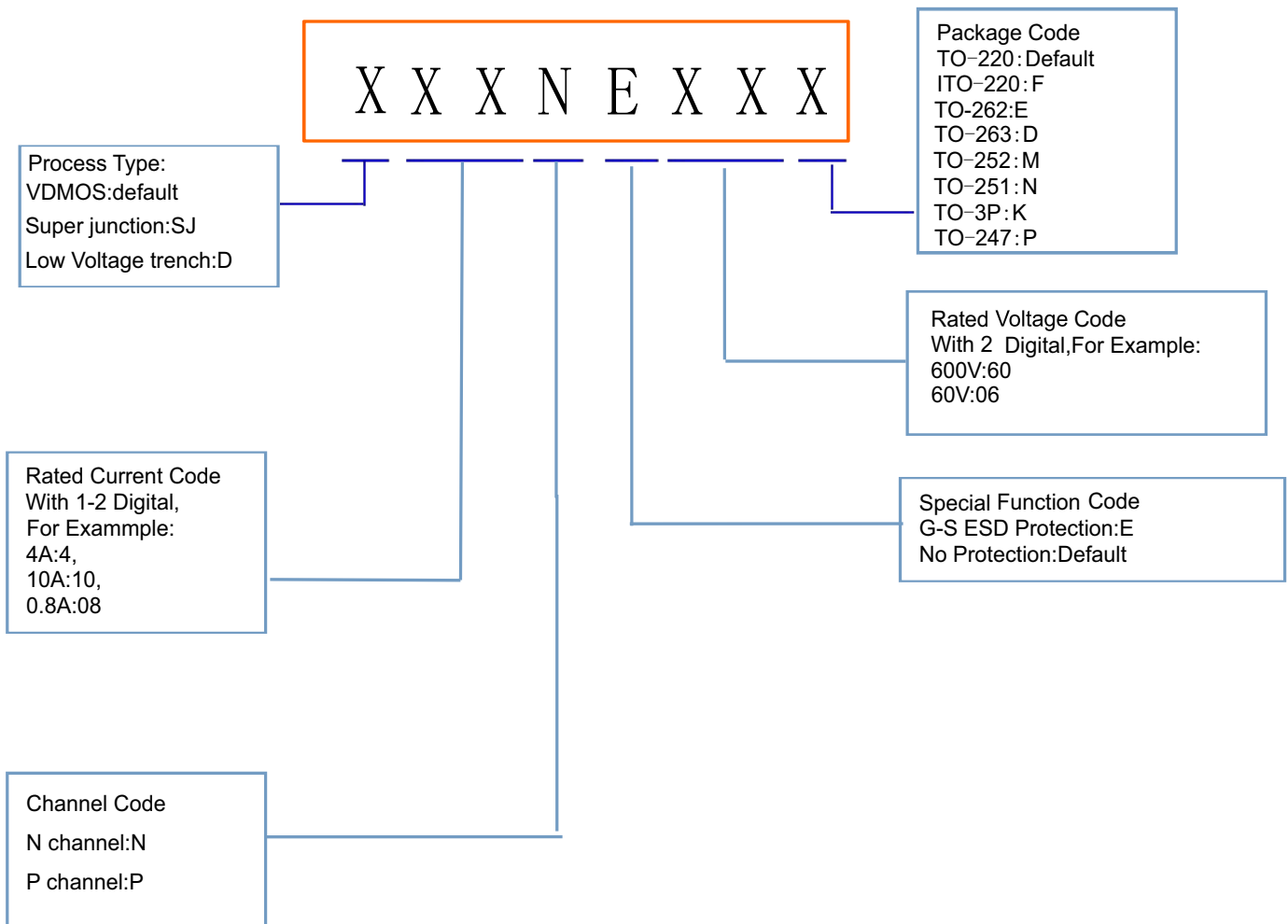


7) . Unclamped Inductive Switching Test Circuit



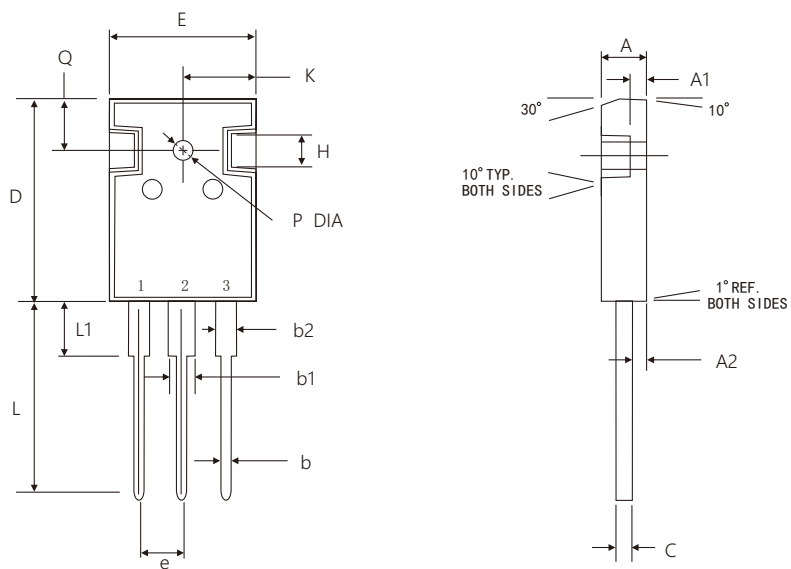
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-247 PACKAGE OUTLINE DIMENSIONS



Dimensions in millimeters

TO-247AB		
Dim	Min	Max
A	4.70	5.30
A1	1.80	2.20
A2	2.24	2.58
b	1.00	1.40
b1	2.60	3.60
b2	1.60	2.60
C	0.40	0.80
D	20.00	22.00
L	19.60	20.40
e	5.20	5.70
L1	3.80	4.50
P	3.00	3.70
Q	5.40	6.40
K	7.40	8.20
H	4.6TYP	

Friendship Reminder

- JiNan JingHeng (hereinafter referred to as JH) reserves the right to make changes to this document and its products and specifications at anytime without notice.

- Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

- JH makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does JH assume any liability for application assistance or customer product design.

- JH does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

- No license is granted by implication or otherwise under any intellectual property rights of JH.

- JH's products are not authorized for use as critical components in life support devices or systems without express written approval of JH.