SEMICONDUCTOR

SJ7N65M
650V SUPER-JUNCTION Power MOSFET

GENERAL DESCRIPTION

The series of devices use advanced trench gate super junction technology and design to provide excellent FOM(RDS(ON) ×Qg),Extremely low switching and conduction losses make switching applications even more efficient, more compact,lighter and cooler.

PRODUCT SUMMARY

V_{DS}(V)	$R_{DS(ON)}$(Ω)Typ	I_D(A)
650	0.85@V_{GS}=10V	7

FEATURE

- Low on-resistance and low conduction losses
- Ultra Low Gate Charge cause lower driving requirements
- 100% avalanche tested
- RoHS compliant

TO-252
SJ7N65M

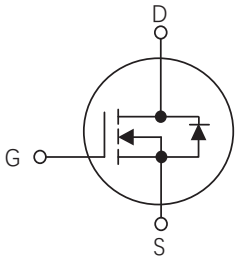
MECHANICAL DATA

- Case:TO-252

Pin Definition:

1. Gate
2. Drain
3. Source

Block Diagram



APPLICATION

Used in PFC,hard switching,and resonant switching circuits。For e.g, PC Silverbox, Adapter, LCD&PDP TV, Lighting,Server,Telecom and UPS。

ORDERING INFORMATION

Part No.	PackageType	Package	Quality (box)
SJ7N65M	TO-252	Tape & Reel	2500

ABSOLUTE MAXIMUM RATINGS (T_C=25℃, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	7	A
Pulsed Drain Current (Note1)	I_{DM}	28	A
Avalanche Energy (Note 2)	E_{AS}	86	mJ
Power Dissipation	P_D	62.5	W
Junction Temperature	T_J	+150	C
Storage Temperature	T_{STG}	-55 ~ + 150	C

THERMAL DATA

Parameter	Symbol	Rating	Unit
Junction to Ambient	$R_{\theta JA}$	60	℃/W
Junction to Case	$R_{\theta JC}$	2.0	℃/W

ELECTRICAL CHARACTERISTICS (T_C=25℃ unless otherwise specified)

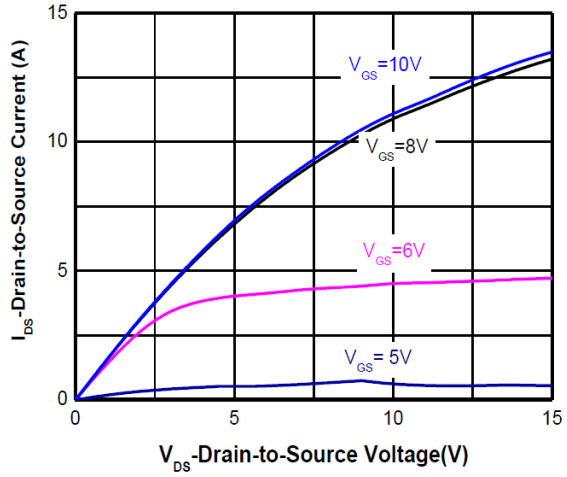
Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250uA	650			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V ,V_{DS}=0V			100	nA
	Reverse		V_{GS}= -30V ,V_{DS}=0V			-100	nA
ON CHARACTERISTICS(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.5		4.5	V
Drain source on resistance		$R_{DS(ON)}$	V_{GS}=10V ,I_D=3.5A		0.85	0.95	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		Ciss	V_{DD}=25V, V_{GS}= 0V, f= 1MHz		332		pF
Output Capacitance		Coss			373		pF
Reverse Transfer Capacitance		Crss			10		pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		$t_{D(ON)}$	V_{DD}=400V ,I_D=3.5A,R_G=20Ω		25		ns
Turn-On Rise Time		t_R			55		ns
Turn-Off Delay Time		$t_{D(OFF)}$			110		ns
Turn-Off Fall Time		t_F			9		ns
Total Gate Charge		Q_G	V_{DS}=400V ,I_D=3.5A V_{GS}=10V		9.2		nC
Gate-Source Charge		Q_{GS}			2.2		nC
Gate-Drain Charge		Q_{GD}			4.2		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=7A		0.9	1.5	V
Maximum Continuous Drain-Source Diode Forward Current		I_S			7		A
Reverse Recovery Current		I_{RRM}	V_{GS}=0V,I_S=3.5A dI$_F$/dt=100A/μS(Note 1)		18		A
Reverse Recovery Time		t_{rr}			190		ns
Reverse Recovery Charge		Q_{RR}			2.3		μC

Note:1. Repetitive Rating : Pulse width limited by maximum junction temperature

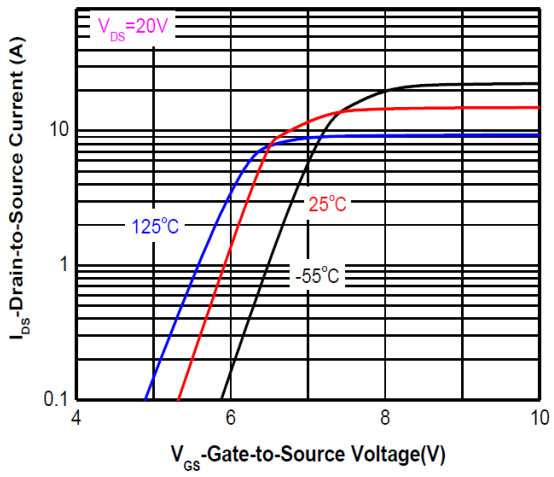
2.L=60mH,I_{AS}=1.7A,V_{DD}=150V,Starting T_J=25℃

3. Pulse Test:Pulse width ≤300μS,Duty cycle≤1%

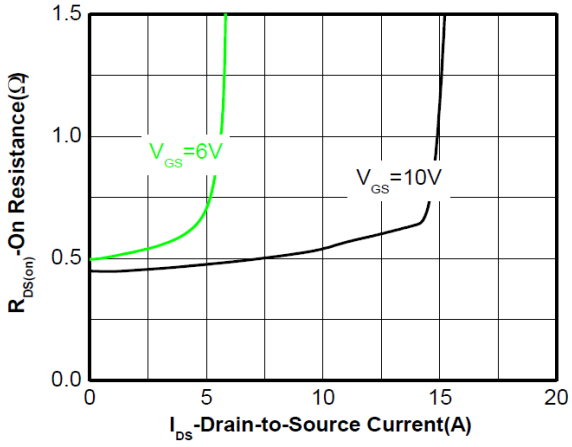
Typical characteristics Diagrams



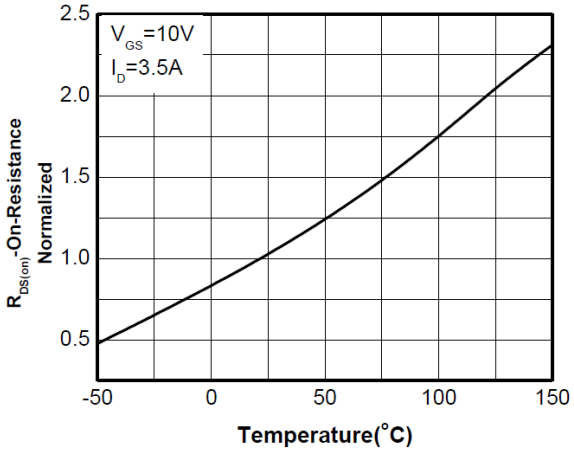
Output characteristics



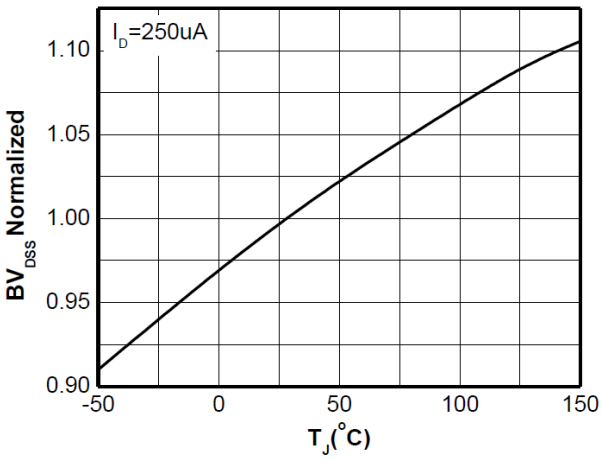
Transfer characteristics



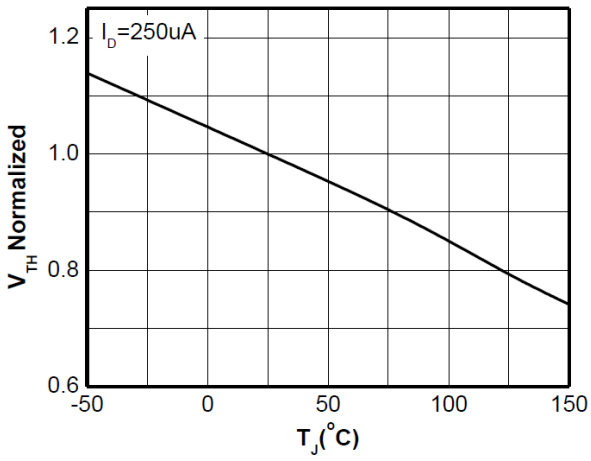
On-Resistance vs. Drain current



On-Resistance vs. Junction temperature

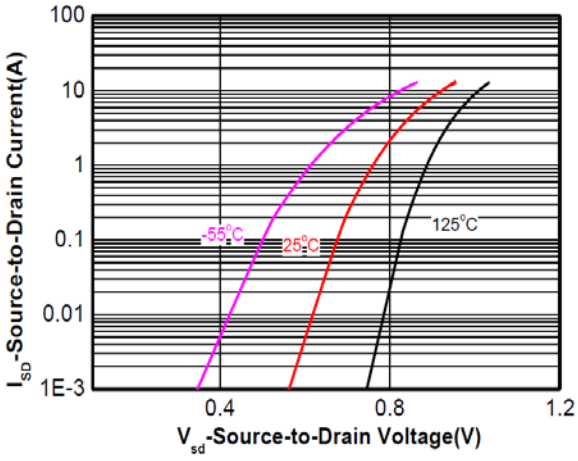


Breakdown Voltage vs. Junction temperature

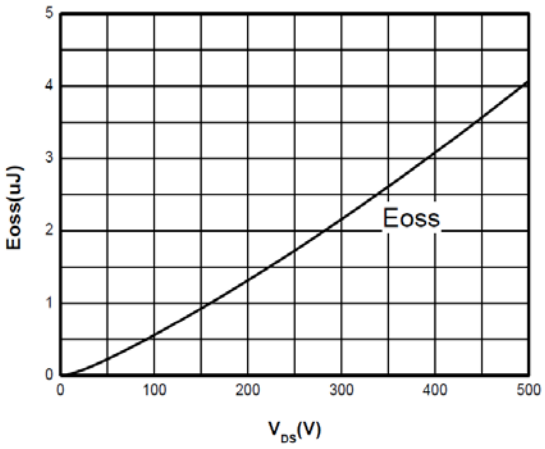


Threshold voltage vs. Junction temperature

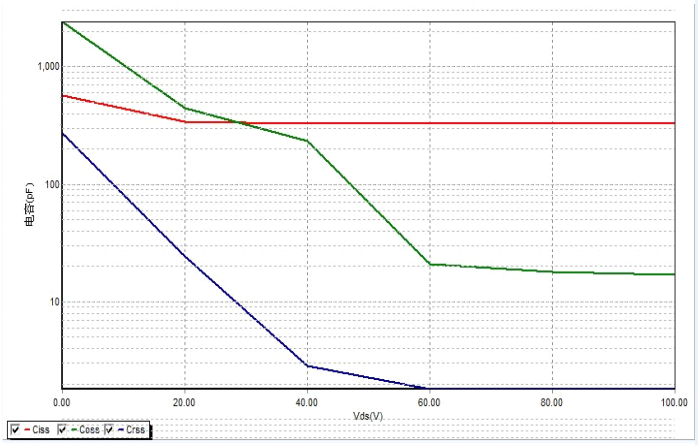
Typical characteristics Diagrams



Body diode forward voltage

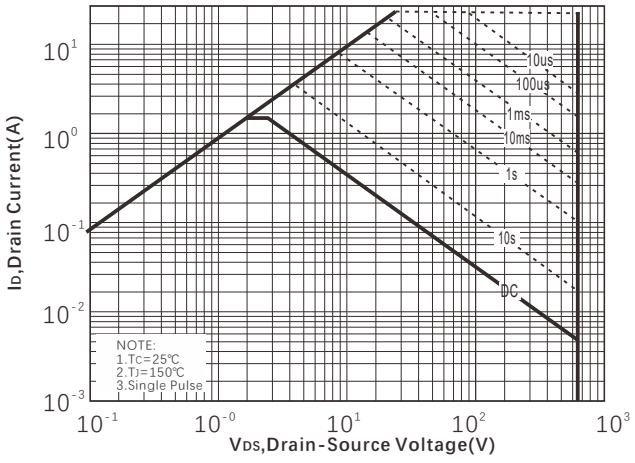


Coss stored Energy

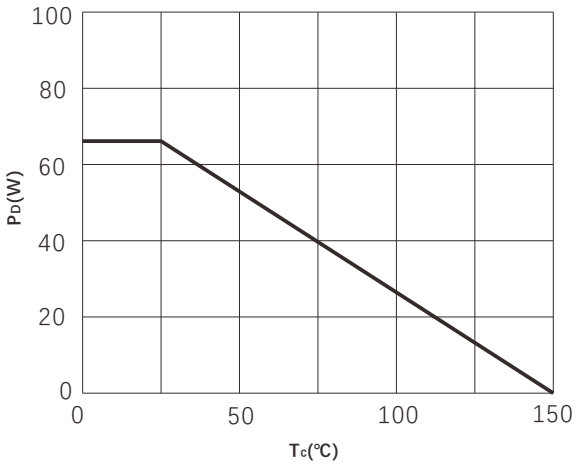


Capacitance

Gate charge Characteristics

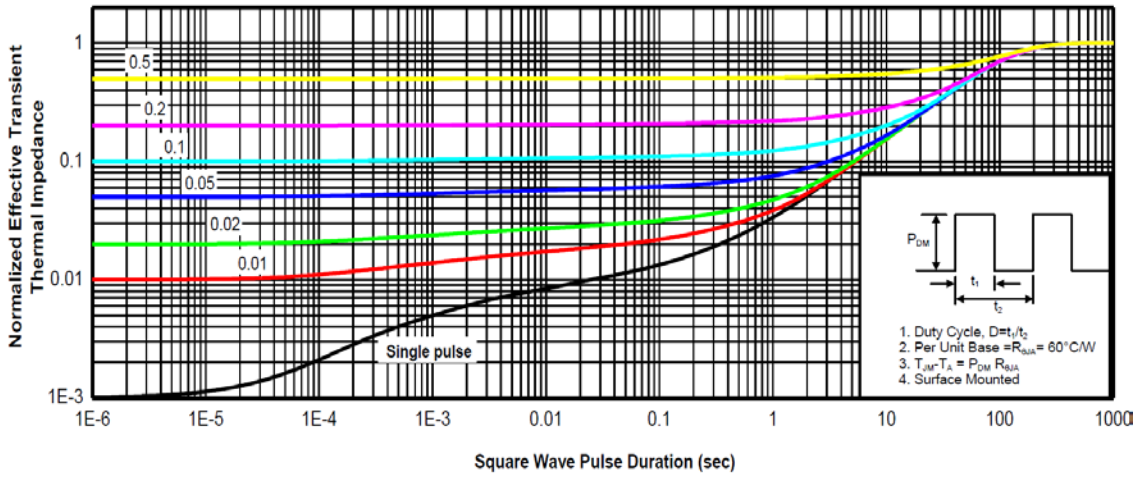


Safe operating area



Power dissipation

Typical characteristics Diagrams



Transient thermal response (Junction-to-Ambient)

TYPICAL TEST CIRCUIT

Table 20 Switching times test circuit and waveform for inductive load

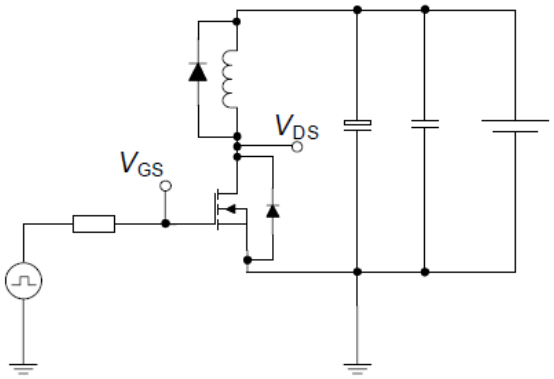
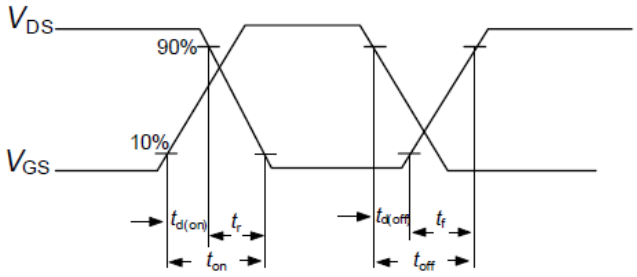
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

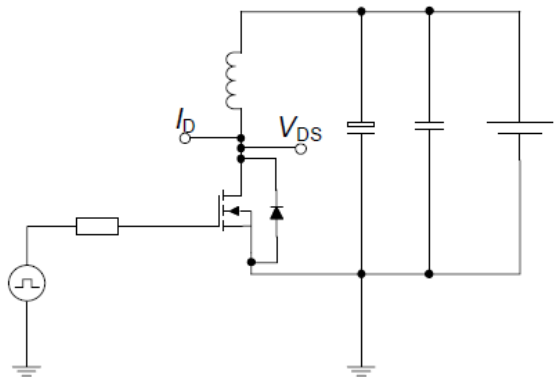
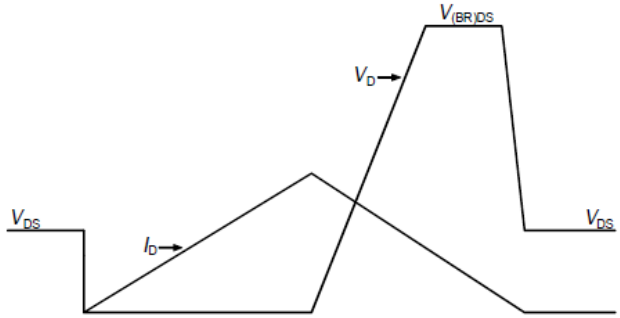
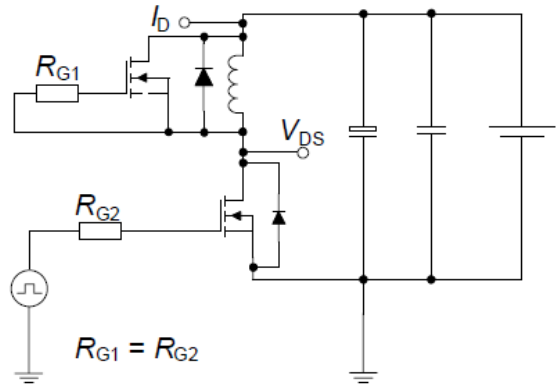
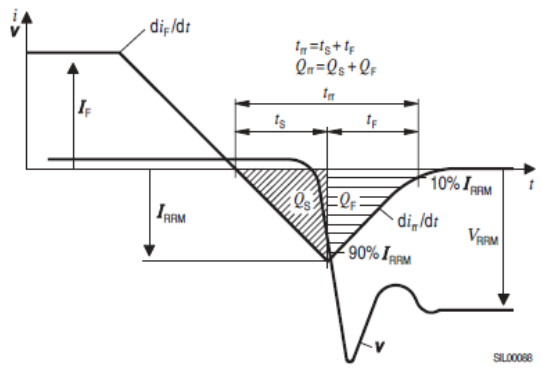
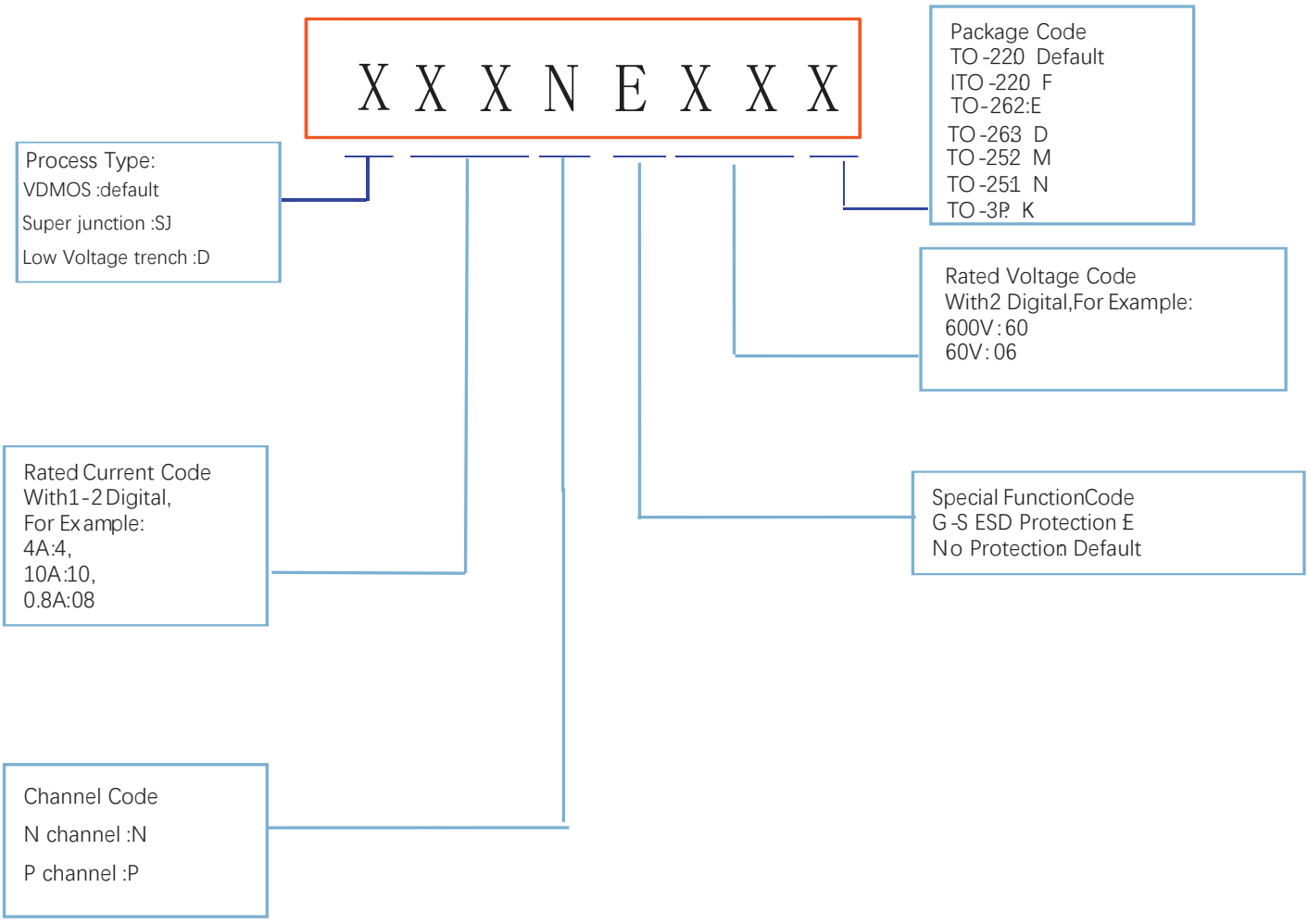
Unclamped inductive load test circuit	Unclamped inductive waveform
	

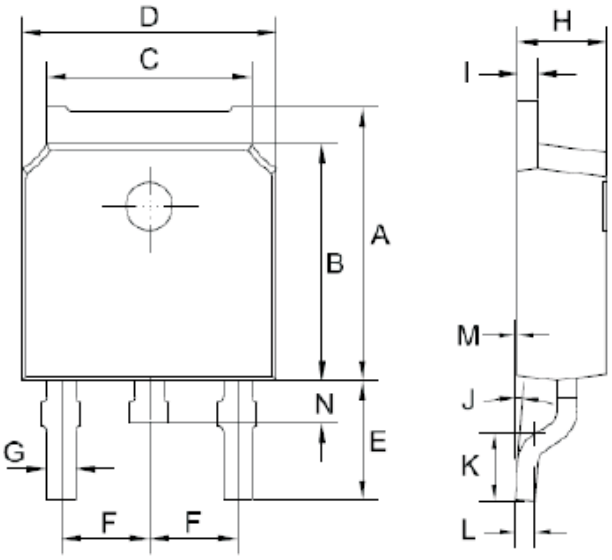
Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
	

Product Names Rules



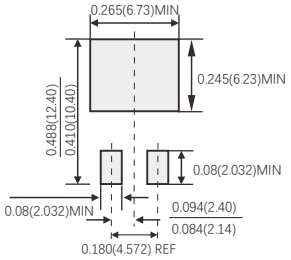
TO-252 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	2.6	3.3	0.102	0.130
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0	8	0	8
K	1.45	1.85	0.057	0.073
L	0.41	0.61	0.016	0.024
M	0	0.12	0.000	0.005
N	0.6	1	0.024	0.039

Suggested Pad Layout

(TO-252)



(设计者可参考推荐值根据焊接工艺
要求自行确定适合的焊盘尺寸)
(Designers can refer to the recommended
values according to the manufacturing process
requirements to determine the appropriate pad size)

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