

General Description

These N-channel enhancement mode power mosfets Used advanced splite gate trench technology design, provided excellent Rdson and low gate charge. Which accords with the RoHS standard.

Features

- Fast switching
- Low on-resistance
- Low gate charge and input capacitance
- 100% avalanche tested
- AEC-Q101 qualified and PPAP capable

Mechanical Data

- Case: TO-252 Package

Application

- Power switching applications
- DC-DC Converters
- Full bridge control

Ordering Information

Part No.	Package Type	Package	Quality(box)
D240N06M-V	TO-252	Tape & Reel	3000



AEC-Q101 Qualified

Product Summary			
V _{DS}	R _{DS(on)} (mΩ) Typ	I _D (A)	Q _g (Typ)
60V	3.2 @ 10V	240	61nc

TO-252
D240N06M-V



Block Diagram

Pin Definition:

1. Gate
2. Drain
- 3/4/5/6/7. Source

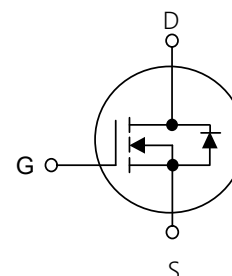


Table1 Absolute Maximum Ratings (T_c=25°C, unless otherwise specified)

Parameter	Symbol	D240N06M-V	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _c =25°C 240*	A
		T _c =100°C 166*	
Pulsed Drain Current (Note 1)	I _{DM}	960	A
Single Pulse Avalanche Energy(Note 2)	E _{AS}	1045	mJ
Power Dissipation T _c =25°C	P _D	277	W
Operating Junction and Storage Temperature	T _J /T _{STG}	-55~+175	°C

※ limited by maximum junction temperature

Table 2. Thermal Characteristics

Parameter	Symbol	D240N06M	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	50	$^{\circ}\text{C/W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	0.54	$^{\circ}\text{C/W}$

Table 3. Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V,I _D =250μA	60	-	-	V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =20V,V _{DS} =0V	-	-	100	nA
	Reverse		V _{GS} = -20V,V _{DS} =0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} ,I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V,I _D =90A	-	3.2	3.5	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C _{ISS}	V _{DS} =30V,V _{GS} =0V,f=1MHz	-	3791	-	pF
Output Capacitance		C _{OSS}		-	1698	-	pF
Reverse Transfer Capacitance		C _{RSS}		-	56.7	-	pF
Gate Resisitance		R _G	V _{DD} =0V,V _{GS} =0V,f=1MHz	-	1.8	-	Ω
Switching Characteristics (Note 4)							
Turn-on Delay Time		t _d (on)	V _{DD} =30V,I _D =90A V _{GS} =10V,R _{GEN} =1.6Ω,	-	17.6	-	ns
Turn-on Rise Time		t _r		-	102.3	-	ns
Turn-off Delay Time		t _d (off)		-	33	-	ns
Turn-off Fall Time		t _f		-	106.9	-	ns
Total Gate Charge		Q _G	V _{DD} =30V,I _D =90A, V _{GS} =10V	-	61	-	nC
Gate-Source Charge		Q _{GS}		-	25.5	-	nC
Gate-Drain Charge		Q _{GD}		-	12.9	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _S =95A	-	-	1.2	V
Maximum Continuous Drain-Source Diode Forward Current		I _S		-	-	120	A
Reverse Recovery Time		t _{rr}	V _{GS} =0V, I _F =60A	-	42.4	-	ns
Reverse Recovery Charge		Q _{RR}	dI _F /dt=110A/μs (Note 1)	-	29.7	-	nC

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature

2 $L=0.5\text{mH}$, $I_D=65A$, $V_{DD}=50V$, $V_{GATE}=10V$, Starting $T_J=25^{\circ}\text{C}$

3 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

4 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

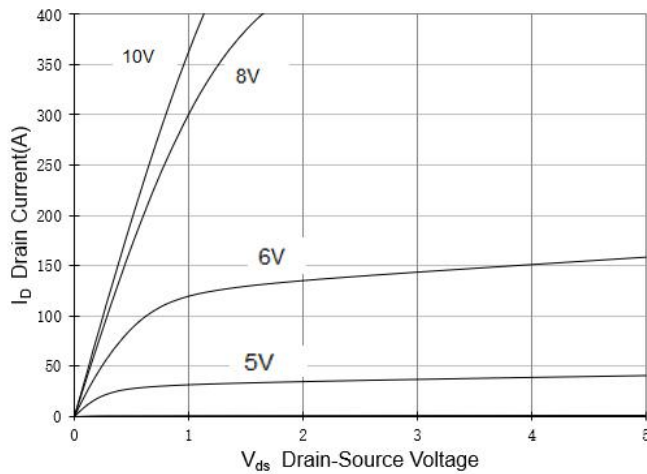


Figure 1 Output Characteristics

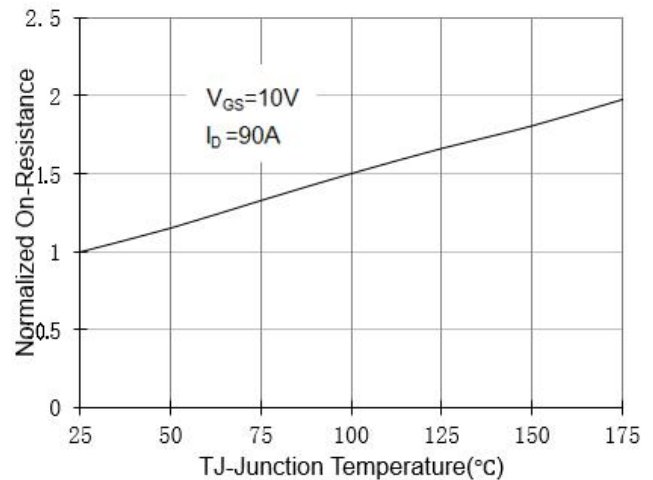


Figure 2 $R_{DS(on)}$ -Junction Temperature

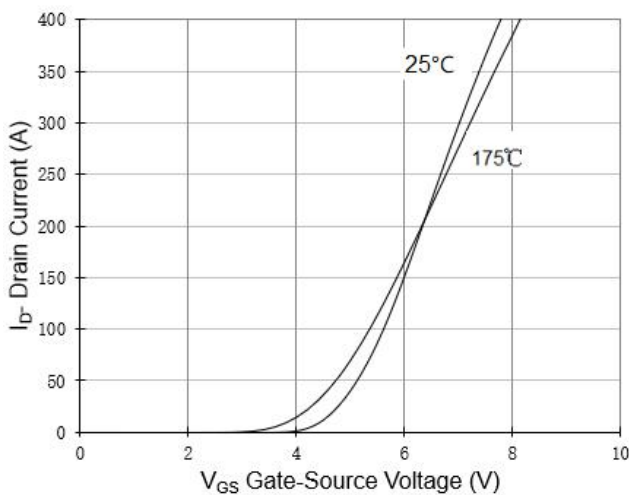


Figure 3 Transfer Characteristics

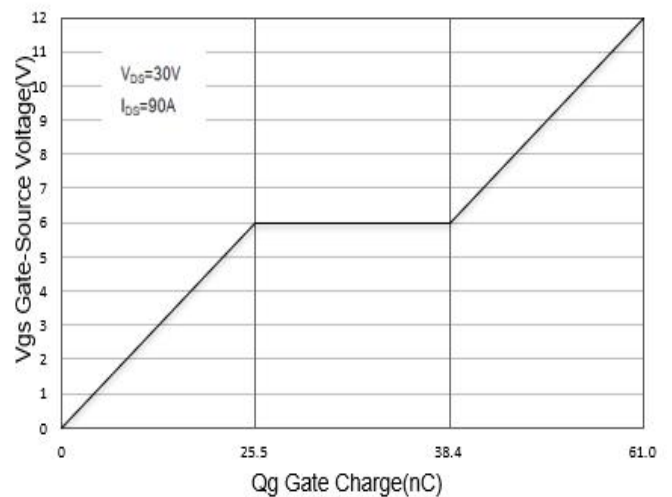


Figure 4 Gate Charge

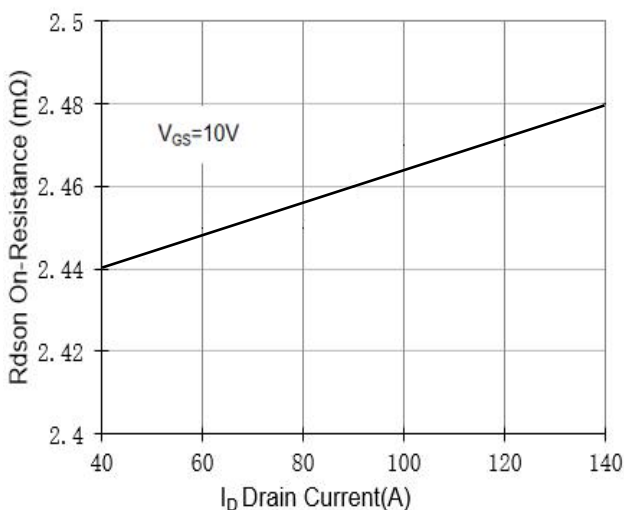


Figure 5 $R_{DS(on)}$ -Drain Current

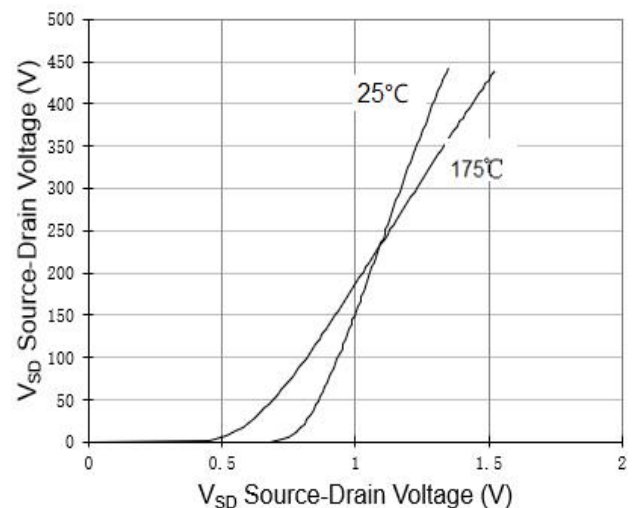


Figure 6 Source-Drain Diode Forward

Typical Characteristics Diagrams

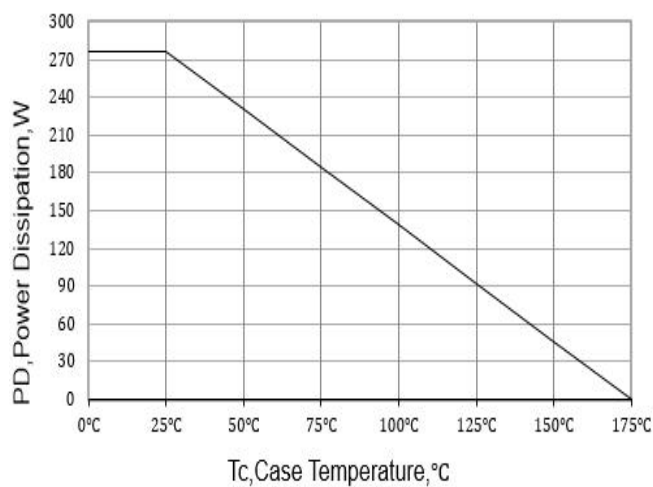


Figure 7 Power De-rating

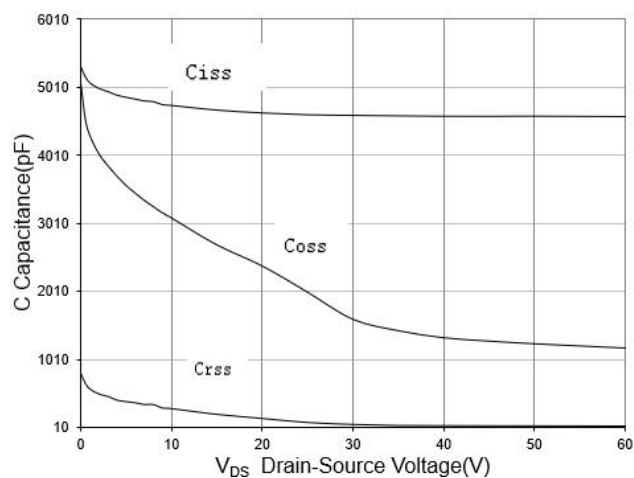


Figure 8 Capacitance vs Vds

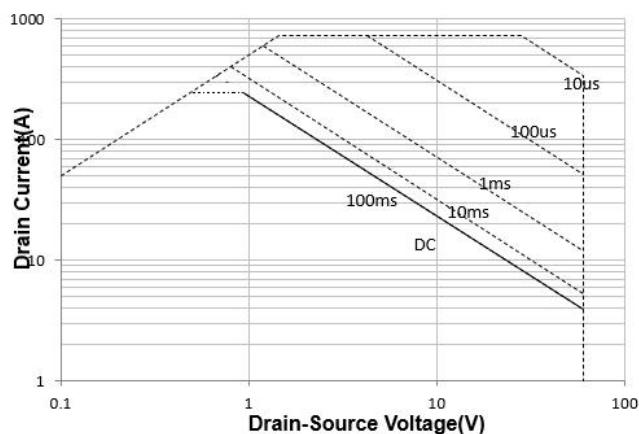


Figure 9 Safe Operation Area

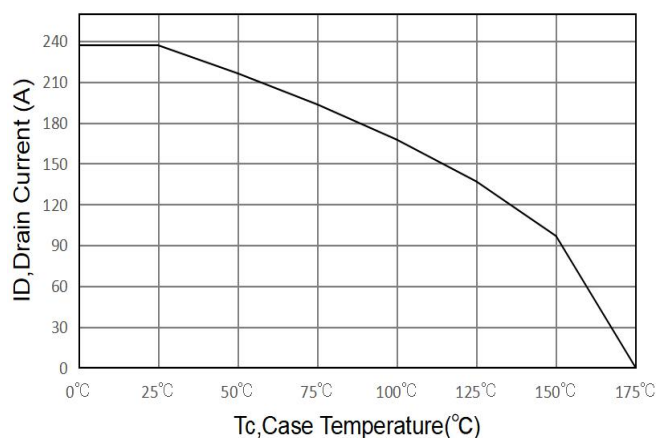


Figure 10 Current De-rating

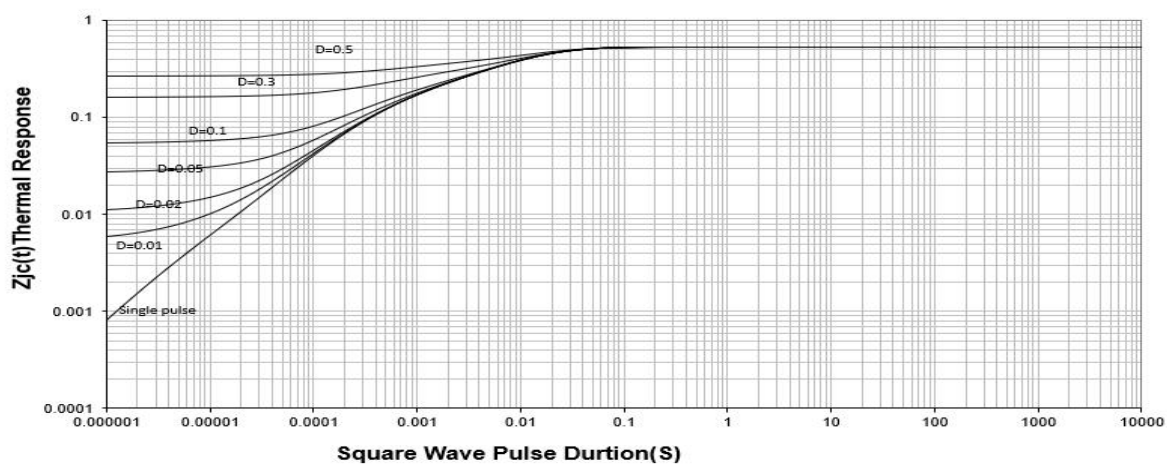
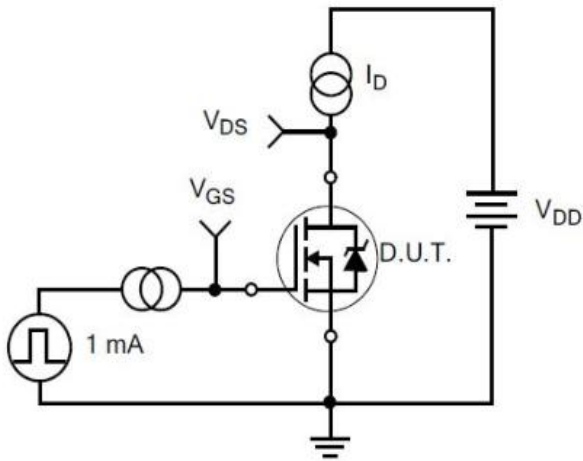
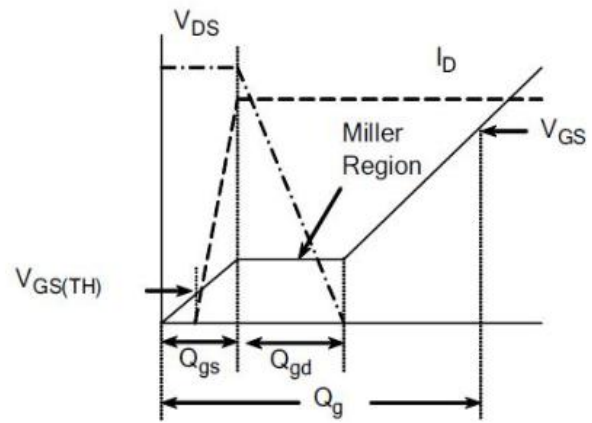


Figure 11 Maximum Transient Thermal Impedance

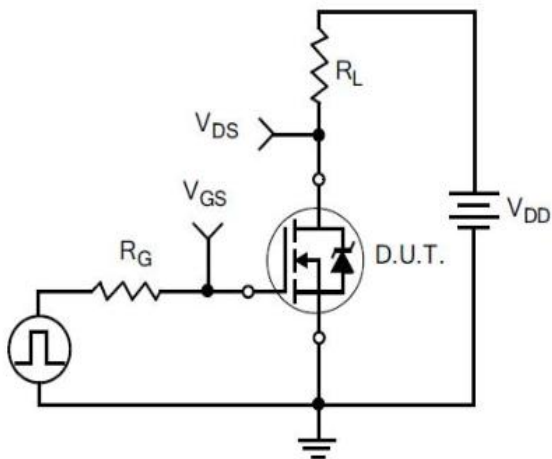
Typical Test Circuit



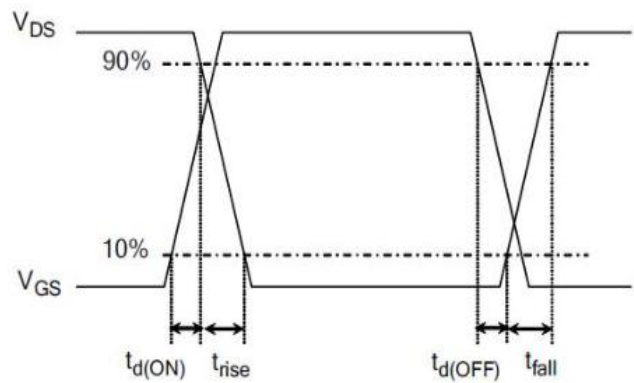
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

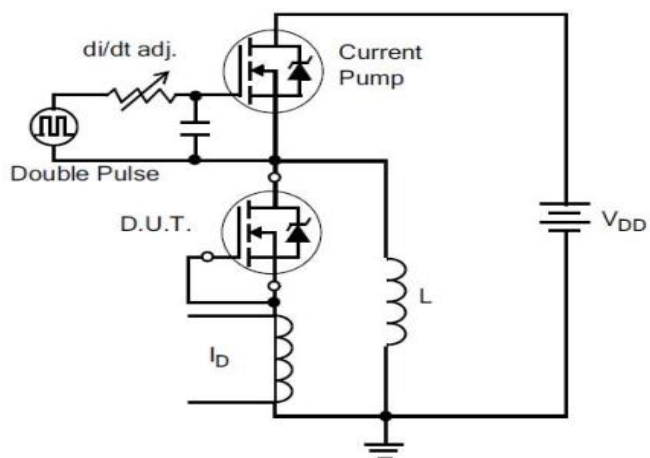


3) Resistive Switching Test Circuit

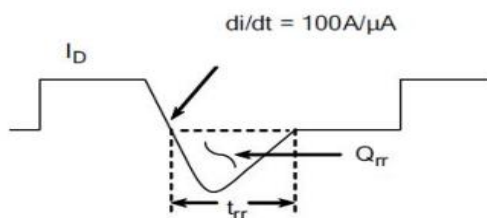


4) Resistive Switching Waveforms

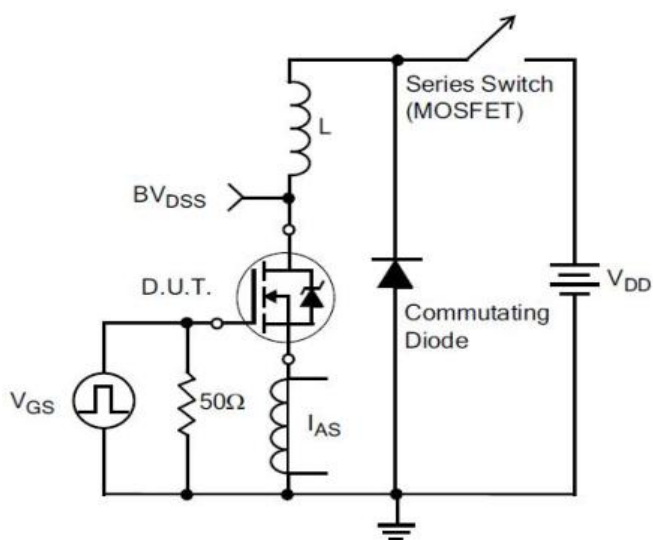
Typical Test Circuit



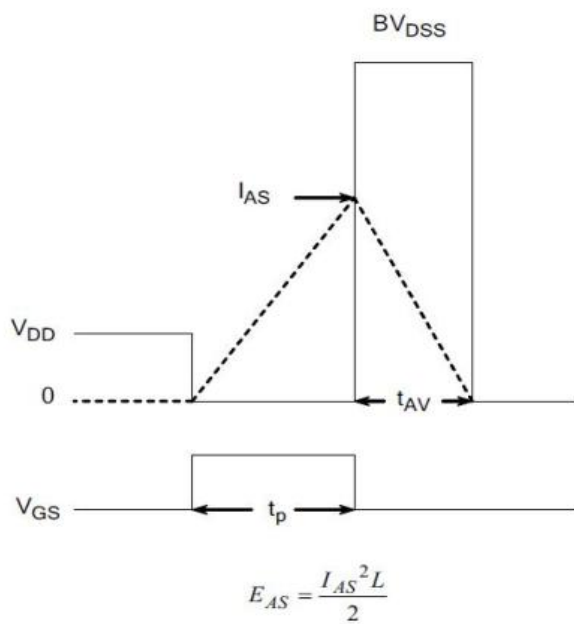
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

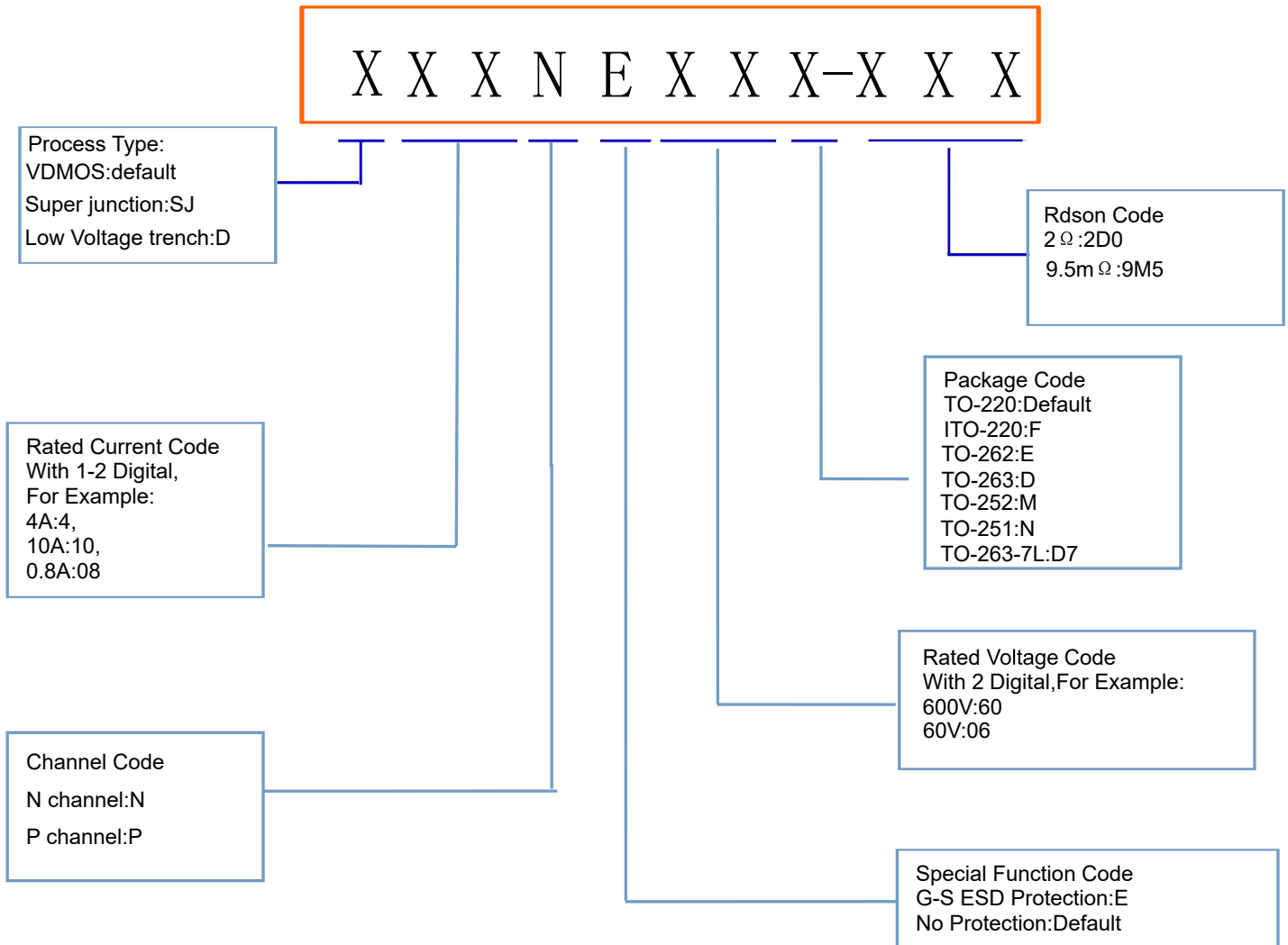


7) . Unclamped Inductive Switching Test Circuit



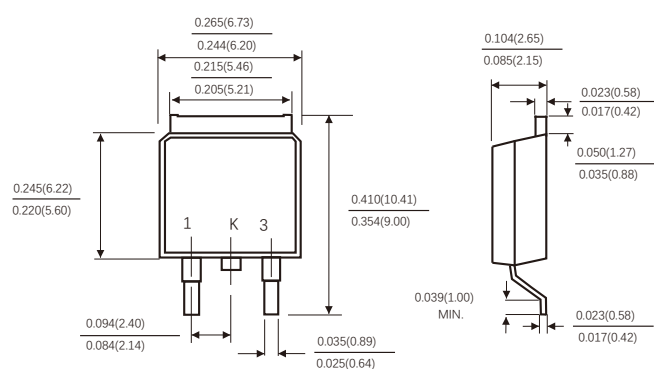
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-252 PACKAGE OUTLINE DIMENSIONS



Dimensions in inches and (millimeters)

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