

### Features

- 100% EAS Guaranteed
- Low  $R_{DS(ON)}$
- Low Gate Charge
- RoHs and Halogen-Free Compliant

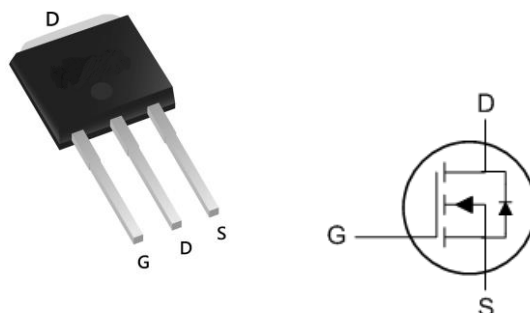
### Product Summary

BVDSS	$R_{DS(ON)}$	ID
100V	8.5m $\Omega$	75A

### Description

The D75N10N is the high cell density trenched N-ch MOSFETs, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the Synchronous Rectification for AC/DC Quick Charger.

### TO-251 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current <sup>1</sup>	75	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current <sup>1</sup>	46	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	290	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	61	mJ
$I_{AS}$	Avalanche Current	35	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	108	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10s$ )	---	25	$^\circ C/W$
	Thermal Resistance Junction-Ambient <sup>1</sup>	---	55	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	1.15	$^\circ C/W$

Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=13.5A$	---	6.6	8.5	m $\Omega$
	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=4.5V, I_D=11.5A$	---	8.7	11	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.3	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=20A$	---	85	---	S
$Q_g$	Total Gate Charge (10V)	$V_{DS}=50V, V_{GS}=10V, I_D=13.5A$	---	45	---	nC
$Q_g$	Total Gate Charge (4.5V)		---	19.3	---	
$Q_{gs}$	Gate-Source Charge		---	9.5	---	
$Q_{gd}$	Gate-Drain Charge		---	4.8	---	
$T_d(on)$	Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3\Omega, I_D=13.5A$	---	10	---	ns
$T_r$	Rise Time		---	6.5	---	
$T_d(off)$	Turn-Off Delay Time		---	45	---	
$T_f$	Fall Time		---	7.5	---	
$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V, f=1\text{MHz}$	---	3320	---	$\mu F$
$C_{oss}$	Output Capacitance		---	605	---	
$C_{rss}$	Reverse Transfer Capacitance		---	20	---	
<b>Diode Characteristics</b>						
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	48	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.1	V
$t_{rr}$	Reverse Recovery Time	$I_F=13.5A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	33	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	150	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.3mH, I_{AS}=35A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_S$  , in real applications , should be limited by total power dissipation.

Typical Characteristics

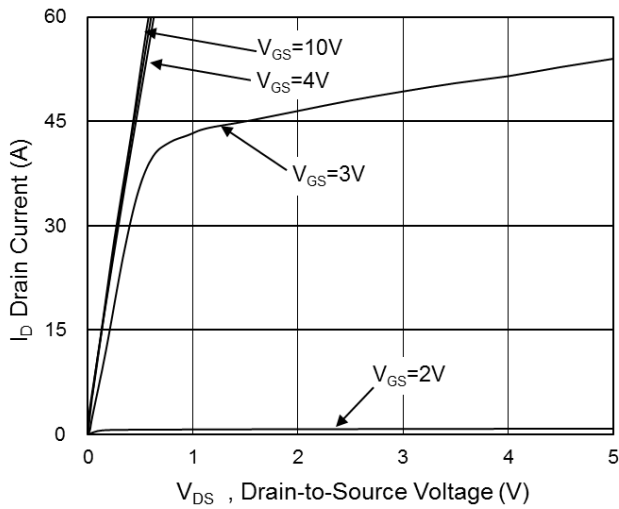


Fig.1 Typical Output Characteristics

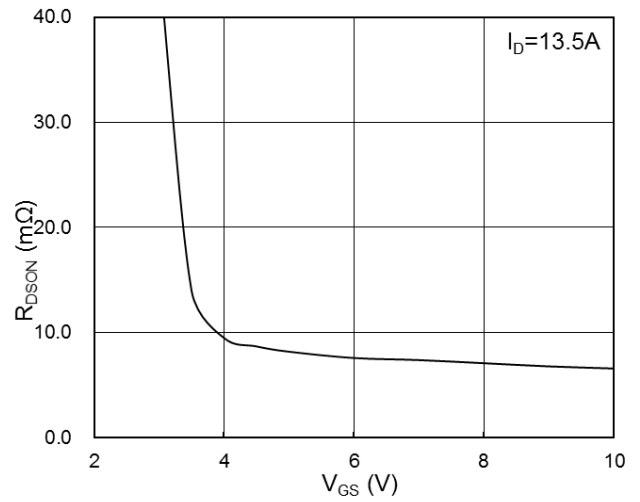


Fig.2 On-Resistance vs G-S Voltage

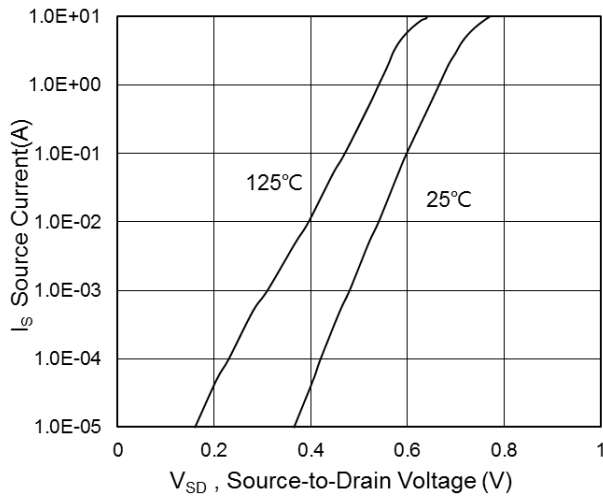


Fig.3 Source-Drain Forward Characteristics

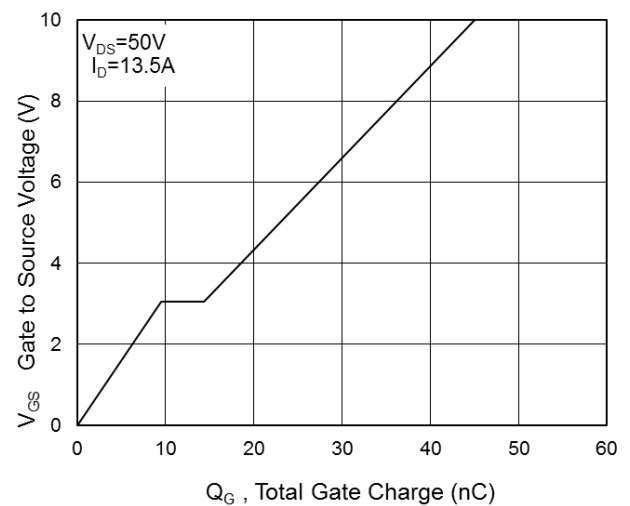


Fig.4 Gate-Charge Characteristics

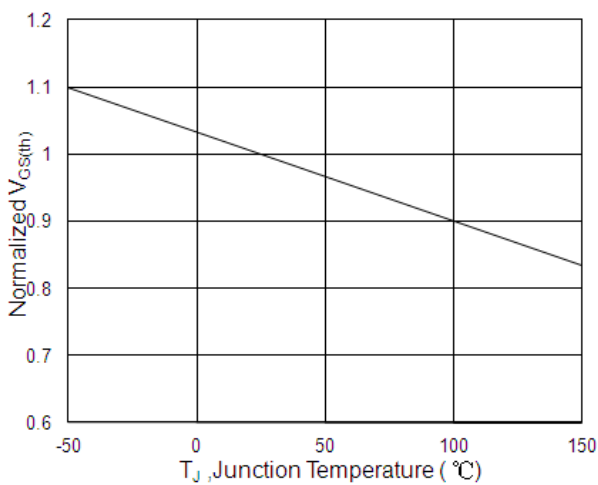


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

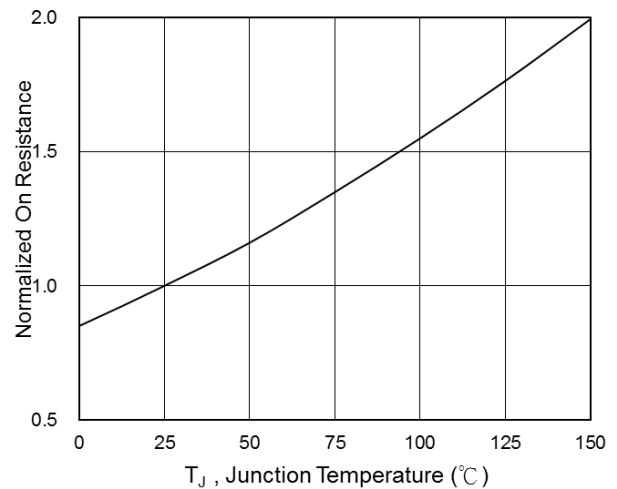
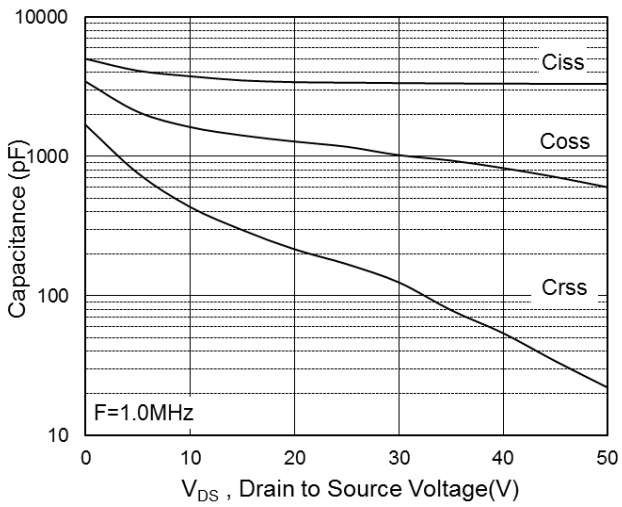
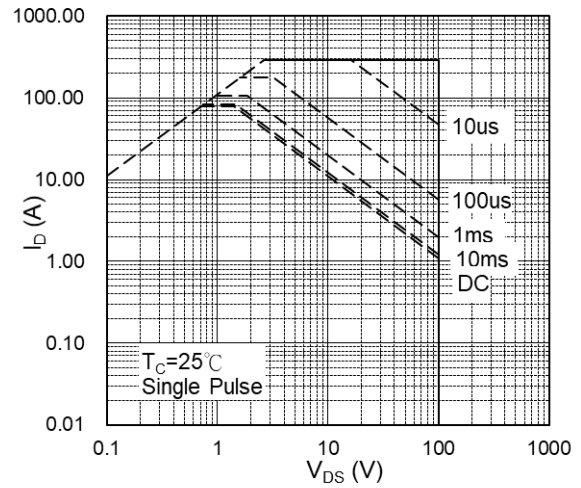


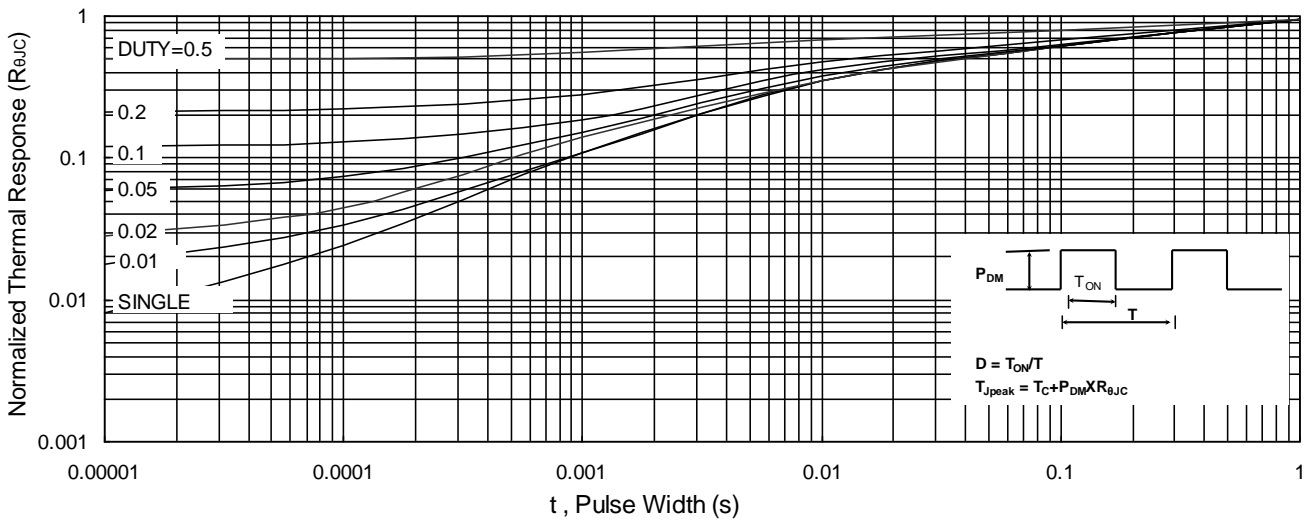
Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$



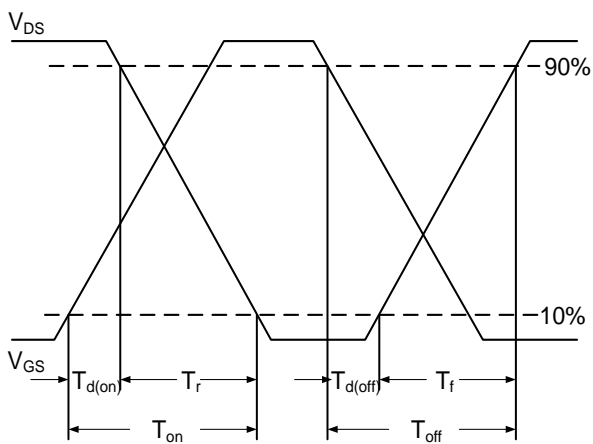
**Fig.7 Capacitance**



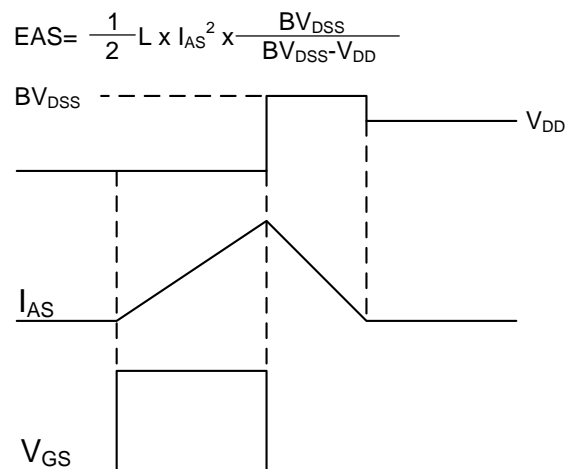
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

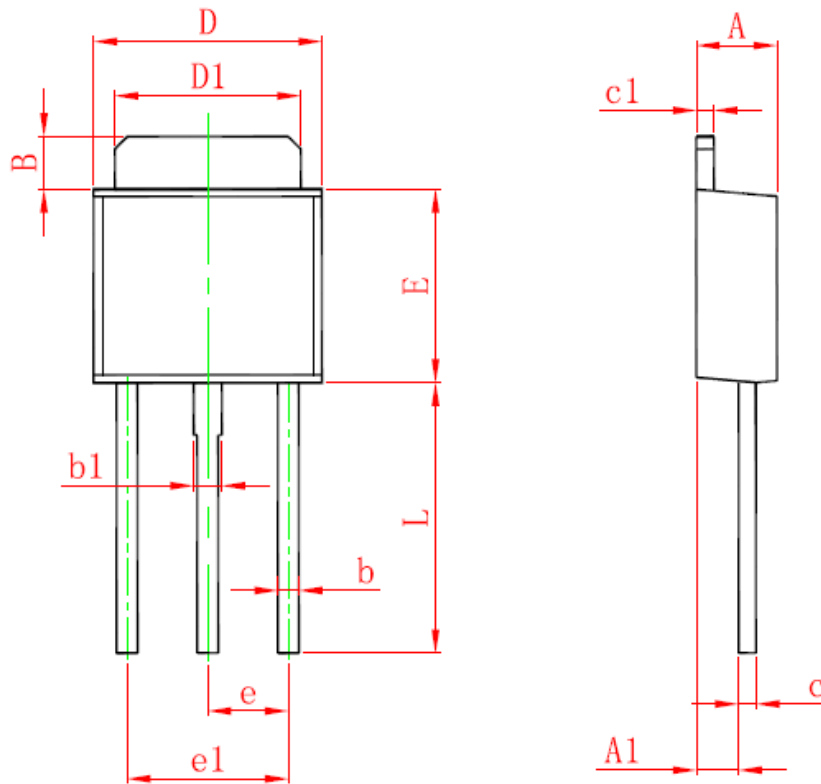


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

# TO-251 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
A1	0.95	1.35	0.037	0.054
B	0.85	1.65	0.033	0.065
b	0.50	0.90	0.020	0.035
b1	0.60	1.10	0.023	0.043
c	0.43	0.61	0.017	0.024
c1	0.43	0.85	0.017	0.033
D	6.35	6.73	0.250	0.265
D1	5.2	5.46	0.205	0.215
E	5.4	6.22	0.213	0.245
e	2.30 BSC		0.091 BSC	
e1	4.50	4.70	0.177	0.185
L	7.50	9.65	0.295	0.380

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