

General Description

The 25N50K uses advanced technology and design to provide excellent $R_{DS(on)}$. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Features

- Low on-resistance
- Low reverse transfer capacitance
- 100% avalanche tested

Mechanical Data

- Case: TO-3P Package

Application

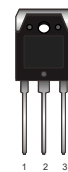
- Power switching application

Ordering Information

Part No.	Package Type	Package	Quality(box)
25N50K	TO-3P	Tube	600

Product Summary			
V_{DS}	$R_{DS(on)}$ (Ω) Typ	I_D (A)	Q_g (Typ)
500V	0.17@ 10V	25	81nc

TO-3P
25N50K



Block Diagram

Pin Definition:

1. Gate
2. Drain
3. Source

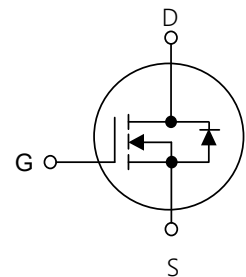


Table 1 Absolute Maximum Ratings ($T_c=25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current $T_c=25^\circ\text{C}$	I_D	25	A
Pulsed Drain Current (Note 1)	I_{DM}	100	A
Single Pulse Avalanche Energy	E_{AS}	2000	mJ
Power Dissipation $T_c=25^\circ\text{C}$	P_D	250	W
Operating Junction and Storage Temperature	T_J/T_{STG}	-55~+175	$^\circ\text{C}$

Table 2. Thermal Characteristics

Parameter	Symbol	25N50K	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	75	$^{\circ}C/W$
Thermal resistance Junction to Case	$R_{\theta JC}$	0.5	$^{\circ}C/W$

Table 3. Electrical Characteristics ($T_J=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	500	-	-	V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500V, V_{GS}=0V$	-	-	1	μA	
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=30V, V_{DS}=0V$	-	-	100	nA
	Reverse	I_{GSS}	$V_{GS}=-30V, V_{DS}=0V$	-	-	-100	nA
On Characteristics(Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	-	4.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=12.5A$	-	0.17	0.2	Ω	
Dynamic Characteristics(Note 3)							
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	3860	-	pF	
Output Capacitance	C_{OSS}		-	428	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	38	-	pF	
Switching Characteristics (Note 3)							
Turn-On Delay Time	$t_d(on)$	$V_{DD}=250V, I_D=25A$ $R_G=10\Omega,$	-	48	-	ns	
Turn-On Rise Time	t_R		-	108	-	ns	
Turn-Off Delay Time	$t_d(off)$		-	165	-	ns	
Turn-Off Fall Time	t_f	$V_{DS}=400V, I_D=25A,$ $V_{GS}=10V$	-	85	-	ns	
Total Gate Charge	Q_G		-	81	-	nC	
Gate-Source Charge	Q_{GS}		-	20	-	nC	
Gate-Drain Charge	Q_{GD}		-	30	-	nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=25A$	-	-	1.5	V	
Maximum Continuous Drain-Source Diode Forward Current	I_S		-	-	25	A	
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_F=25A$	-	530	-	ns	
Reverse Recovery Charge	Q_{RR}	$di/dt=100A/\mu s$ (Note 1)	-	8.2	-	μC	

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature
 2 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
 3 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

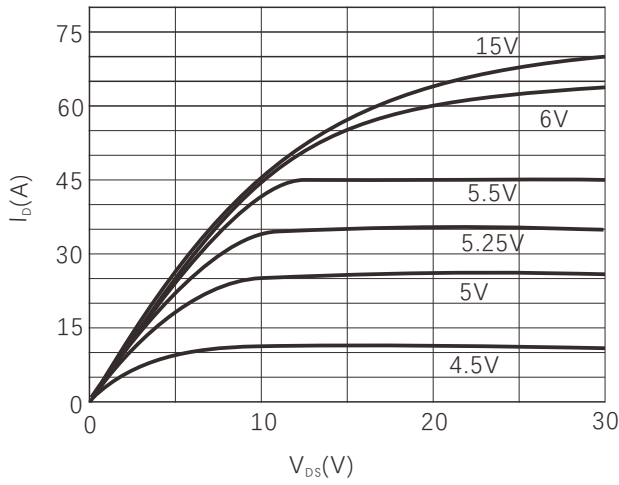


Figure 2. Normalized $R_{DS(ON)}$ vs Temperature

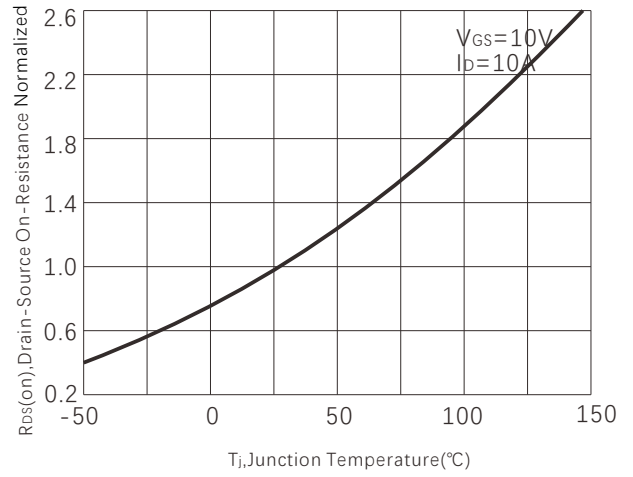


Figure 3. On-Resistance vs. Drain Current

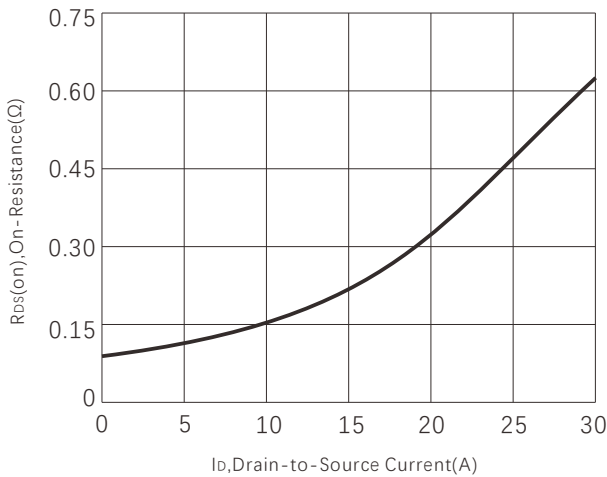


Figure 4. Capacitance

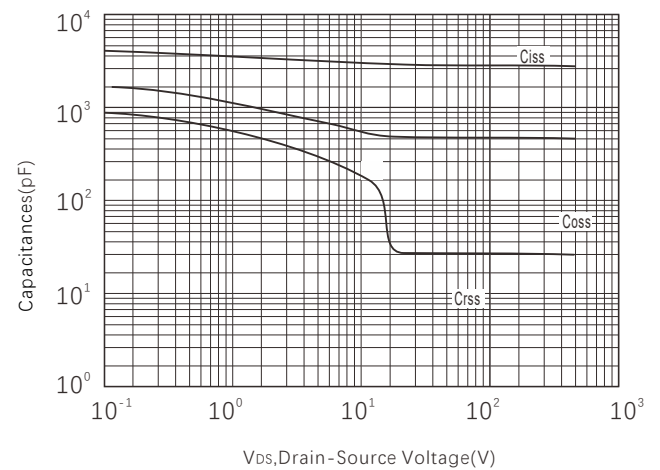


Figure 5. Gate charge

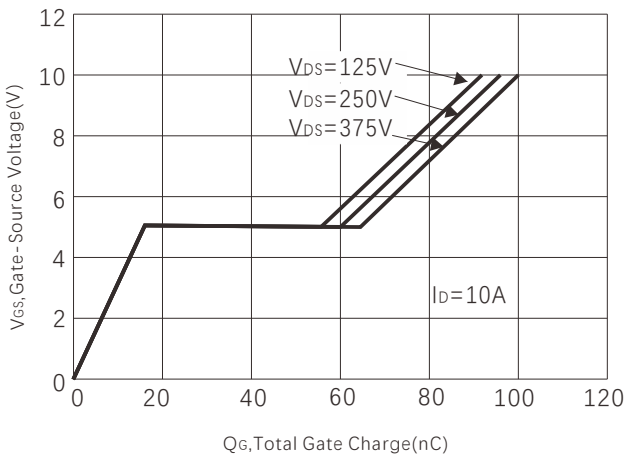


Figure 6. Source-Drain Diode Forward Voltage

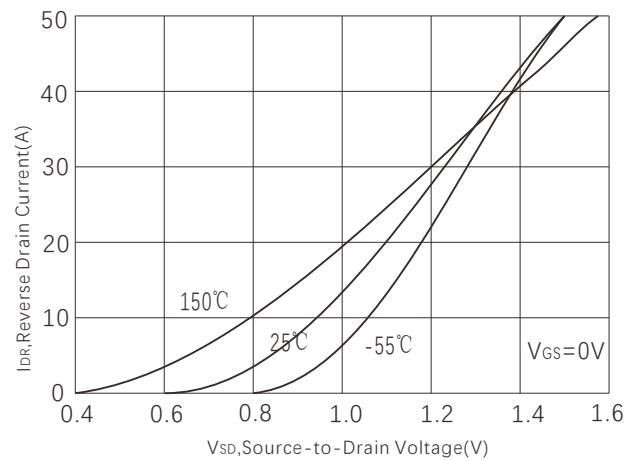


Figure 7. Typical Breakdown Voltage vs Temperature

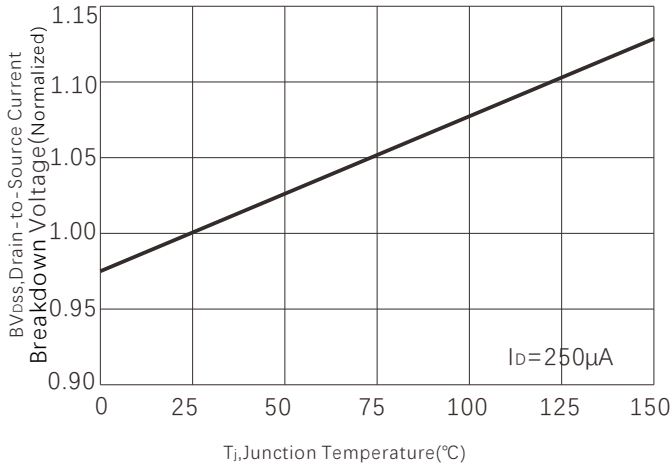


Figure 8. Gate Threshold Voltage vs Temperature

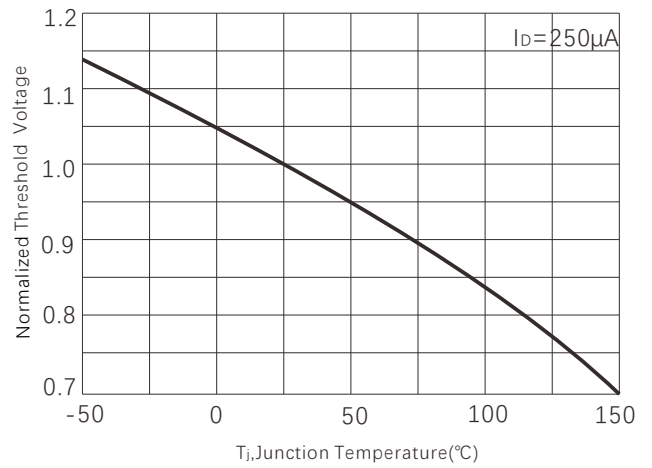


Figure 9. Safe operating area

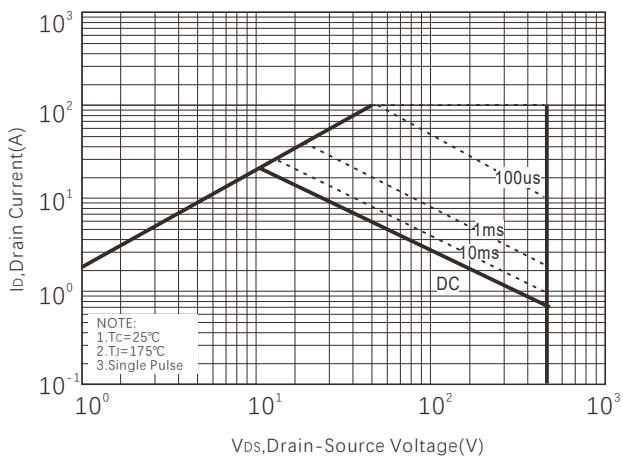


Figure 10. Power dissipation vs Case Temperature

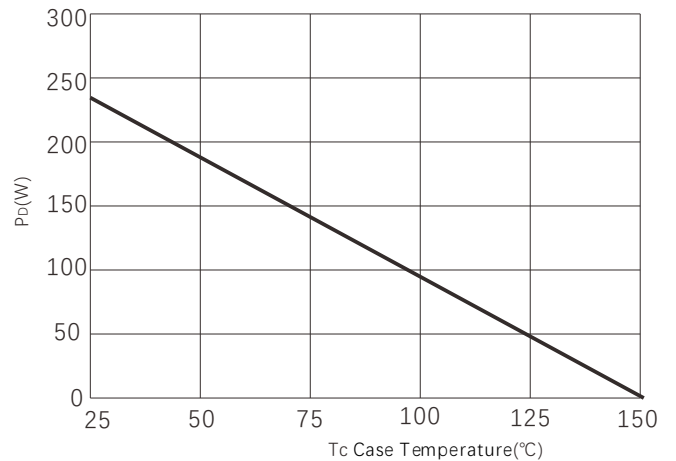
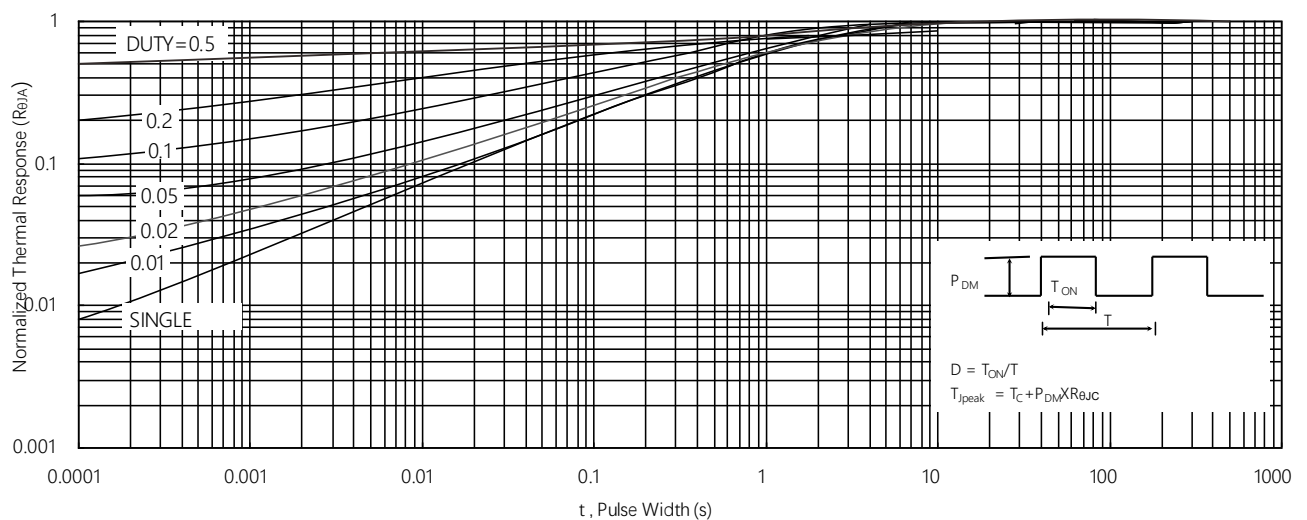
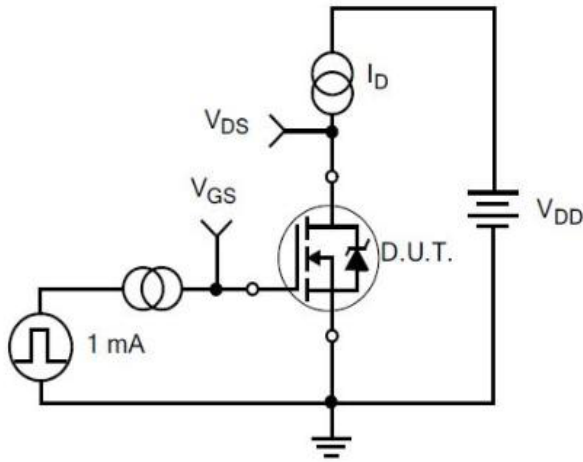


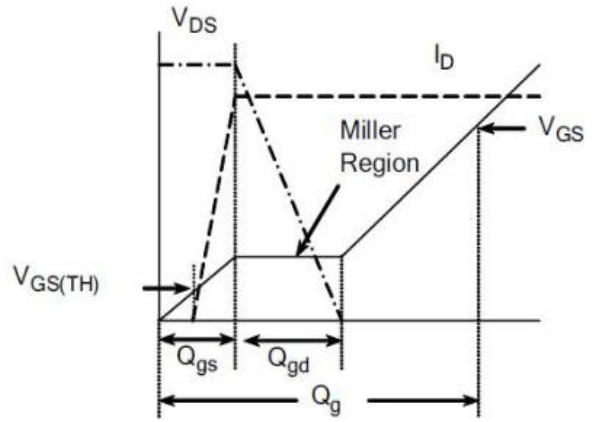
Figure 11. Normalized Maximum Transient Thermal Impedance



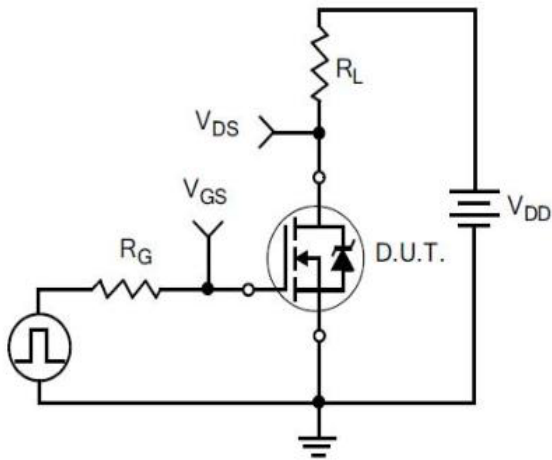
Typical Test Circuit



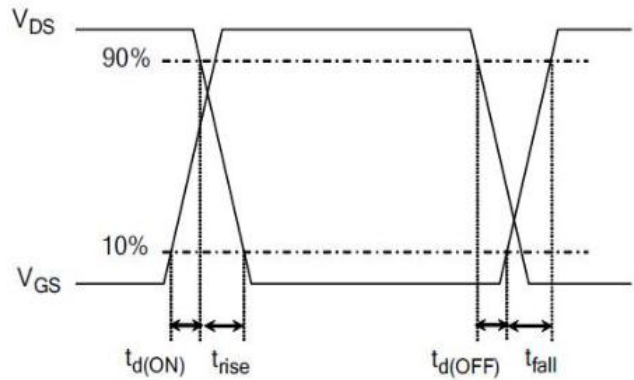
1) Gate Charge Test Circuit



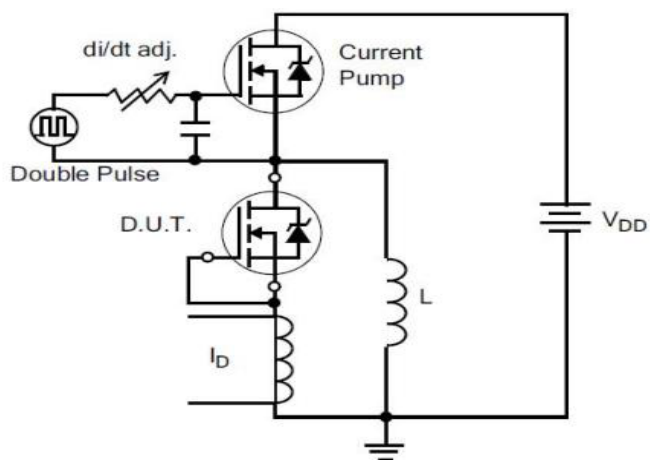
2) Gate Charge Waveform



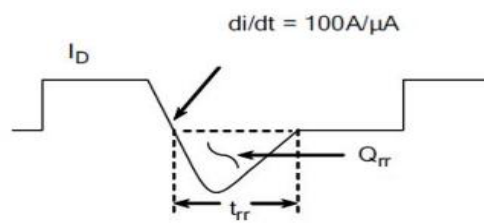
3) Resistive Switching Test Circuit



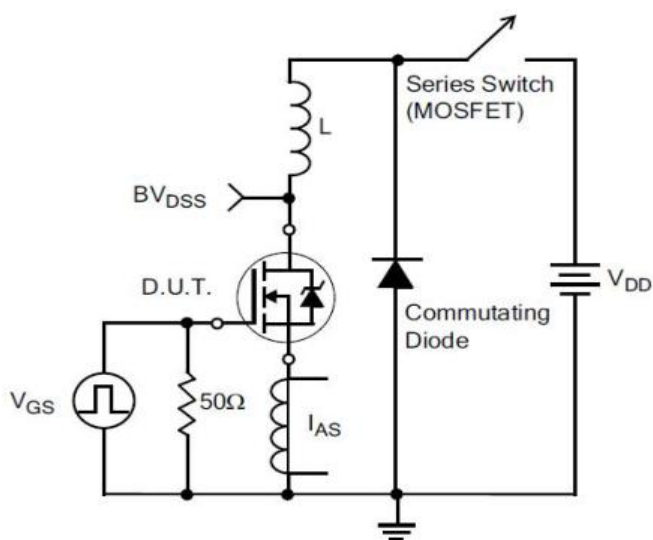
4) Resistive Switching Waveforms



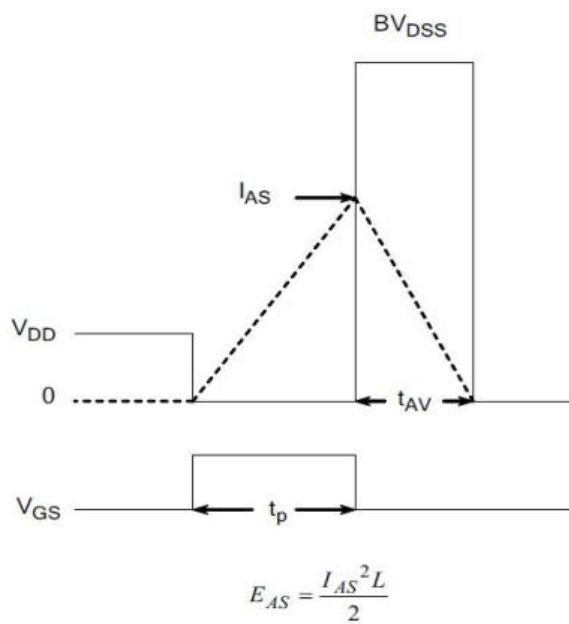
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



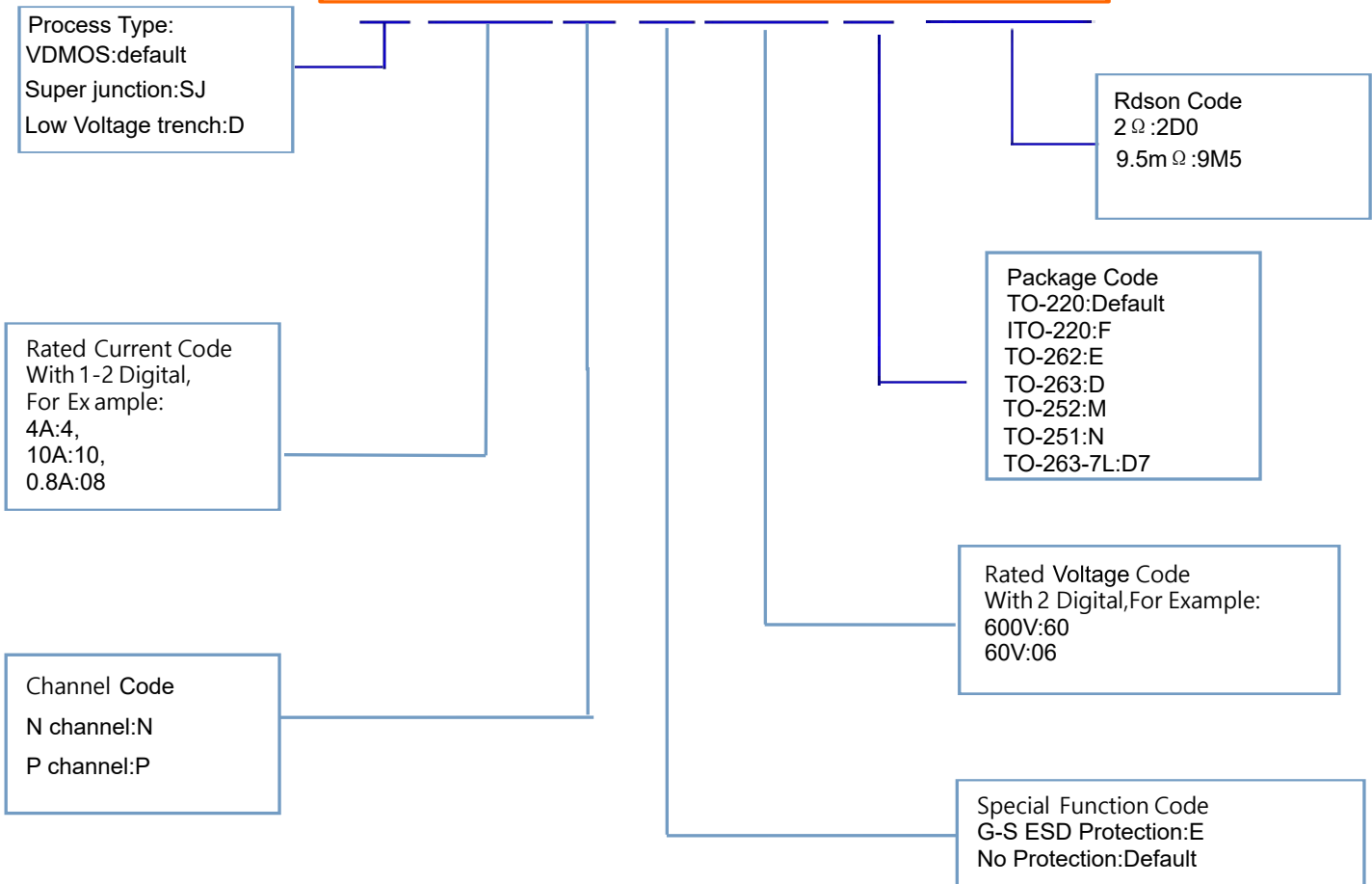
7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

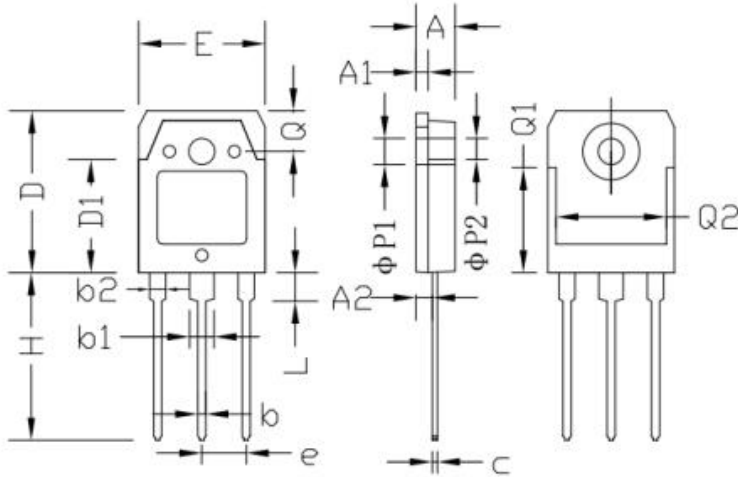
Product Names Rules

X X X N E X X X-X X X



Dimensions

TO-3P PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	4.60	5.00	0.181	0.197
A1	1.45	1.65	0.057	0.065
A2	2.20	2.60	0.087	0.102
b	0.80	1.20	0.032	0.047
b1	2.80	3.20	0.110	0.126
b2	1.80	2.20	0.071	0.087
C	0.55	0.75	0.022	0.030
D	19.20	19.70	0.756	0.776
D1	13.10	14.70	0.516	0.578
E	15.40	15.80	0.607	0.623
e	5.45 TYP		0.215 TYP	
H	19.80	20.20	0.780	0.826
L	3.30	3.70	0.130	0.146
ΦP1	3.20 TYP		0.126 TYP	
ΦP2	3.50 TYP		0.138 TYP	
Q	5.00 TYP		0.197 TYP	
Q1	12.40 TYP		0.488 TYP	
Q2	12.6	-	0.496	-

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