

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

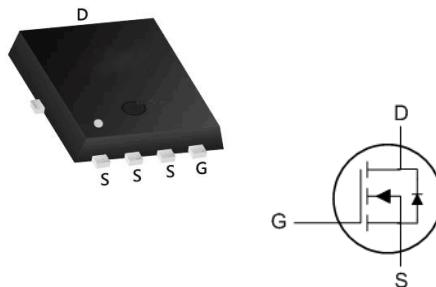
Product Summary

BVDSS	RDS(ON)	ID
30V	9mΩ	46A

Description

The JHQ3004 is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications. The JHQ3004 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

DFN3 X3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	46	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	29	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	11	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	9	A
I _{DM}	Pulsed Drain Current ²	92	A
EAS	Single Pulse Avalanche Energy ³	57.8	mJ
I _{AS}	Avalanche Current	34	A
P _D @T _C =25°C	Total Power Dissipation ⁴	29	W
P _D @T _A =25°C	Total Power Dissipation ⁴	1.67	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	75	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	4.32	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	30	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.027	---	$\text{V}/^\circ\text{C}$
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=15\text{A}$	---	---	9	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=10\text{A}$	---	---	15	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.0	---	2.5	V
$\Delta V_{\text{GS(th)}}$	$V_{\text{GS(th)}}$ Temperature Coefficient		---	-5.8	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=15\text{A}$	---	9.8	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $I_D=12\text{A}$	---	12.8	---	nC
Q_{gs}	Gate-Source Charge		---	3.3	---	
Q_{gd}	Gate-Drain Charge		---	6.5	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=12\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$	---	4.5	---	ns
T_r	Rise Time		---	10.8	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	25.5	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1317	---	pF
C_{oss}	Output Capacitance		---	163	---	
C_{rss}	Reverse Transfer Capacitance		---	131	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	46	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	92	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=34\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.

Typical Characteristics

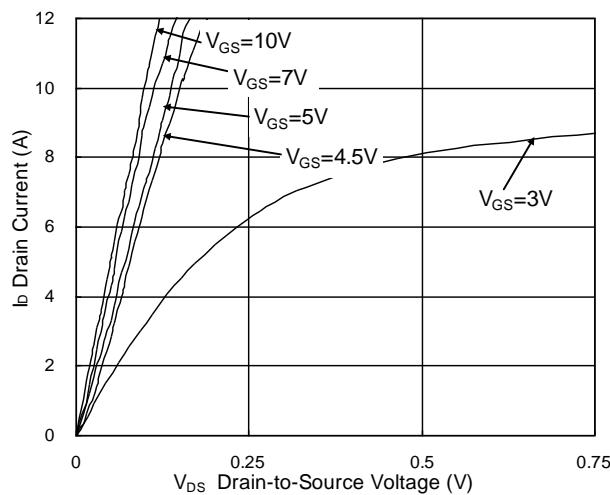


Fig.1 Typical Output Characteristics

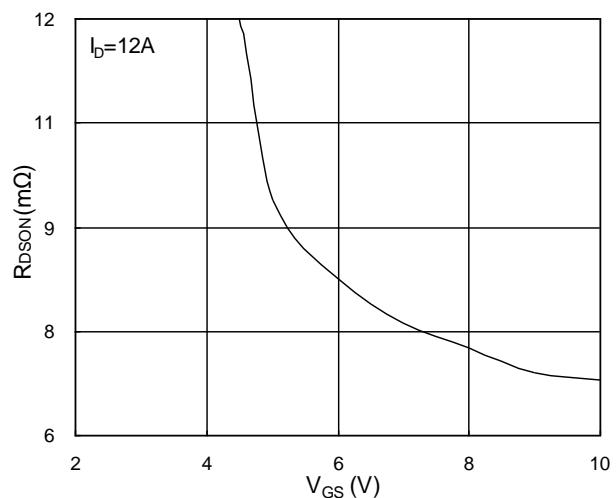


Fig.2 On-Resistance vs. Gate-Source

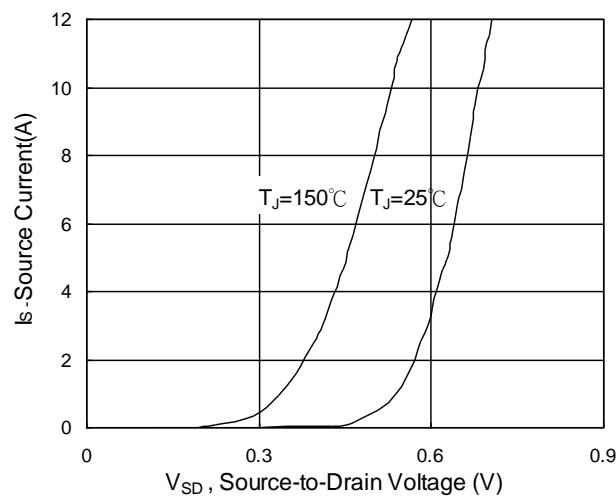


Fig.3 Forward Characteristics Of Reverse

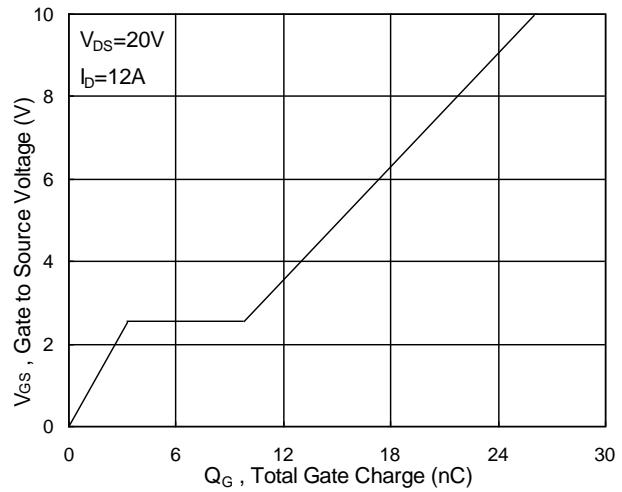


Fig.4 Gate-Charge Characteristics

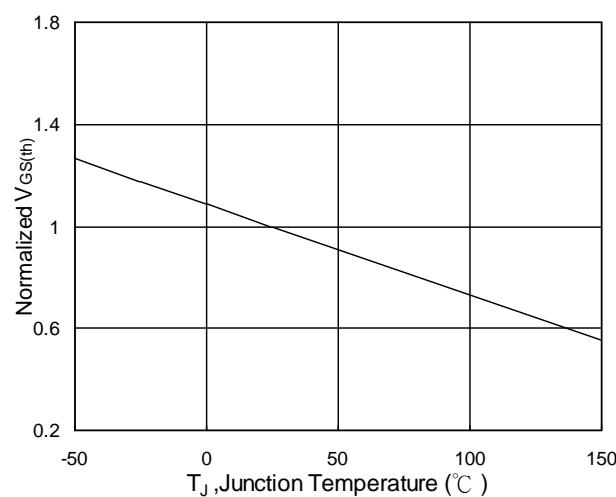


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

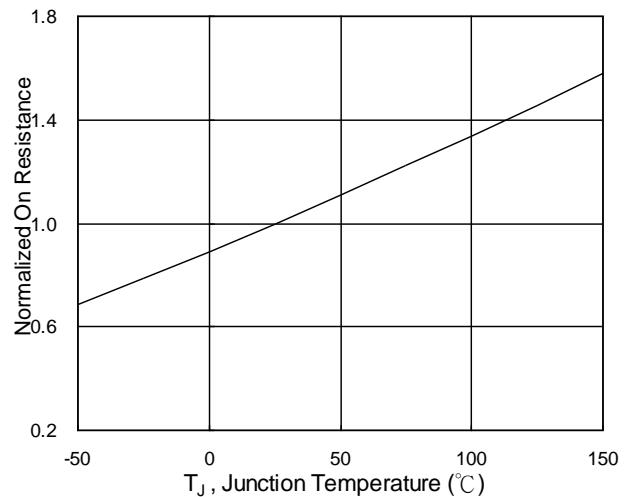
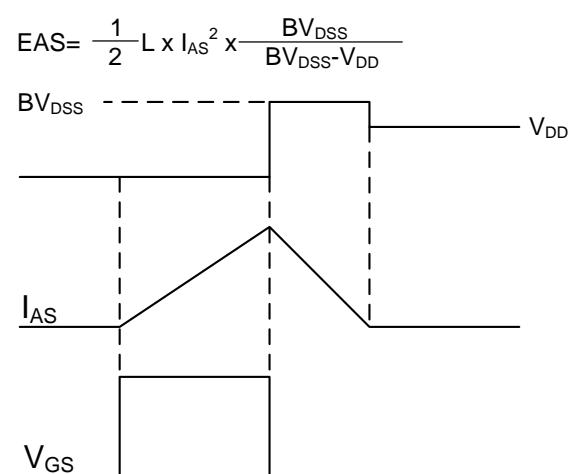
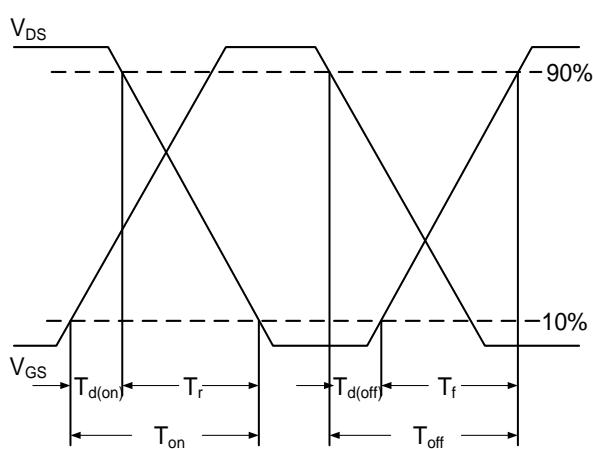
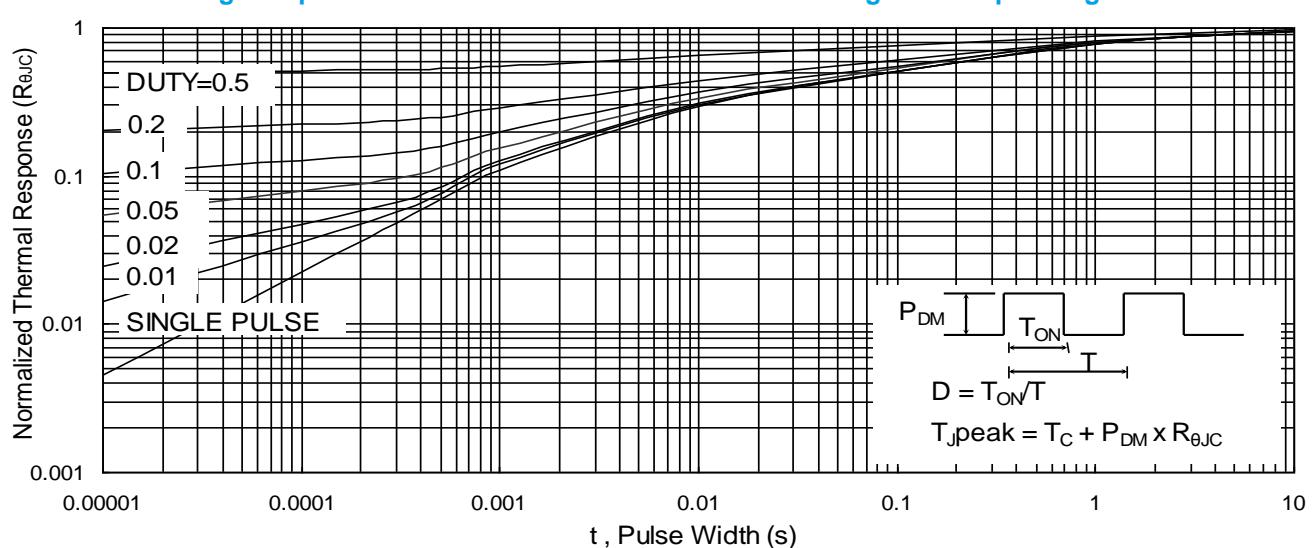
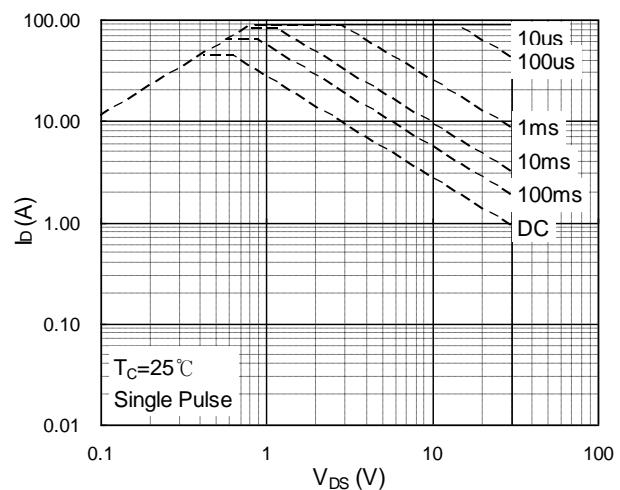
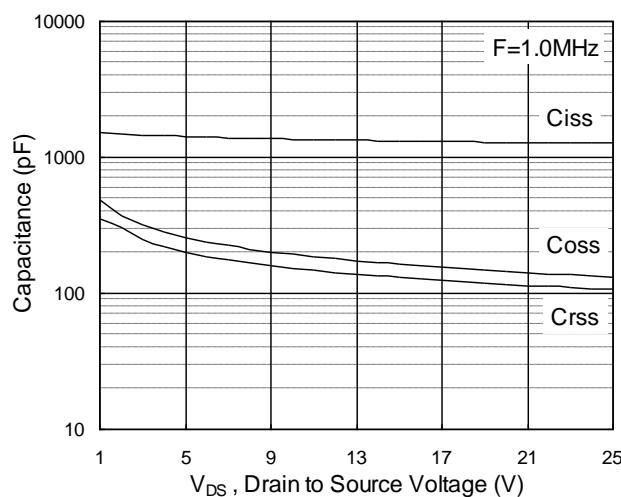
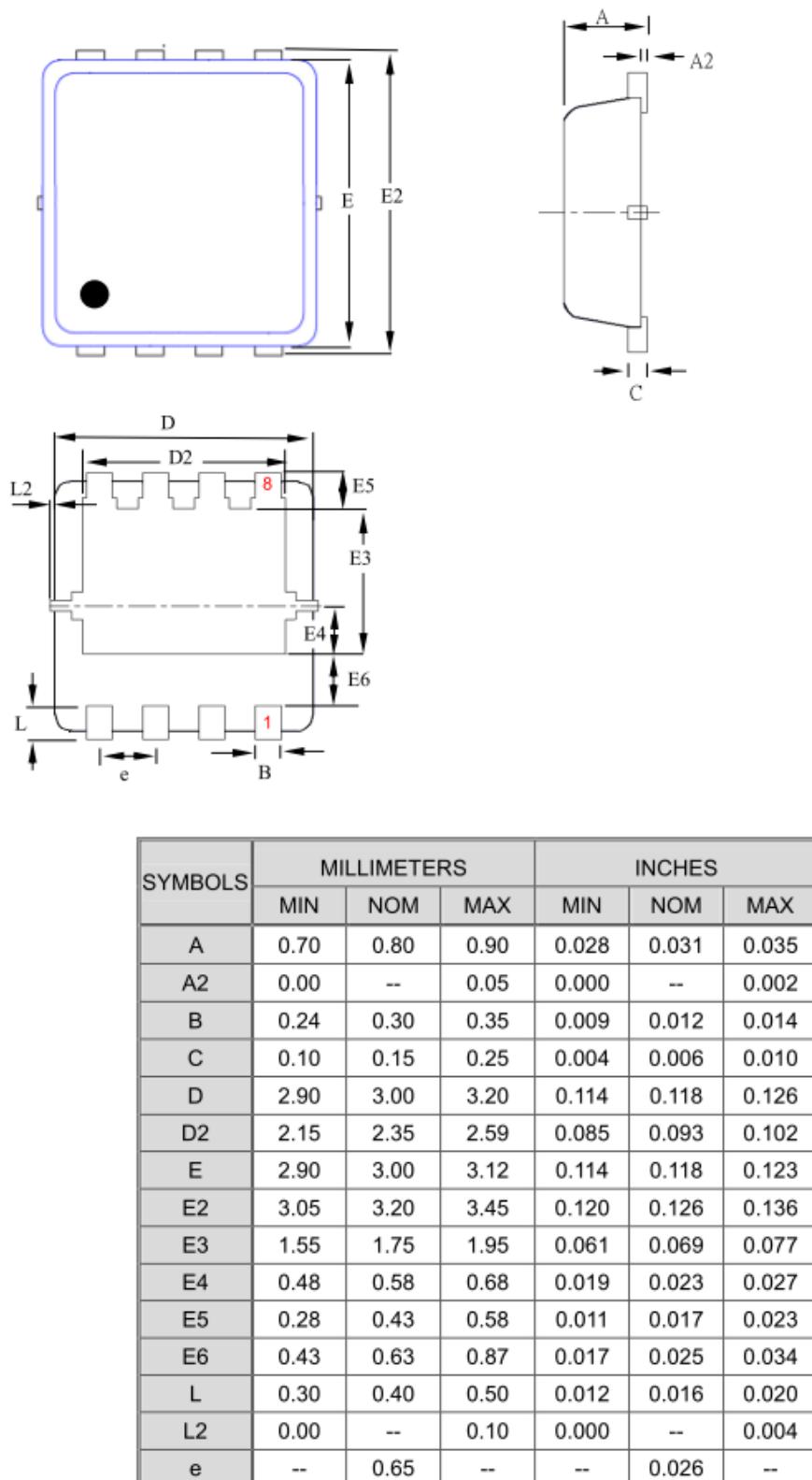


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



DFN3*3 Package Outline Dimensions



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