

### Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

### Description

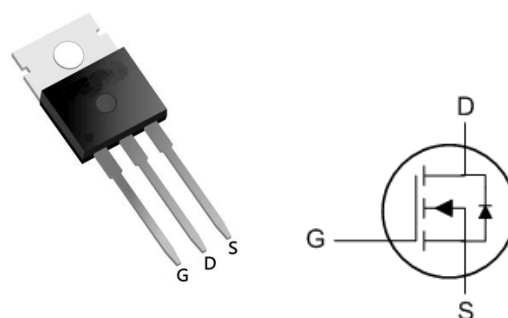
The D165N04 is the high cell density trenched N-ch MOSFETs, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications.

The D165N04 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

### Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
40V	3.3mΩ	167A

### TO-220 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	167	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	105	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	360	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	125	mJ
I <sub>AS</sub>	Avalanche Current	50	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	149	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	0.84	°C/W

# D165N04

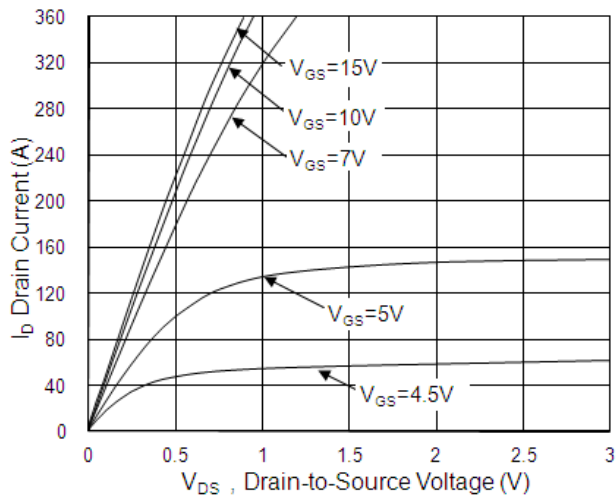
## Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=30A$	---	2.6	3.3	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2	---	4.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	53	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	0.8	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=32V, V_{GS}=10V, I_D=20A$	---	65	---	nC
$Q_{gs}$	Gate-Source Charge		---	24	---	
$Q_{gd}$	Gate-Drain Charge		---	21	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=20V, V_{GS}=10V, R_G=3.3\Omega, I_D=30A$	---	26	---	ns
$T_r$	Rise Time		---	38	---	
$T_{d(off)}$	Turn-Off Delay Time		---	63	---	
$T_f$	Fall Time		---	20	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	4711	---	pF
$C_{oss}$	Output Capacitance		---	869	---	
$C_{rss}$	Reverse Transfer Capacitance		---	367	---	
<b>Diode Characteristics</b>						
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	167	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	360	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=30A, di/dt=100A/\mu s,$	---	20.3	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	9.5	---	nC

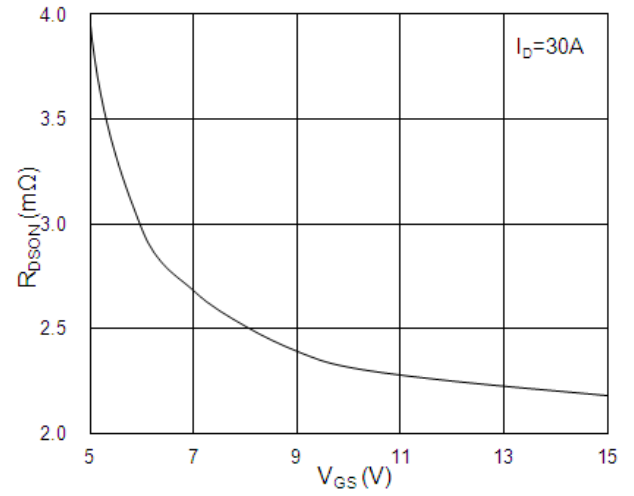
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=50A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 85A.

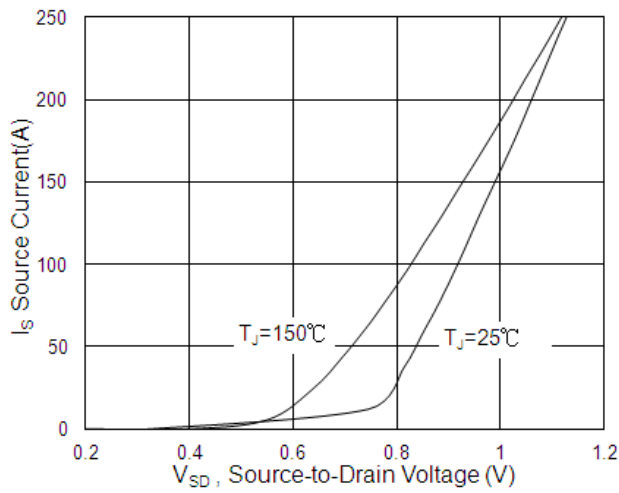
## Typical Characteristics



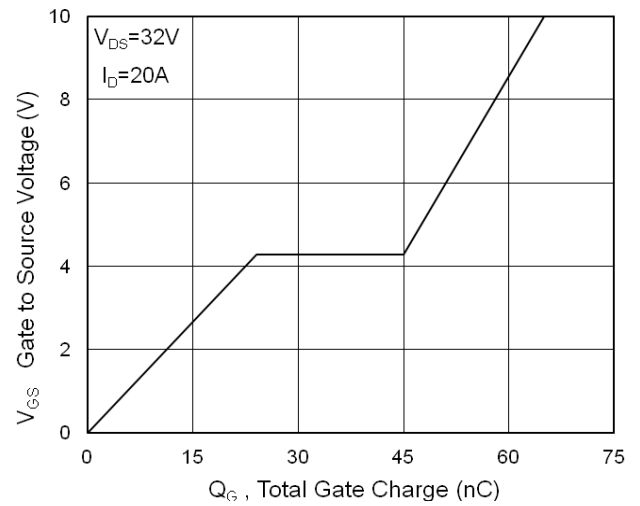
**Fig.1 Typical Output Characteristics**



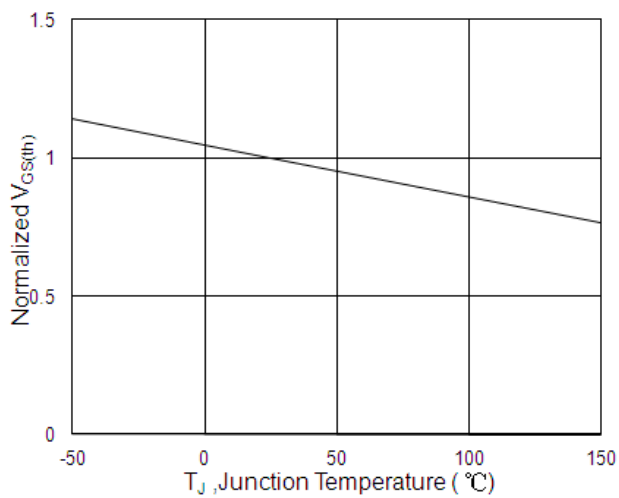
**Fig.2 On-Resistance v.s Gate-Source**



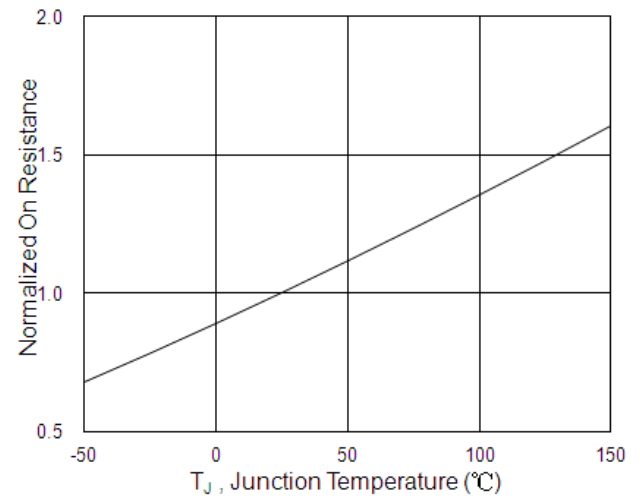
**Fig.3 Forward Characteristics of Reverse**



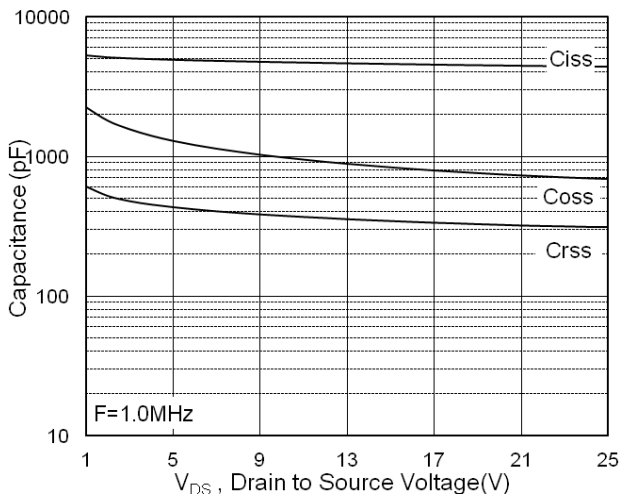
**Fig.4 Gate-Charge Characteristics**



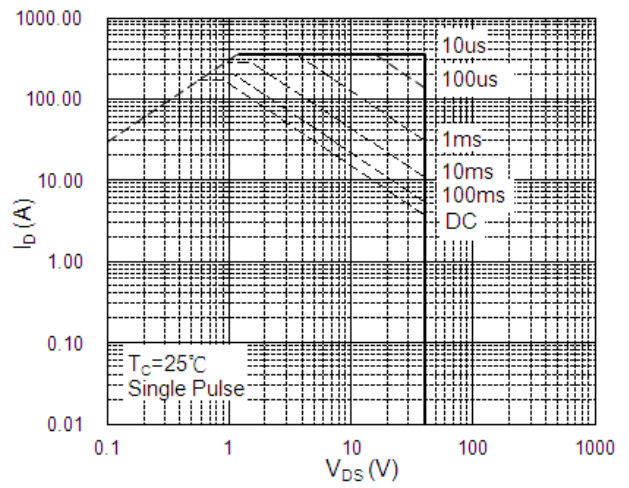
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



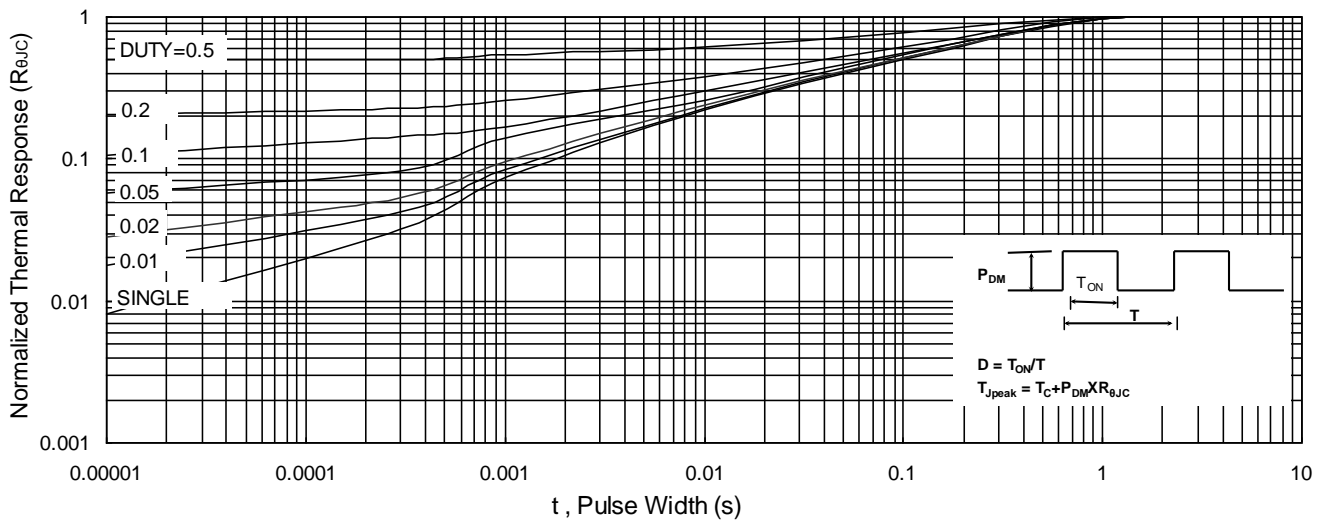
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



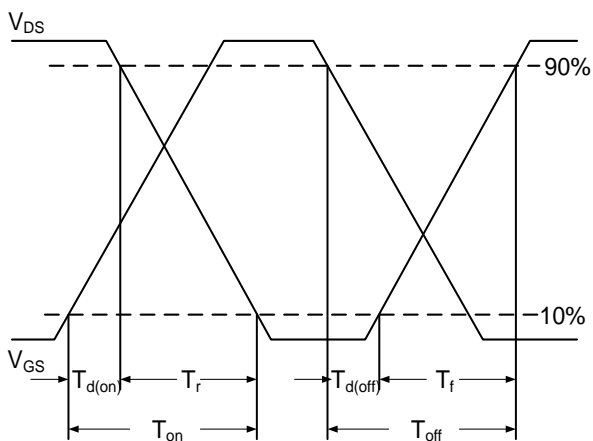
**Fig.7 Capacitance**



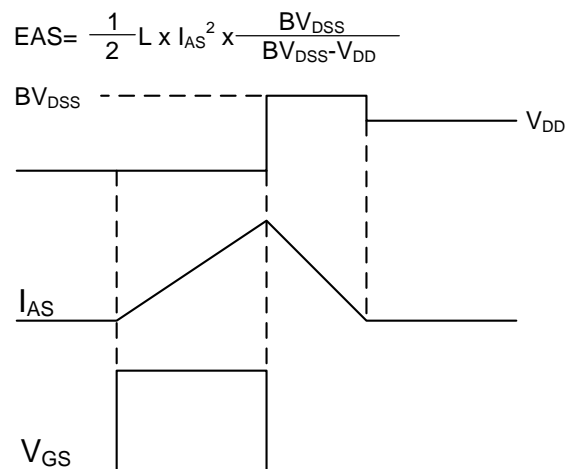
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



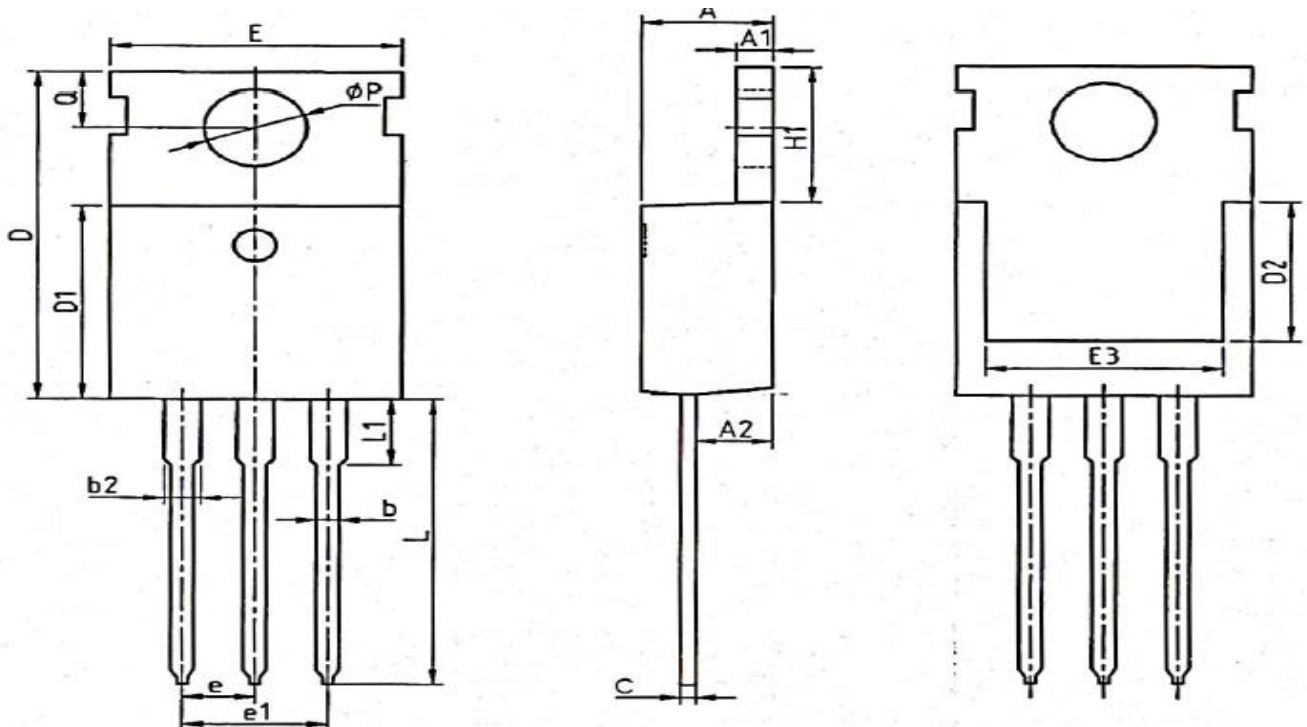
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

# D165N04

## TO-220 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.556	4.826	0.14	0.19
A1	0.508	1.4	0.02	0.055
A2	2.032	2.921	0.08	0.115
b	0.381	1.016	0.015	0.04
b2	1.143	1.778	0.045	0.07
c	0.356	0.61	0.014	0.024
D	14.224	16.51	0.56	0.65
D1	8.382	9.017	0.33	0.355
D2	5.5	-	0.216	-
E	9.652	10.668	0.38	0.42
E3	6.858	-	0.27	-
e	2.540 BSC		0.100 BSC	
e1	5.080 BSC		0.200 BSC	
H1	5.842	6.858	0.23	0.27
L	12.7	14.732	0.5	0.58
L1	-	4.06	-	0.16
Q	2.54	3.048	0.1	0.12

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