

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Description

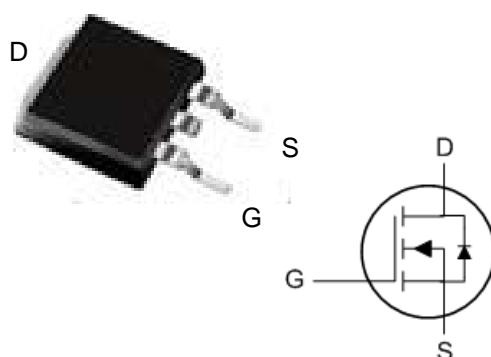
The D70N03M is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The D70N03M meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Product Summary

BVDSS	RDS(on)(Typ.)	ID
30V	2mΩ	70A

TO-252Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	70	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	54	A
I _{DM}	Pulsed Drain Current ²	280	A
EAS	Single Pulse Avalanche Energy ³	180	mJ
I _{AS}	Avalanche Current	60	A
P _D @T _C =25°C	Total Power Dissipation ⁴	60	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	2	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	30	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=30\text{A}$	---	2	2.4	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=15\text{A}$	---	2.6	3.2	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=24\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=30\text{A}$	---	50	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=15\text{A}$	---	56.9	---	nC
Q_{gs}	Gate-Source Charge		---	13.8	---	
Q_{gd}	Gate-Drain Charge		---	23.5	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=1\text{A}$	---	20.1	---	ns
T_r	Rise Time		---	6.3	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	124.6	---	
T_f	Fall Time		---	15.8	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	4345	---	pF
C_{oss}	Output Capacitance		---	340	---	
C_{rss}	Reverse Transfer Capacitance		---	225	---	
Diode Characteristics						
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	70	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=60\text{A}$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- The maximum current rating is package limited.

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Typical Characteristics

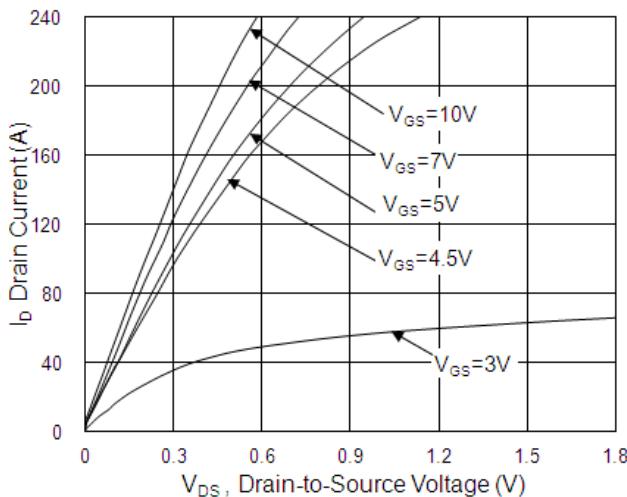


Fig.1 Typical Output Characteristics

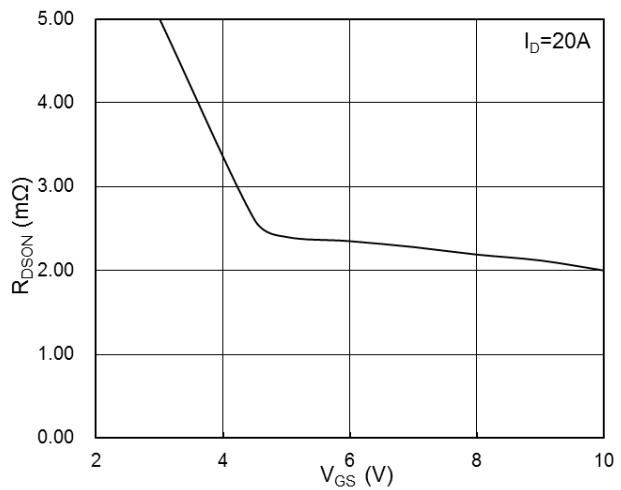


Fig.2 On-Resistance vs. G-S Voltage

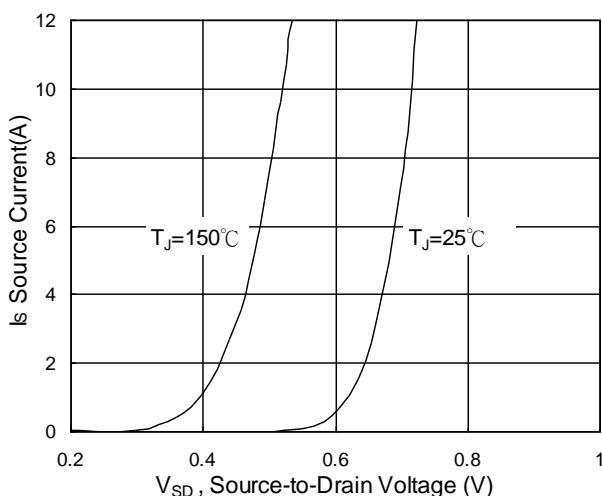


Fig.3 Source Drain Forward Characteristics

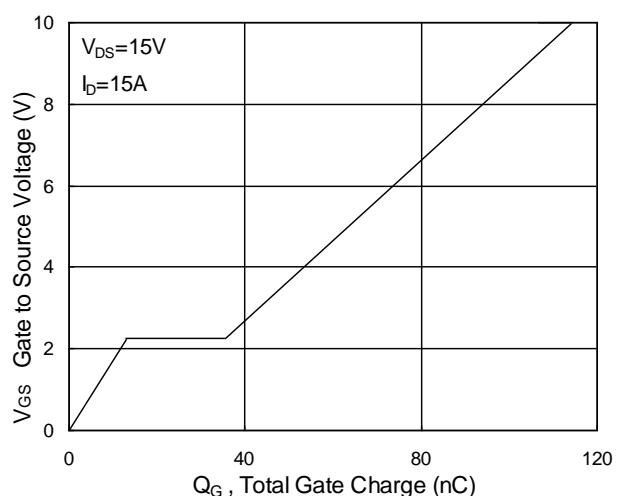


Fig.4 Gate-Charge Characteristics

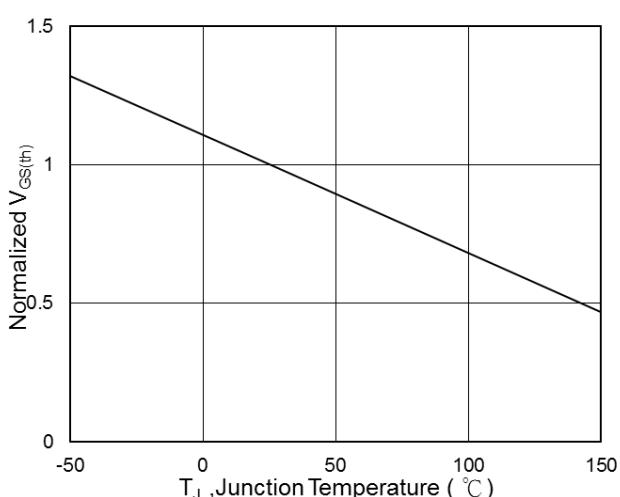


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

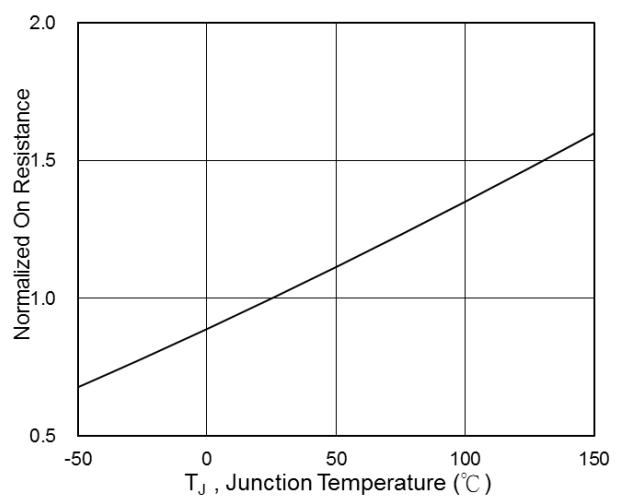


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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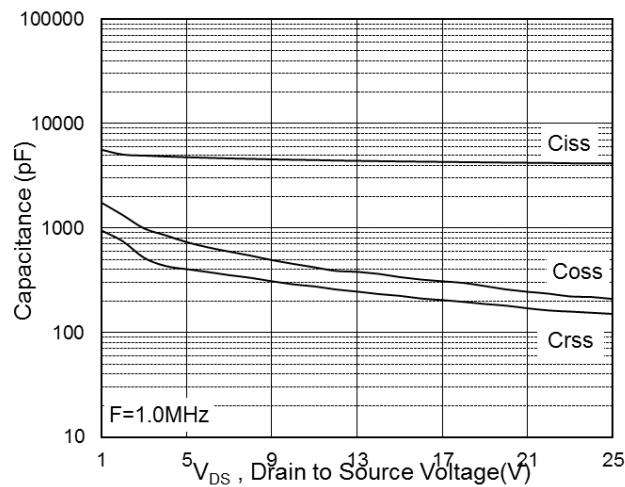


Fig.7 Capacitance

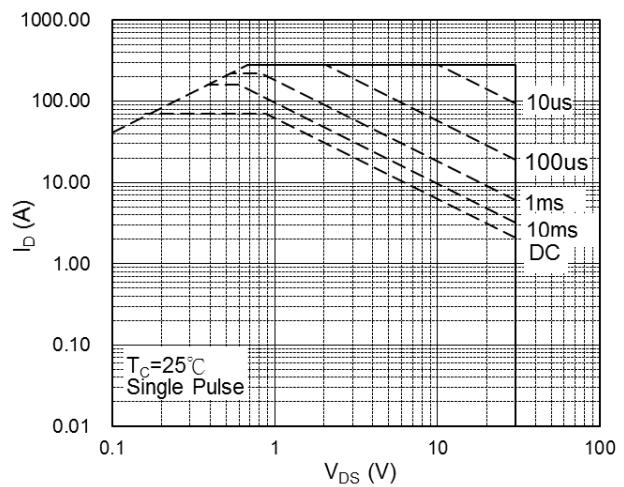


Fig.8 Safe Operating Area

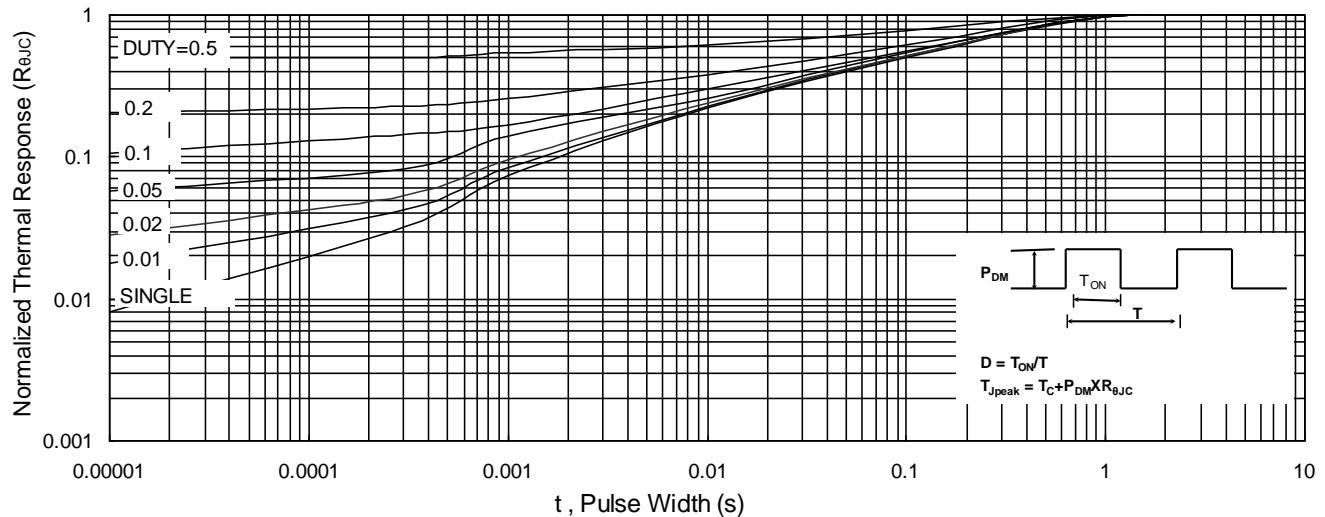


Fig.9 Normalized Maximum Transient Thermal Impedance

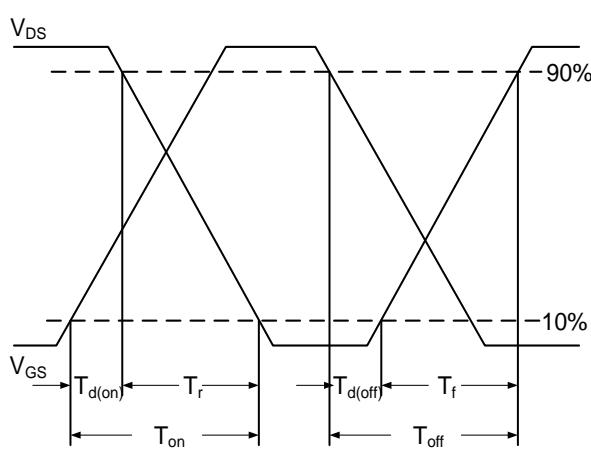


Fig.10 Switching Time Waveform

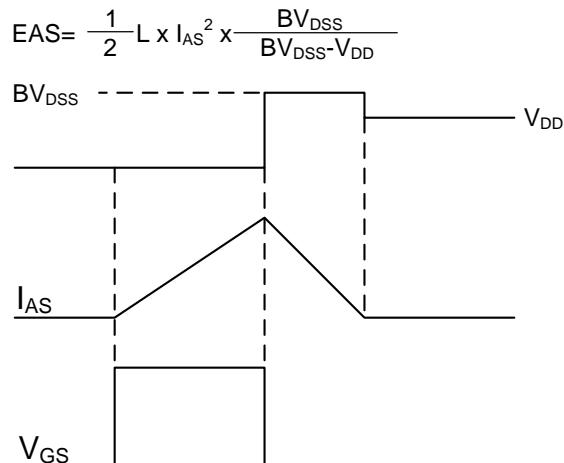
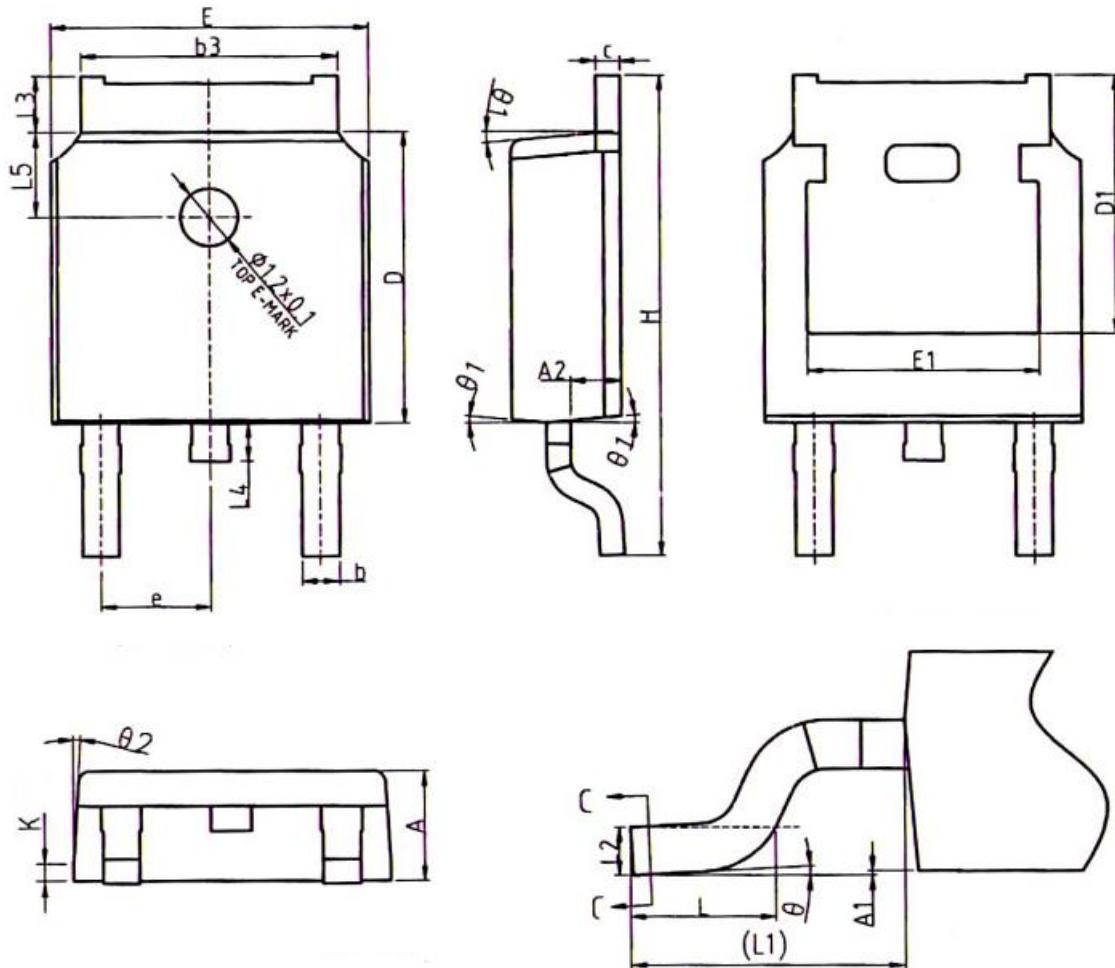


Fig.11 Unclamped Inductive Switching Waveform

TO252 Package Outline Dimensions



SYMBOL	MILLIMETERS			SYMBOL	MILLIMETERS		
	MIN	NOM	MAX		MIN	NOM	MAX
A	2.20	2.30	2.38	H	9.90	10.10	10.30
A1	0.00	---	0.10	L	1.40	1.50	1.70
A2	0.97	1.07	1.17	L1	2.90REF		
b	0.72	0.78	0.85	L2	0.51BSC		
b3	5.23	5.33	5.46	L3	0.90	---	1.25
c	0.47	0.53	0.58	L4	0.60	0.80	1.00
D	6.00	6.10	6.20	L5	1.70	1.80	1.90
D1	5.30REF			θ	0°	---	8°
E	6.50	6.60	6.70	θ1	5°	7°	9°
E1	4.70	4.83	4.92	θ2	5°	7°	9°
e	2.286BSC			K	0.40REF		

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