

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

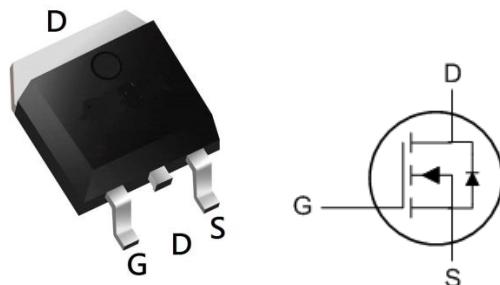
BVDSS	RDS(ON)	ID
40V	3.3mΩ	165A

Description

The D165N04D is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

The D165N04D meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO263 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	40	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	165	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	100	A
I _{DM}	Pulsed Drain Current ²	250	A
EAS	Single Pulse Avalanche Energy ³	125	mJ
I _{AS}	Avalanche Current	50	A
P _D @T _C =25°C	Total Power Dissipation ⁴	149	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	0.84	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=30\text{A}$	---	2.6	3.3	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	2	---	4.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=30\text{A}$	---	53	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	0.8	---	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	65	---	nC
Q_{gs}	Gate-Source Charge		---	24	---	
Q_{gd}	Gate-Drain Charge		---	21	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=30\text{A}$	---	26	---	ns
T_r	Rise Time		---	38	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	63	---	
T_f	Fall Time		---	20	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	4711	---	pF
C_{oss}	Output Capacitance		---	869	---	
C_{rss}	Reverse Transfer Capacitance		---	367	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	165	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=30\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	20.3	---	nS
Q_{rr}	Reverse Recovery Charge		---	9.5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=50\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 85A.

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Typical Characteristics

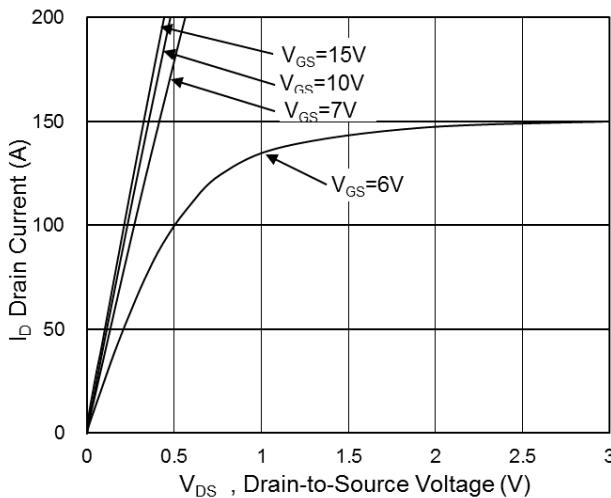


Fig.1 Typical Output Characteristics

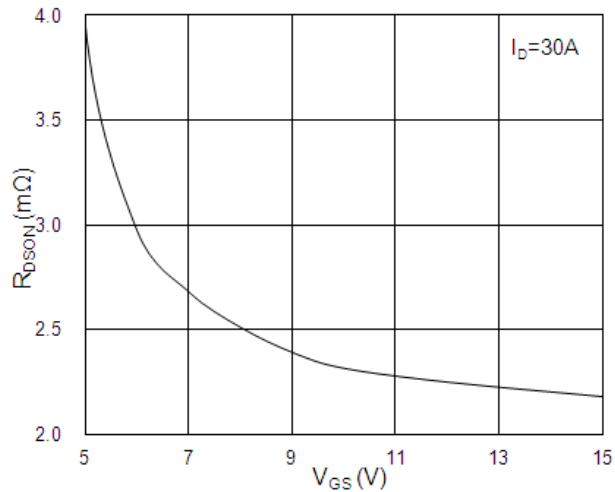


Fig.2 On-Resistance vs G-S Voltage

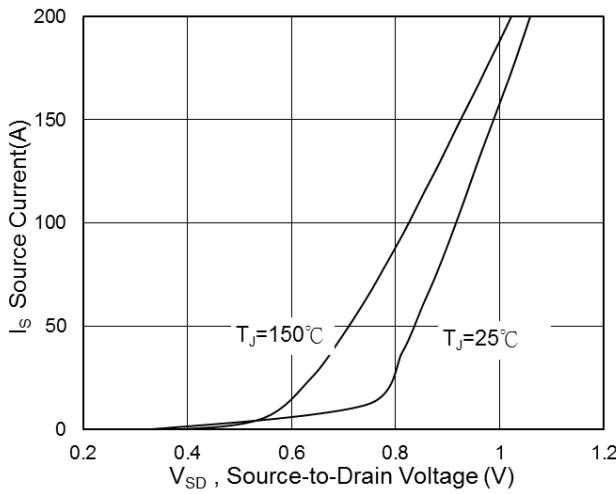


Fig.3 Forward Characteristics of Reverse

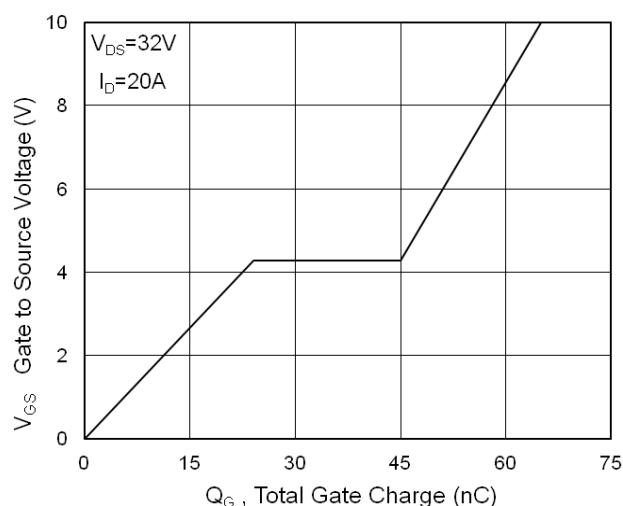


Fig.4 Gate-Charge Characteristics

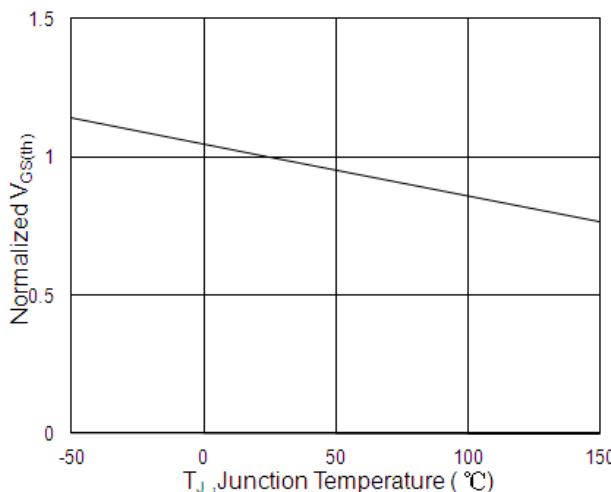


Fig.5 Normalized $V_{GS(th)}$ vs T_J

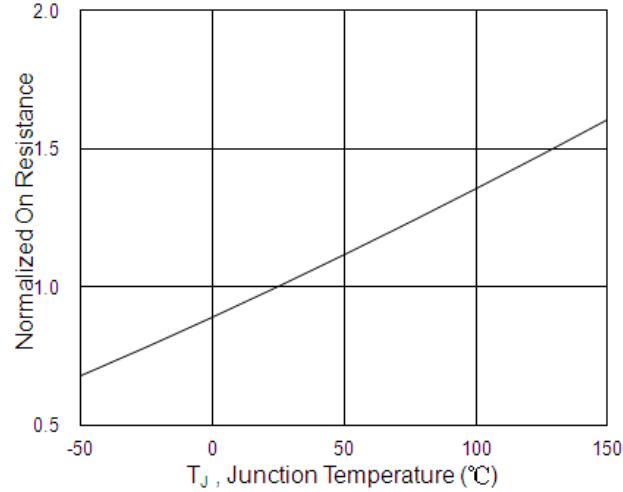


Fig.6 Normalized $R_{DS(on)}$ vs T_J

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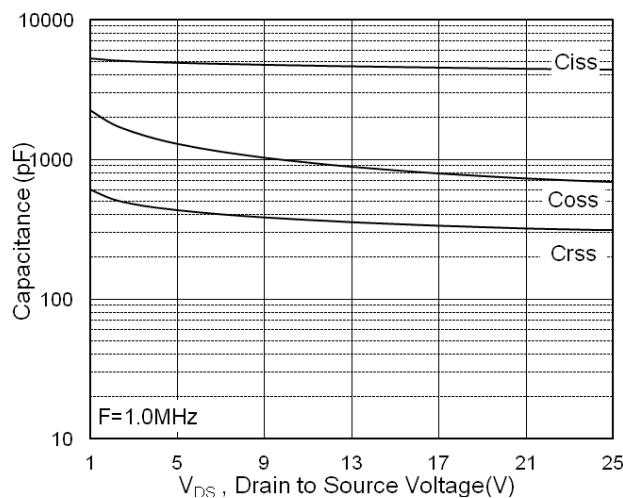


Fig.7 Capacitance

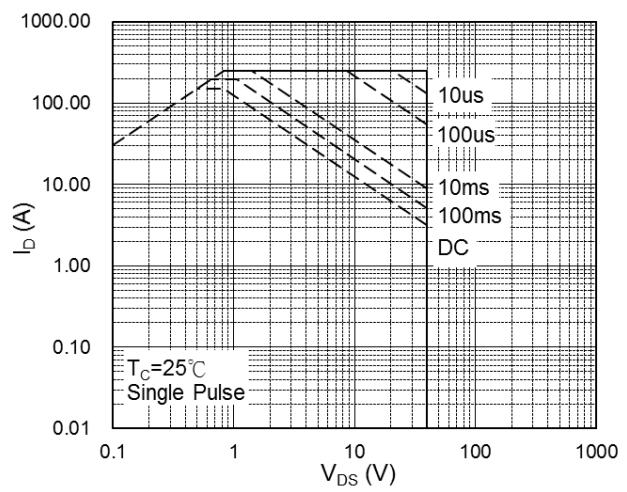


Fig.8 Safe Operating Area

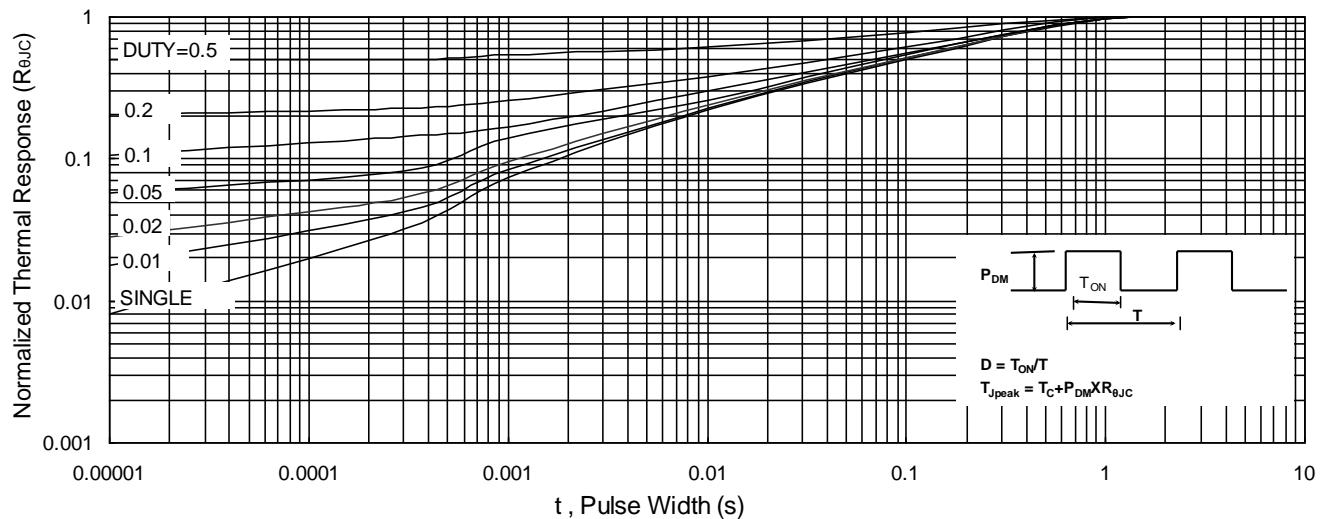


Fig.9 Normalized Maximum Transient Thermal Impedance

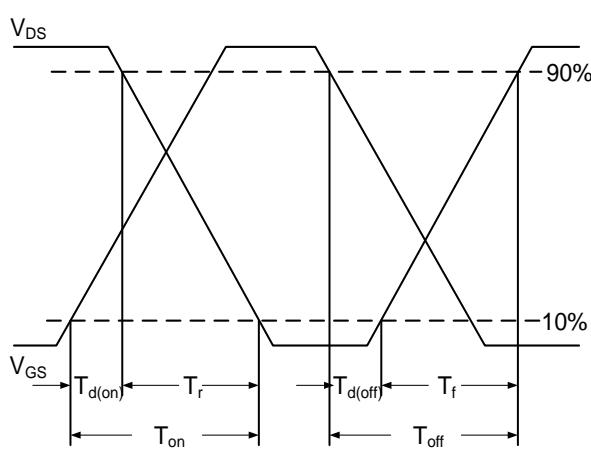


Fig.10 Switching Time Waveform

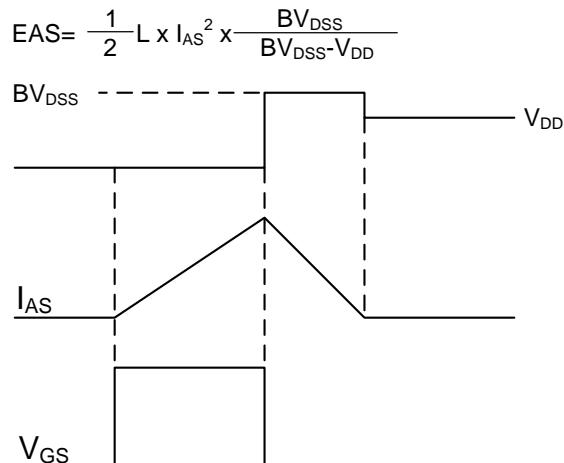
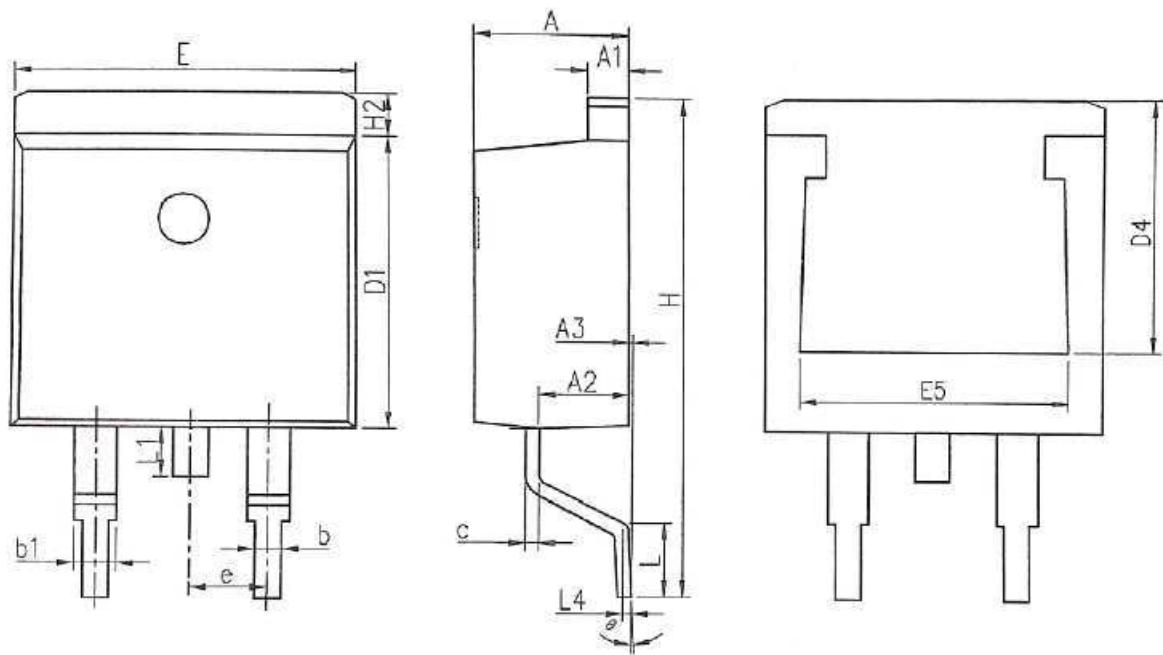


Fig.11 Unclamped Inductive Switching Waveform

TO-263 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.370	4.770	0.172	0.188
A1	1.220	1.420	0.048	0.056
A2	2.200	2.890	0.087	0.114
A3	0.000	0.250	0.000	0.010
b	0.700	0.960	0.028	0.038
b1	1.170	1.470	0.046	0.058
c	0.300	0.530	0.012	0.021
D1	8.500	9.300	0.335	0.366
D4	6.600	-	0.260	-
E	9.860	10.36	0.388	0.408
E5	7.060	-	0.278	-
e	2.540 BSC		0.100 BSC	
H	14.70	15.70	0.579	0.618
H2	1.070	1.470	0.042	0.058
L	2.000	2.600	0.079	0.102
L1	1.400	1.750	0.055	0.069
L4	0.250 BSC		0.010 BSC	
Θ	0°	9°	0°	9°

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