

General Description

These N-channel enhanced VDMOSFETS Used advanced trench technology design, provided excellent Rdson and low gate charge. Which accords with the RoHS standard.

Product Summary			
V _{DS}	R _{DS(on)} (mΩ) Typ	I _D (A)	Q _g (Typ)
100V	83 @ 10V	12	15.5nc

Features

- Fast switching
- Low on-resistance
- Low gate charge and input capacitance
- 100% single pulse avalanche energy test

Mechanical Data

- Case:TO-251,TO-252 Package

Application

- Switching applications
- LED backlighting
- UPS power supply
- Load switch

TO-251
D12N10N



TO-252
D12N10M



Ordering Information

Part No.	Package Type	Package	Quality(box)
D12N10N	TO-251	Tube	1000
D12N10M	TO-252	Tape & Reel	3000

Block Diagram

Pin Definition:

1. Gate
2. Drain
3. Source

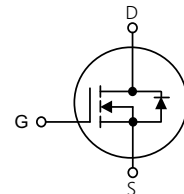


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter	Symbol	D12N10M/D12N10N	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _C =25°C	12
		T _C =100°C	8.5
Pulsed Drain Current (Note 1)	I _{DM}	48	A
Single Pulse Avalanche Energy (Note 2)	E _{AS}	16	mJ
Power Dissipation	P _D	T _a =25°C	1.25
		T _C =25°C	28
Operating Junction and Storage Temperature	T _J /T _{STG}	-55~+150	°C

Table 2. Thermal Characteristics

Parameter	Symbol	D12N10M/D12N10N	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	120	$^{\circ}C/W$
Thermal resistance Junction to Case	$R_{\theta JC}$	5.36	$^{\circ}C/W$

Table 3. Electrical Characteristics ($T_c=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate- Source Leakage Current	Forward	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Reverse	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On Characteristics(Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=6A$	-	83	110	m Ω
		$V_{GS}=4.5V, I_D=6A$	-	88	120	
Dynamic Characteristics(Note 5)						
Input Capacitance	C_{ISS}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	735	-	pF
Output Capacitance	C_{OSS}		-	49	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	18	-	pF
Switching Characteristics (Note 5)						
Turn-On Delay Time	$t_d(on)$	$V_{DS}=50V, R_L=8.6\Omega,$ $V_{GS}=10V, R_G=3\Omega$	-	9.7	-	ns
Turn-On Rise Time	t_R		-	3.6	-	ns
Turn-Off Delay Time	$t_d(off)$		-	20.4	-	ns
Turn-Off Fall Time	t_f		-	5.4	-	ns
Total Gate Charge	Q_G	$V_{DS}=50V, I_D=4.5A,$ $V_{GS}=10V$	-	15.5	-	nC
Gate-Source Charge	Q_{GS}		-	2.1	-	nC
Gate-Drain Charge	Q_{GD}		-	3.4	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=12A$	-	0.89	1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I_S		-	-	12	A
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_F=4.5A$	-	25	-	ns
Reverse Recovery Charge	Q_{RR}	$dI_F/dt=500A/\mu s$ (Note 1)	-	115	-	nC

Notes : 1 Repetitive Rating: Pulse width limited by maximum junction temperature

2 $L=0.5mH, I_D=8A, V_{DD}=50V$, Starting $T_J=25^{\circ}C$

4 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

5 Guaranteed by design, not subject to production

Typical Characteristics Diagrams

Figure1. On-Region Characteristics

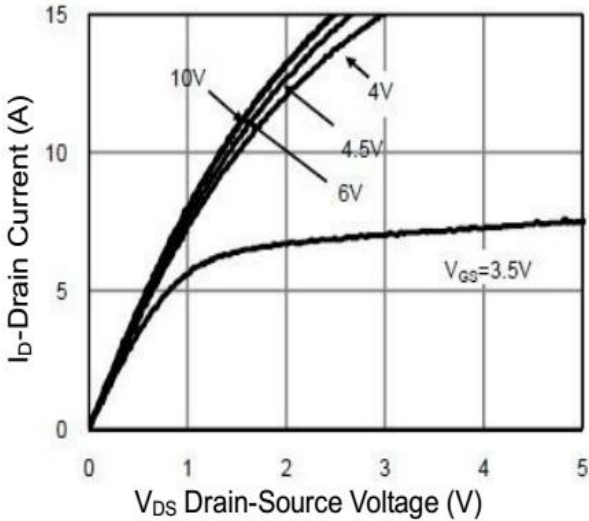


Figure 2: Transfer Characteristics

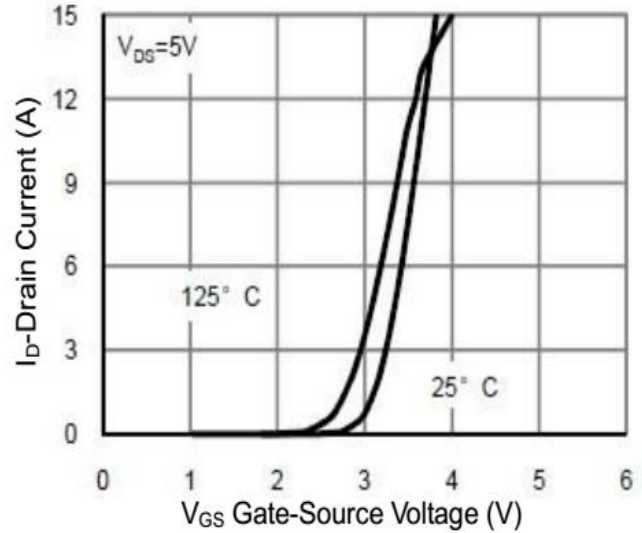


Figure3. On-Resistance vs. Drain Current and Gate Voltage

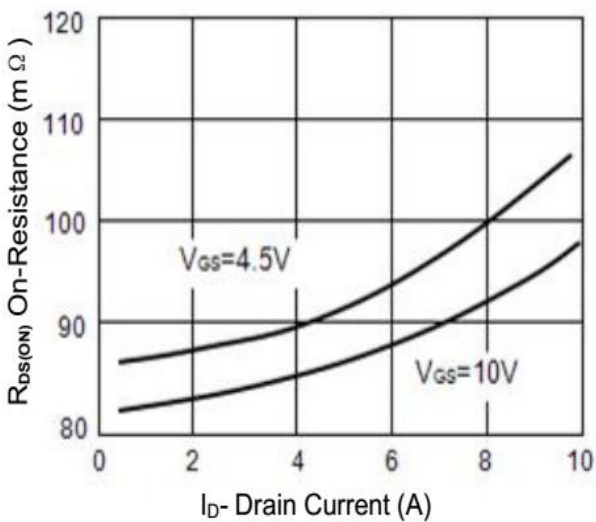
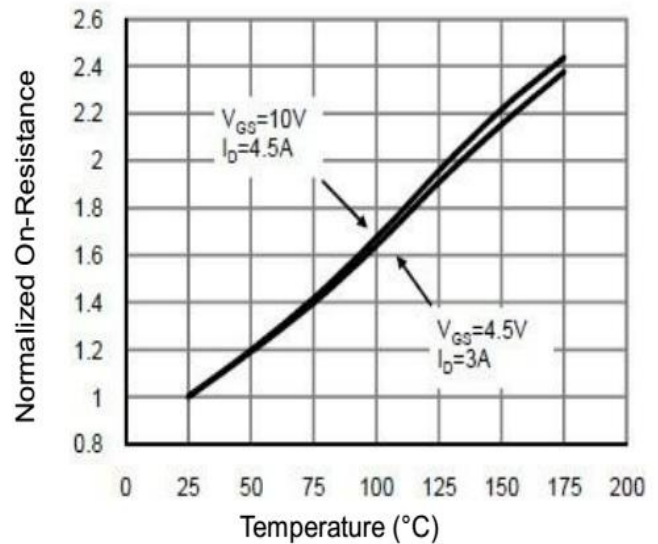


Figure4. On-Resistance vs. Junction Temperature



Typical Characteristics Diagrams

Figure5. On-Resistance vs. Gate-Source Voltage

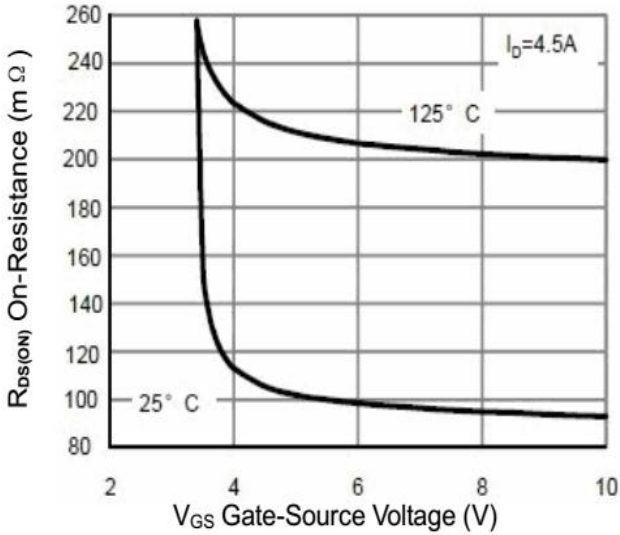


Figure6. Body-Diode Characteristics

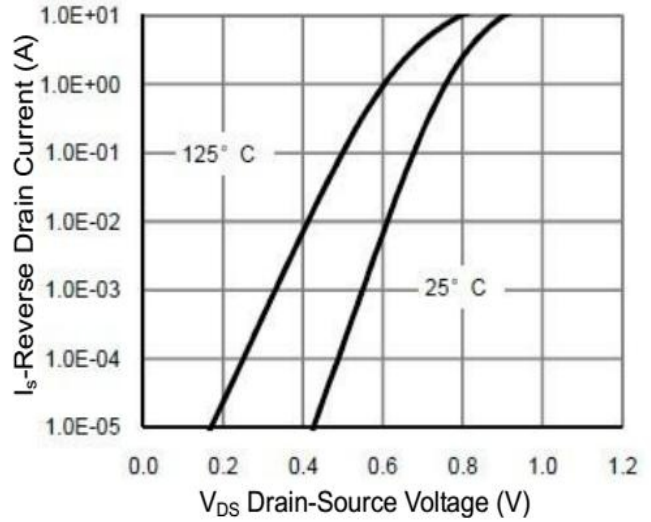


Figure7. Gate-Charge Characteristics

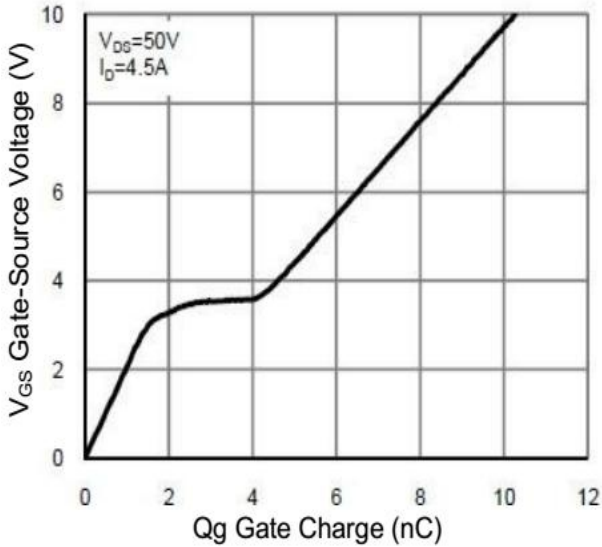
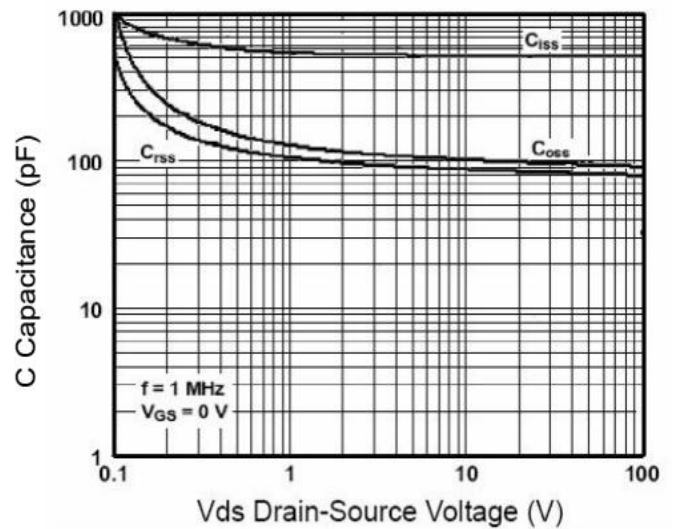


Figure 8. Capacitance Characteristics



Typical Characteristics Diagrams

Figure 9. Maximum Forward Biased Safe Operating Area

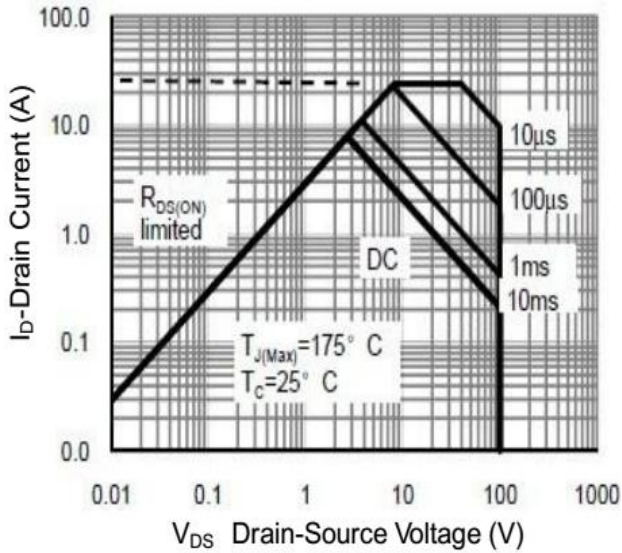


Figure 10. Single Pulse Power Rating Junction-to-Case

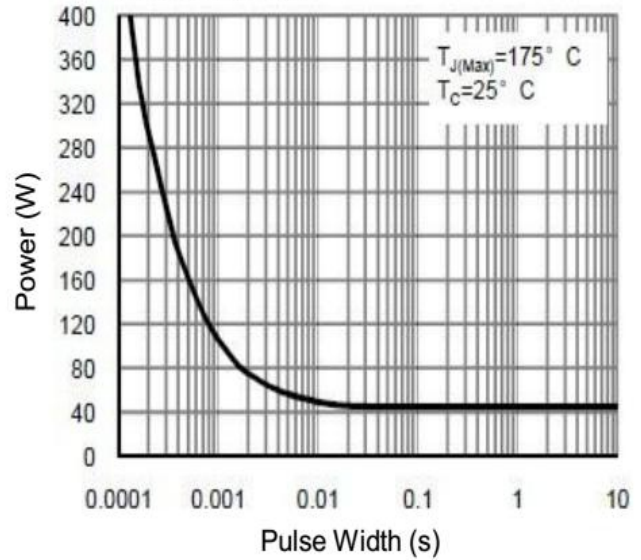
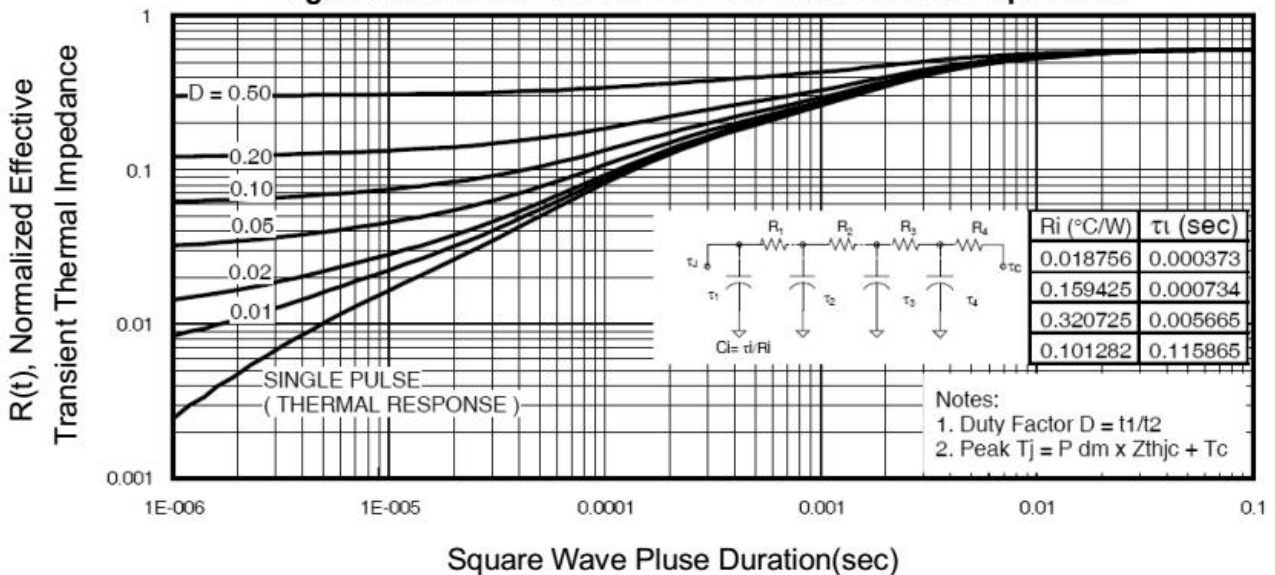
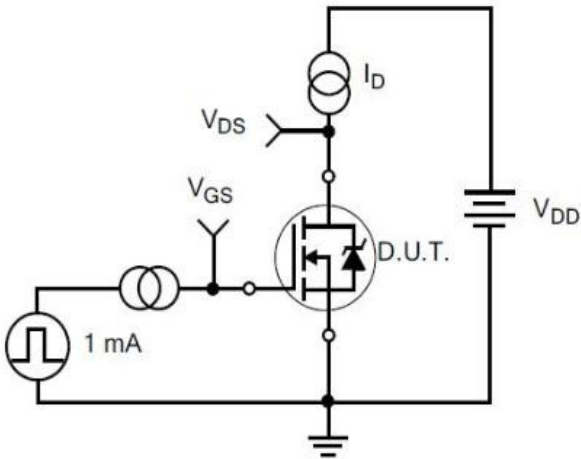


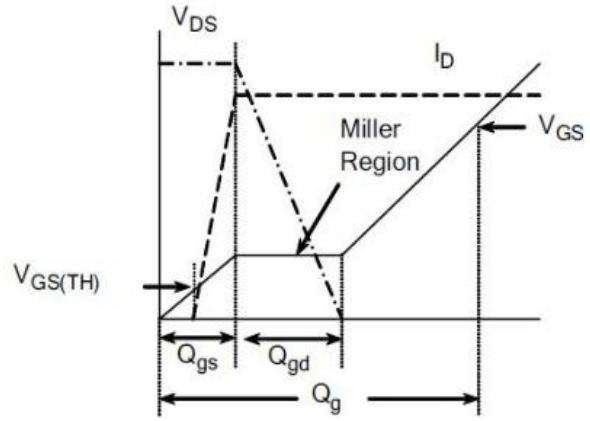
Figure 11. Normalized Maximum Transient Thermal Impedance



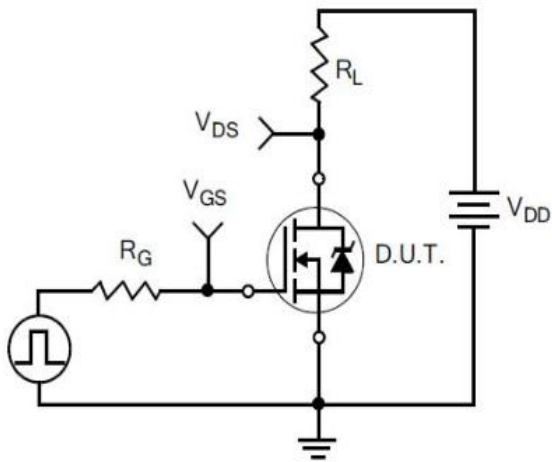
Typical Test Circuit



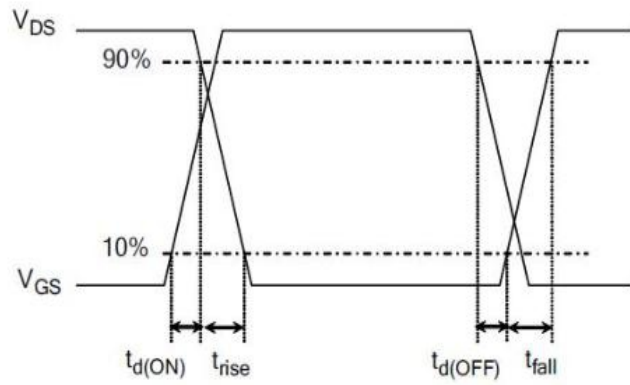
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

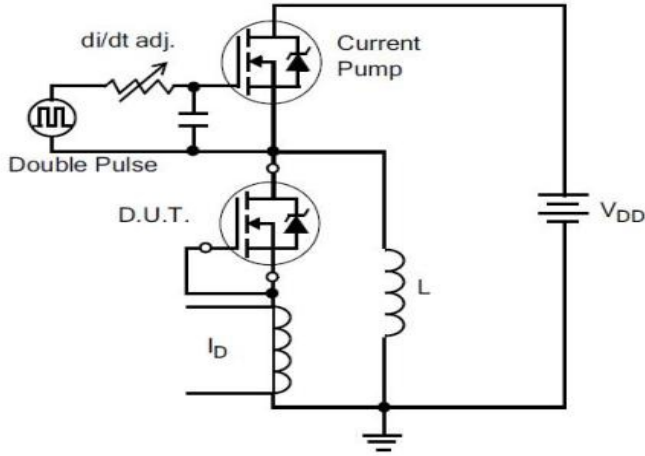


3) Resistive Switching Test Circuit

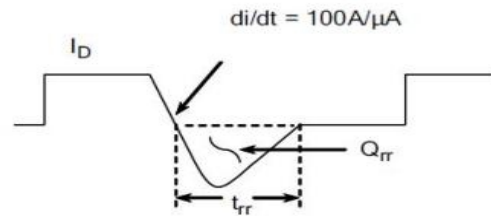


4) Resistive Switching Waveforms

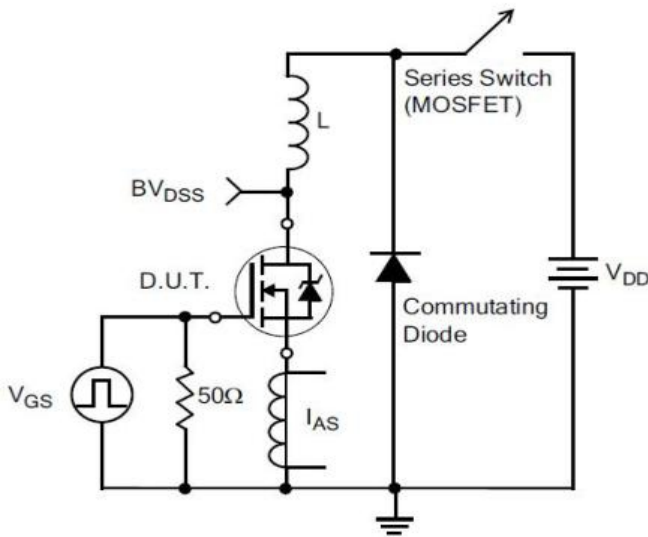
Typical Test Circuit



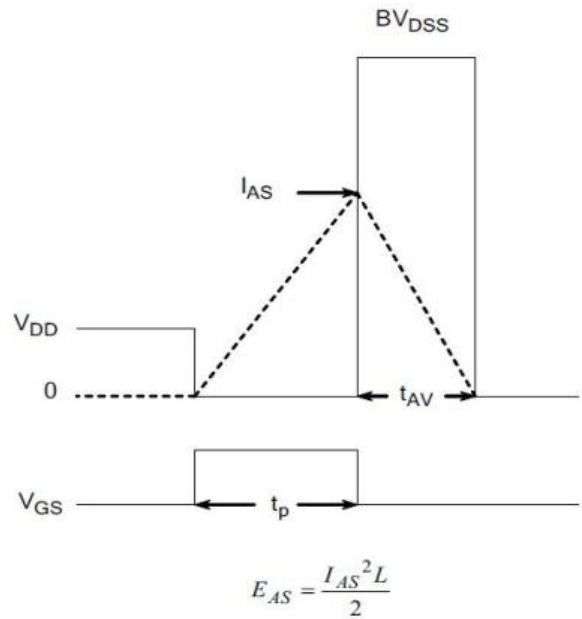
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform

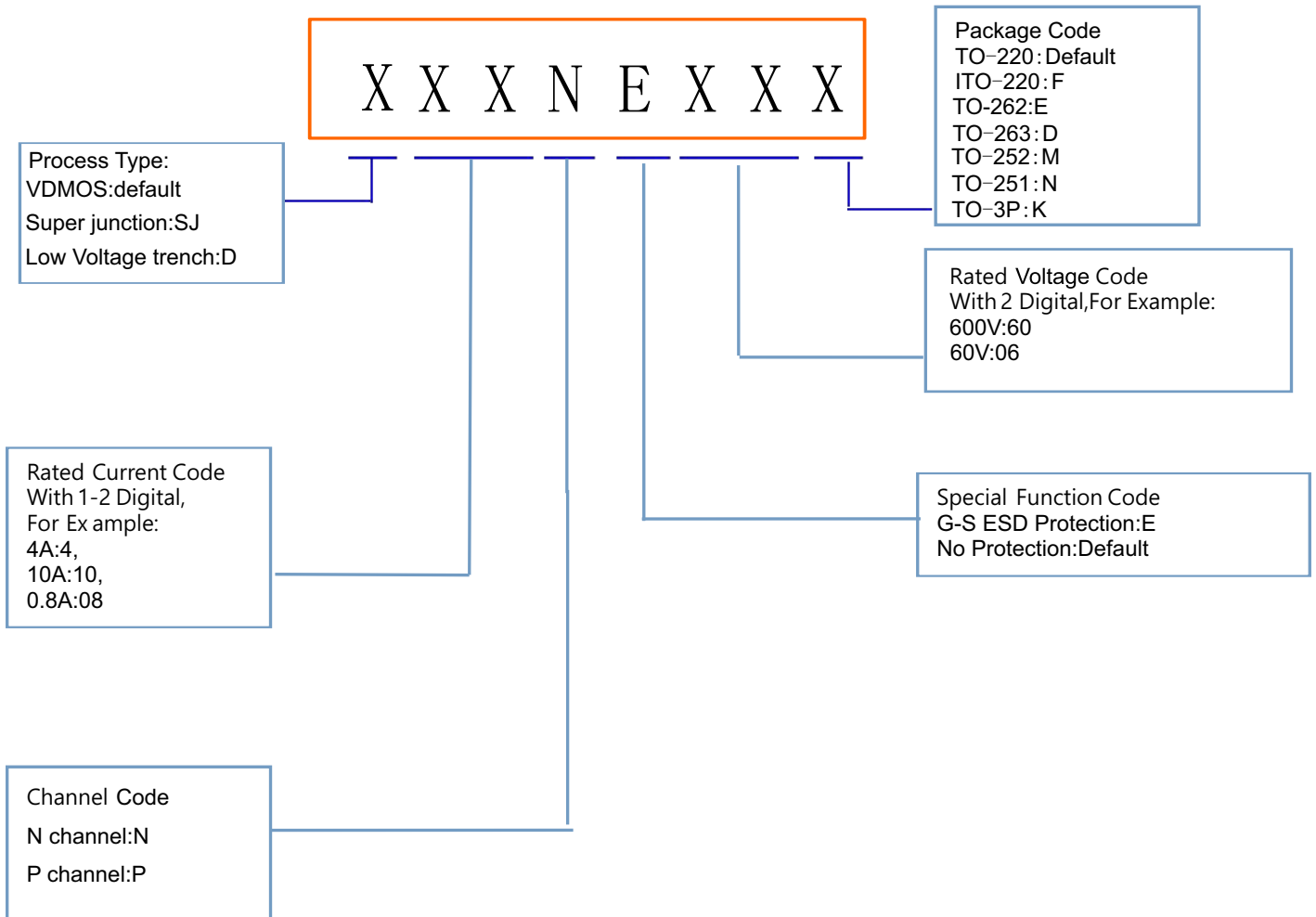


7) . Unclamped Inductive Switching Test Circuit



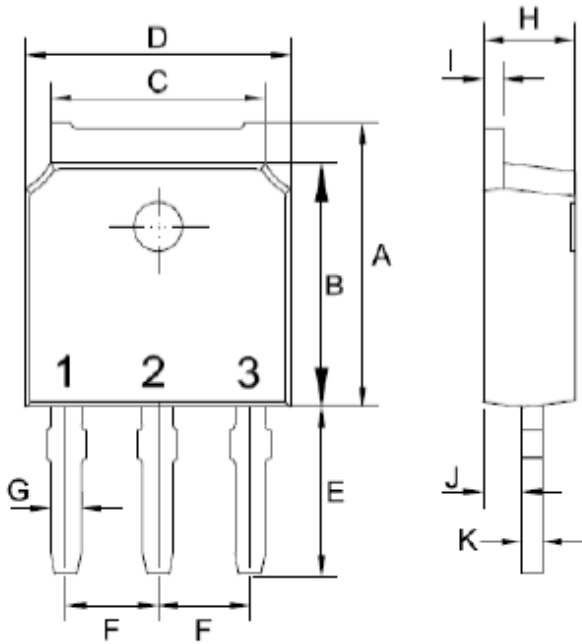
8) Unclamped Inductive Switching Waveforms

Product Names Rules



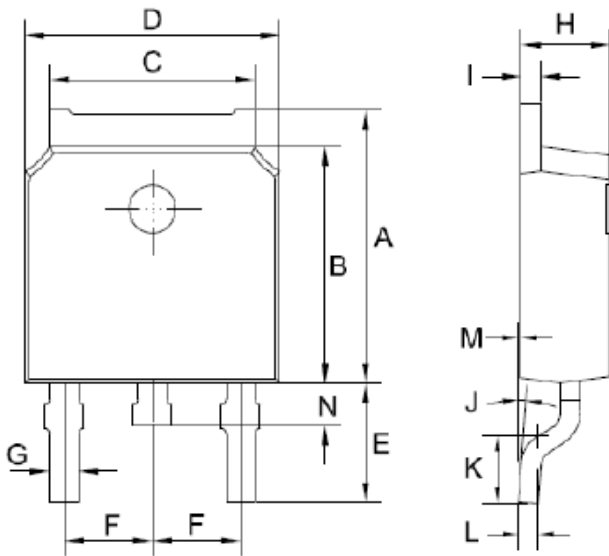
Dimensions

TO-251 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	3.5	4.35	0.138	0.171
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0.71	1.31	0.028	0.052
K	0.41	0.61	0.016	0.024

TO-252 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	2.6	3.3	0.102	0.130
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0°	8°	0°	8°
K	1.45	1.85	0.057	0.073
L	0.41	0.61	0.016	0.024
M	0	0.12	0.000	0.005
P	0.6	1	0.024	0.039

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