

Features

- Uses advanced SGT technology
- Extremely low on-resistance RDS(on)
- Excellent gate charge x RDS(on) product(FOM)

Product Summary			
V _{DS}	R _{DS(on)} (mΩ) Typ	I _D (A)	Q _g (Typ)
80V	5.3 @ 10V 50A	80	56.6nc

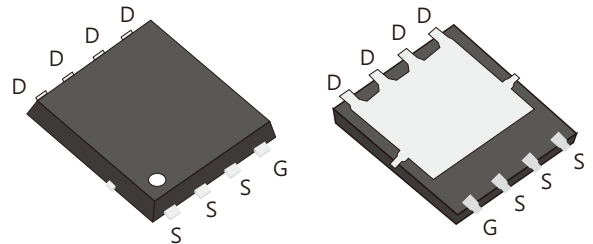
Mechanical Data

- Case:DFN5×6 Package

DFN5×6
D067N08G

Application

- Motor Drives
- SR (Synchronous rectification)
- DC/DC converter
- General purpose applications



Ordering Information

Part No.	Package Type	Package	Quality(box)
D067N08G	DFN5×6	Tape & Reel	5000

Block Diagram

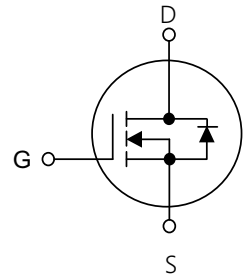


Table1 Absolute Maximum Ratings (T_c=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	80	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _c =25°C	80
		T _c =100°C	70
Pulsed Drain Current (Note 1)	I _{DM}	400	A
Single Pulse Avalanche Energy(Note 2)	E _{AS}	484	mJ
Power Dissipation T _c =25°C	P _D	220	W
Operating Junction and Storage Temperature	T _J /T _{STG}	-55~+150	°C

Table 2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	65	$^{\circ}C/W$
Thermal resistance Junction to Case	$R_{\theta JC}$	0.76	$^{\circ}C/W$

Table 3. Electrical Characteristics ($T_J=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA	
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Reverse	I_{GSS}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	2.9	4.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$	-	5.3	6.7	m Ω	
Dynamic Characteristics(Note 4)							
Input Capacitance	C_{ISS}	$V_{DS}=40V, V_{GS}=0V, f=1MHz$	-	3633	-	pF	
Output Capacitance	C_{OSS}		-	580	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	28	-	pF	
Gate Resitance	R_G	$V_{DD}=0V, V_{GS}=0V, f=1MHz$	-	1.3	-	Ω	
Switching Characteristics (Note 4)							
Turn-On Delay Time	$t_d(on)$	$V_{DS}=40V, V_{GS}=10V, R_L=3\Omega,$	-	17.3	-	ns	
Turn-On Rise Time	t_r		-	33	-	ns	
Turn-Off Delay Time	$t_d(off)$		-	38.9	-	ns	
Turn-Off Fall Time	t_f		-	18.1	-	ns	
Total Gate Charge	Q_G	$V_{DS}=40V, I_D=25A, V_{GS}=10V$	-	56.6	-	nC	
Gate-Source Charge	Q_{GS}		-	21.4	-	nC	
Gate-Drain Charge	Q_{GD}		-	12.5	-	nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=50A$	-	0.85	1.2	V	
Maximum Continuous Drain-Source Diode Forward Current	I_S		-	-	80	A	
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_F=20A, dI_F/dt=500A/\mu s$	-	68	-	ns	
Reverse Recovery Charge	Q_{RR}		-	66	-	nC	

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature

2 $L=0.5mH, R_G=25\Omega, Starting T_J=25^{\circ}C$

3 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1. Output Characteristics

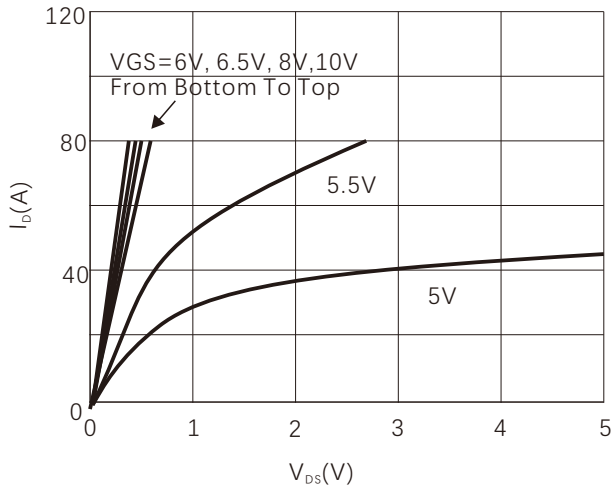


Figure 2. Normalized $R_{DS(ON)}$ vs Temperature

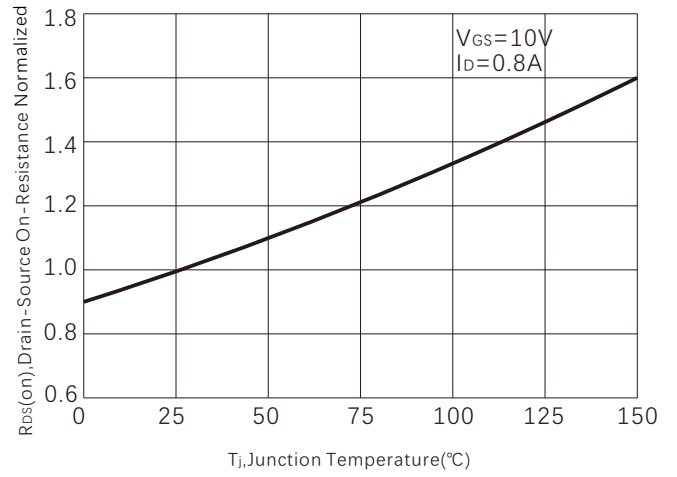


Figure 3. On-Resistance vs. Drain Current

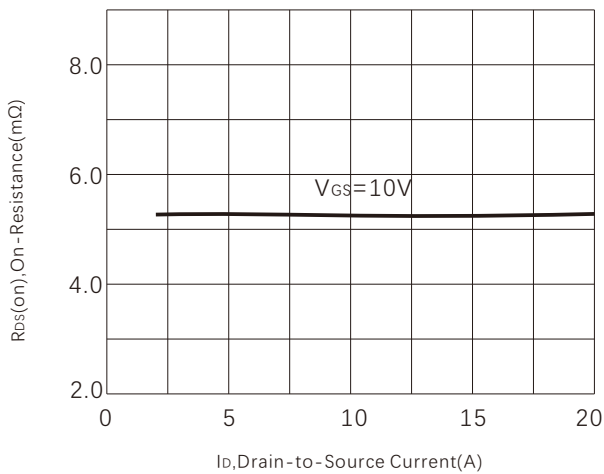


Figure 4. Capacitance

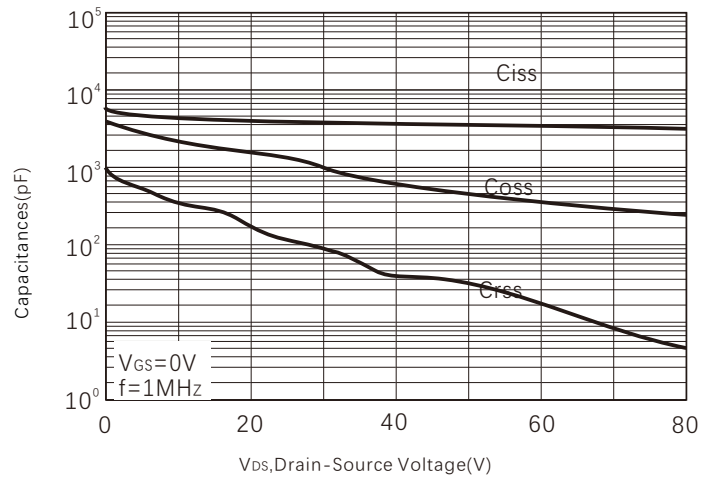


Figure 5. Gate charge

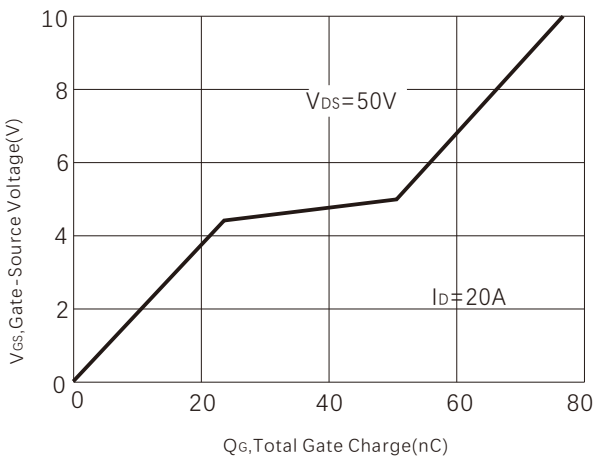


Figure 6. Source-Drain Diode Forward Voltage

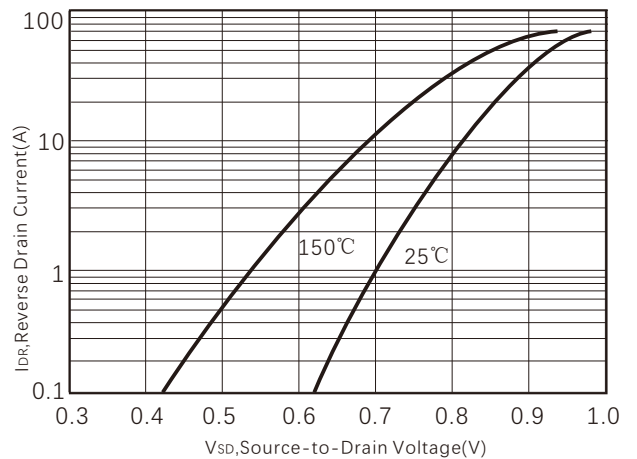


Figure 7. Maximum Drain Current vs Temperature

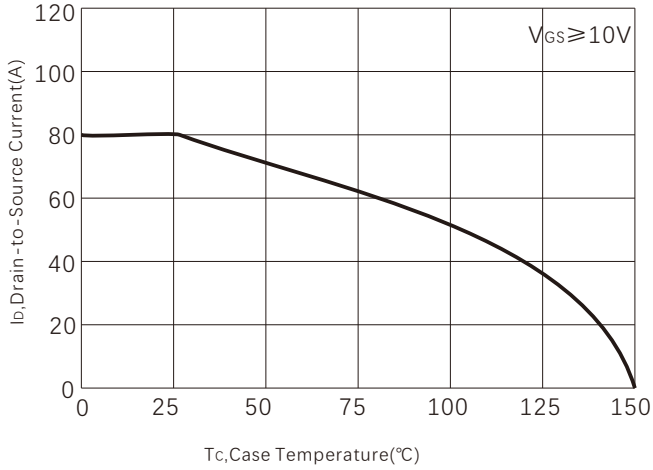


Figure 8. Transfer Characteristics

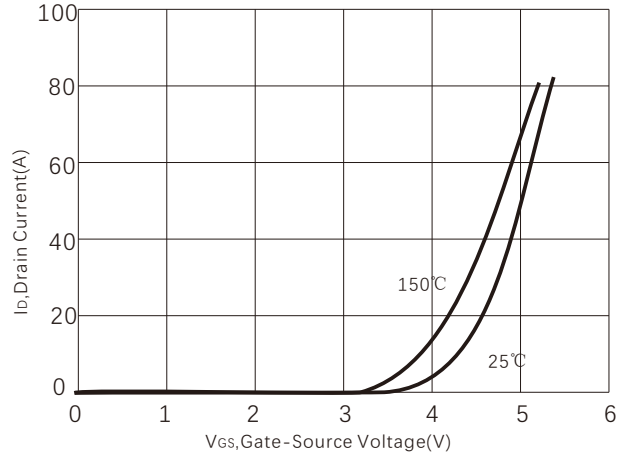


Figure 9. Safe operating area

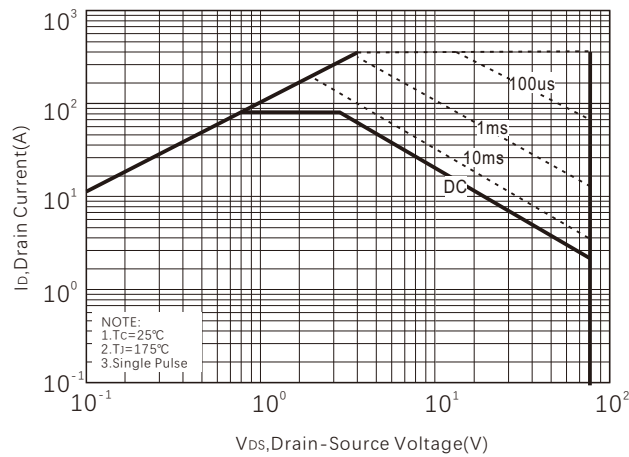
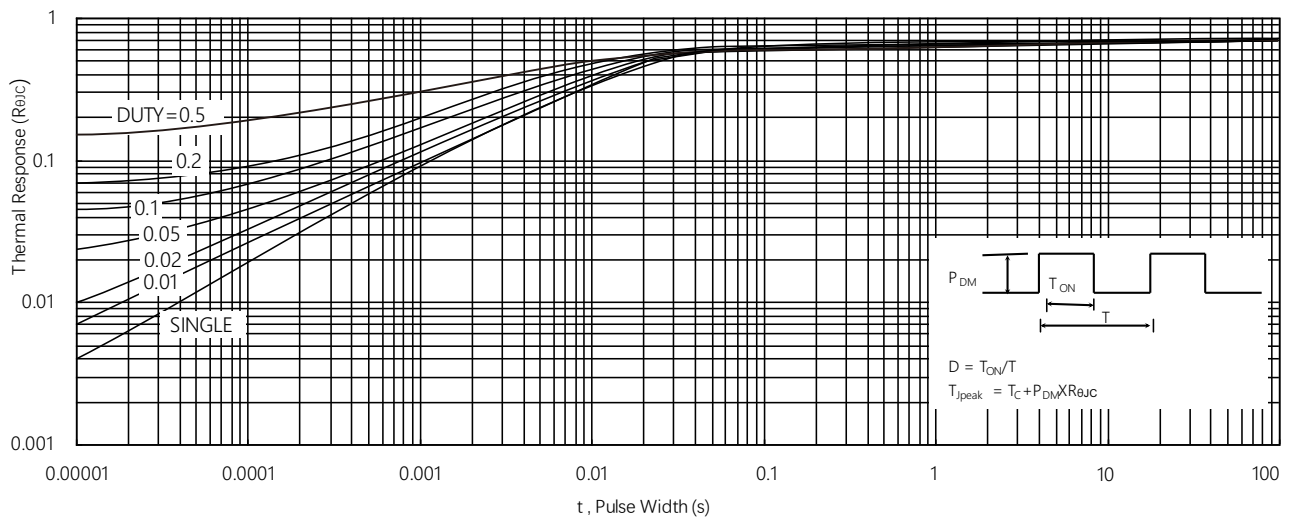
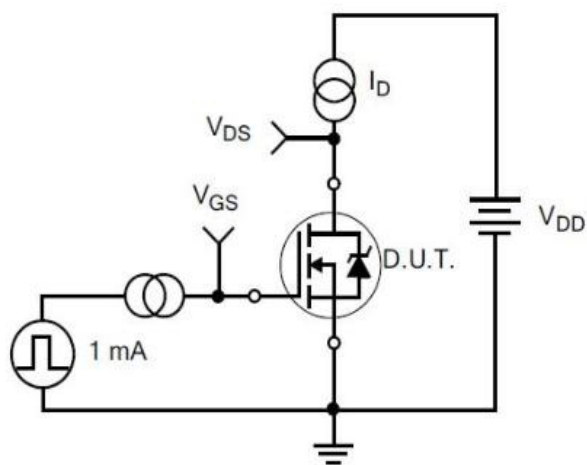


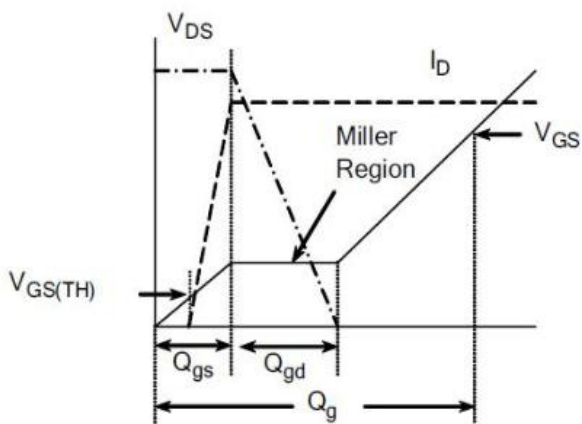
Figure 10. Maximum Transient Thermal Impedance



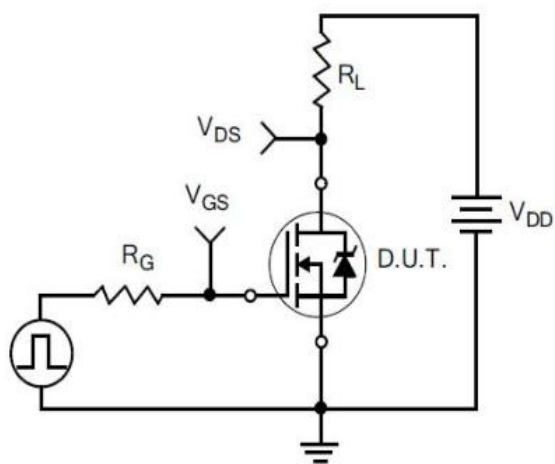
Typical Test Circuit



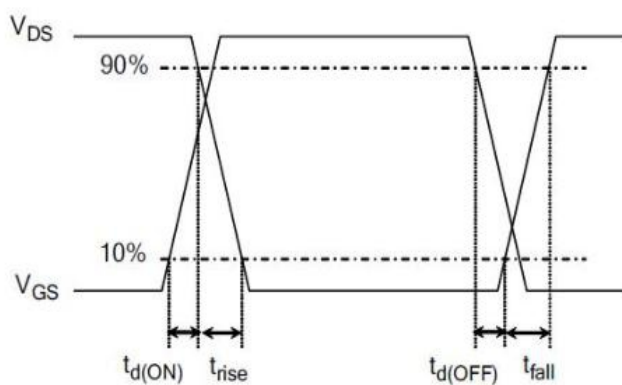
1) Gate Charge Test Circuit



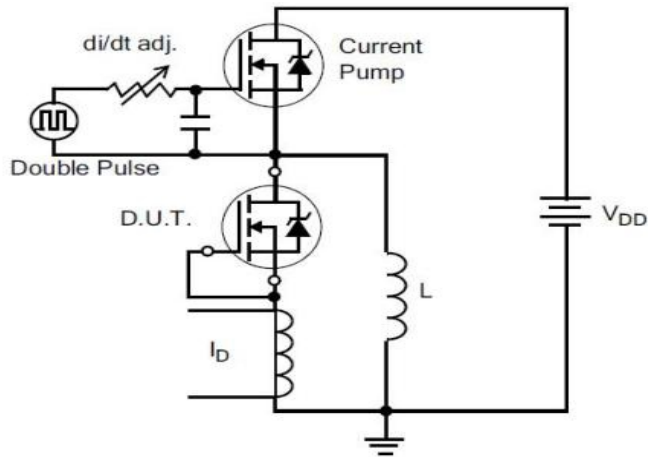
2) Gate Charge Waveform



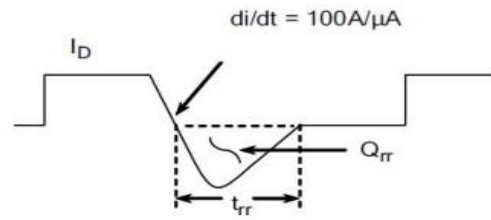
3) Resistive Switching Test Circuit



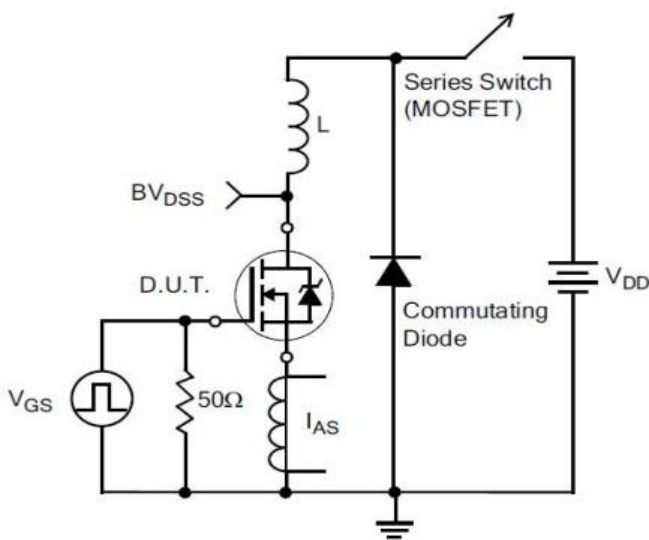
4) Resistive Switching Waveforms



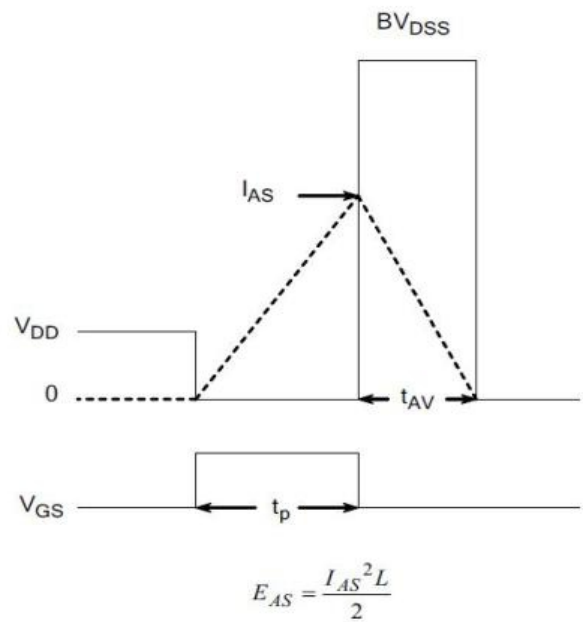
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



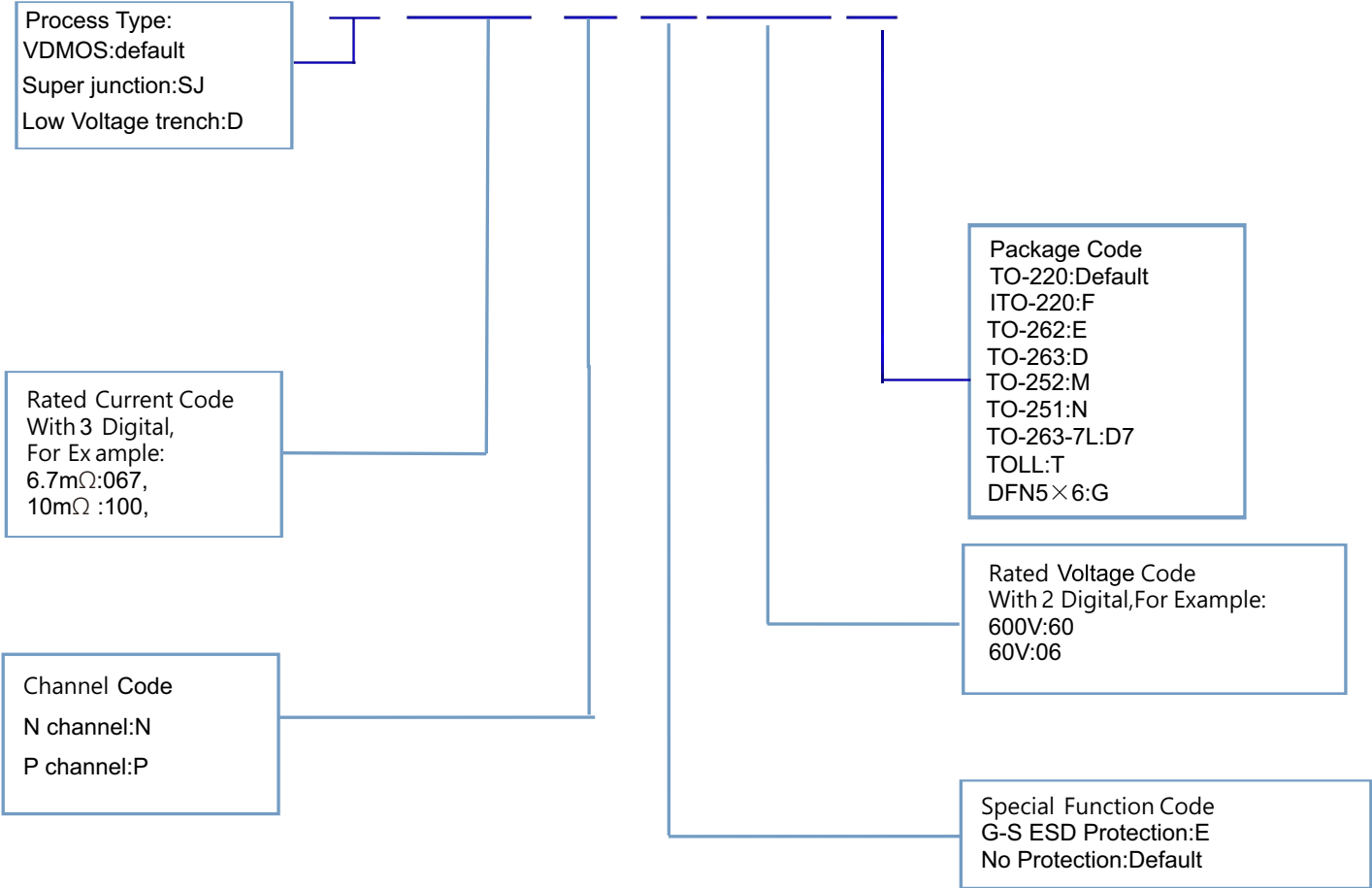
7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

Product Names Rules

X X X X N E X X X



Dimensions

DFN5×6 PACKAGE OUTLINE DIMENSIONS

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