

Features

- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

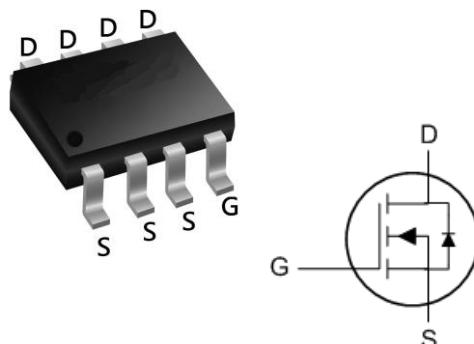
BVDSS	RDS(on)	ID
100V	152mΩ	2 A

Description

The JHS0014 is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The JHS0014 meet the RoHS and Green Product requirement with full function reliability approved.

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	2	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.6	A
I_{DM}	Pulsed Drain Current ²	4	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation ³	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	85	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	40	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	100	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.122	---	$\text{V}/^\circ\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=2\text{A}$	---	125	152	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=1\text{A}$	---	130	158	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$\Delta V_{\text{GS}(\text{th})}$	$V_{\text{GS}(\text{th})}$ Temperature Coefficient		---	-4.84	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	10	uA
		$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=2\text{A}$	---	10.2	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	2.3	4.6	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=2\text{A}$	---	25.5	---	nC
Q_{gs}	Gate-Source Charge		---	4.2	---	
Q_{gd}	Gate-Drain Charge		---	4.3	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$	---	17.3	---	ns
T_r	Rise Time		---	2.8	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	50	---	
T_f	Fall Time		---	2.8	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1077	---	pF
C_{oss}	Output Capacitance		---	46	---	
C_{rss}	Reverse Transfer Capacitance		---	32	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	2	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	4	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$		---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.

Typical Characteristics

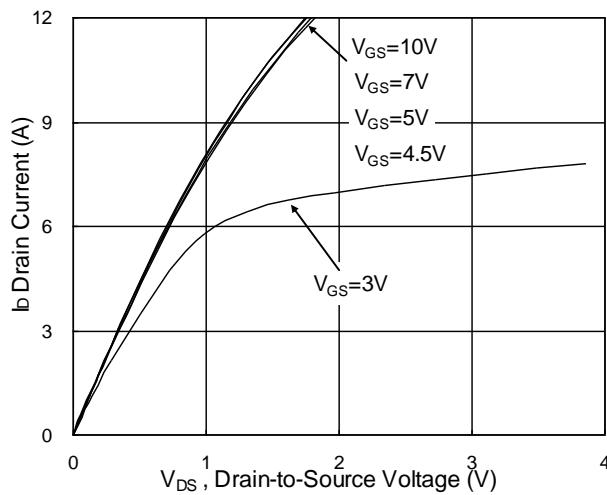


Fig.1 Typical Output Characteristics

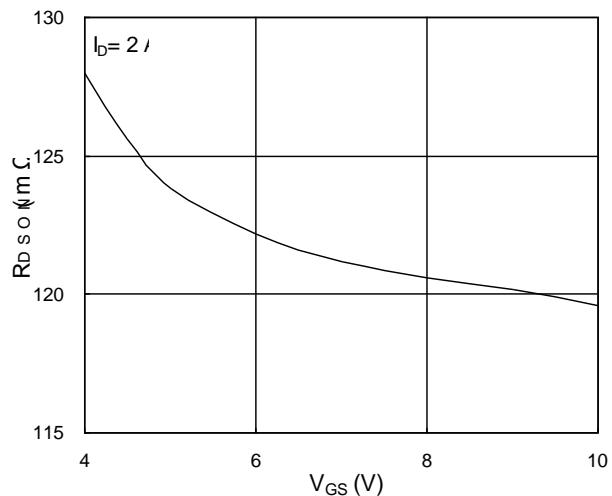


Fig.2 On-Resistance vs. Gate-Source

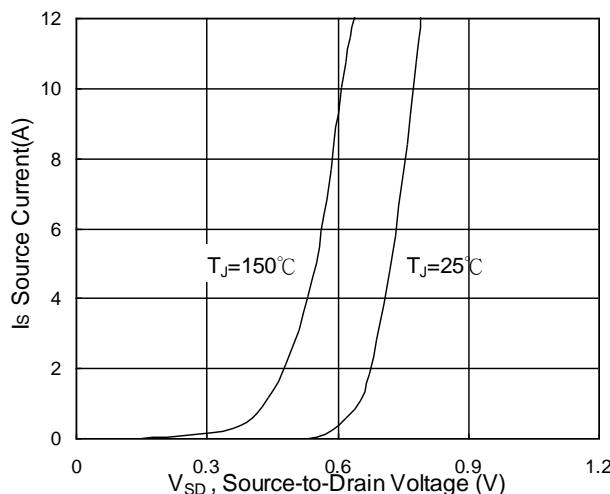


Fig.3 Forward Characteristics Of Reverse

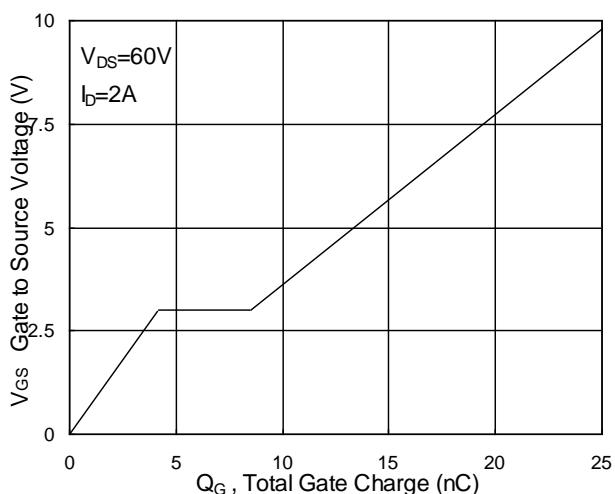


Fig.4 Gate-Charge Characteristics

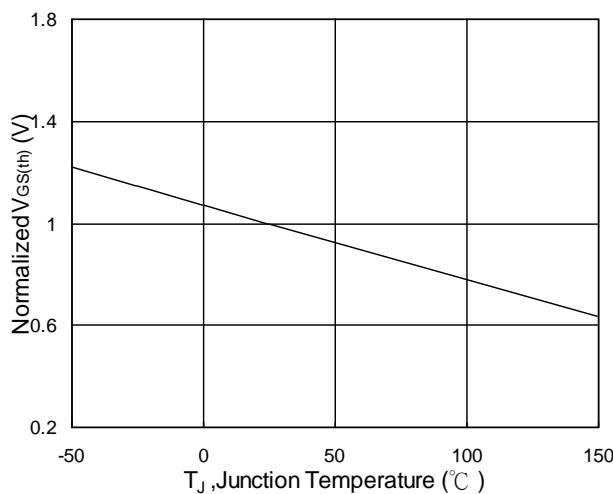


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

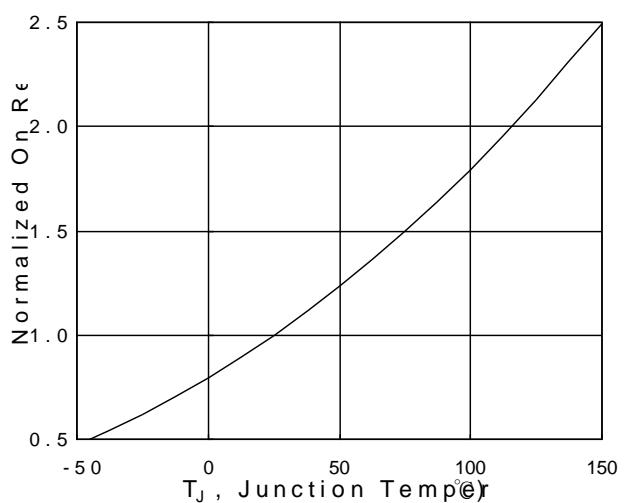
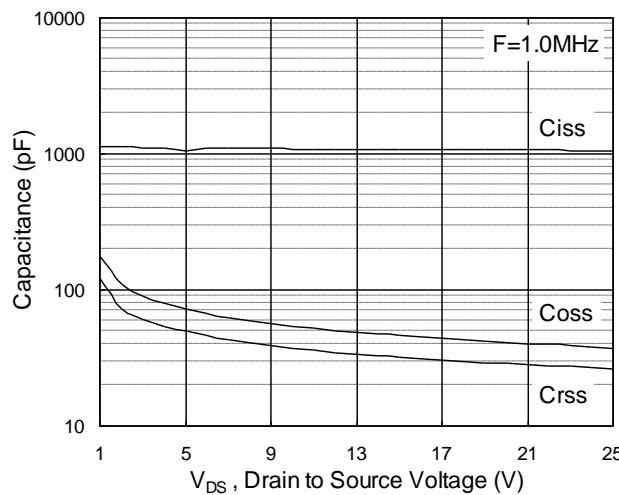
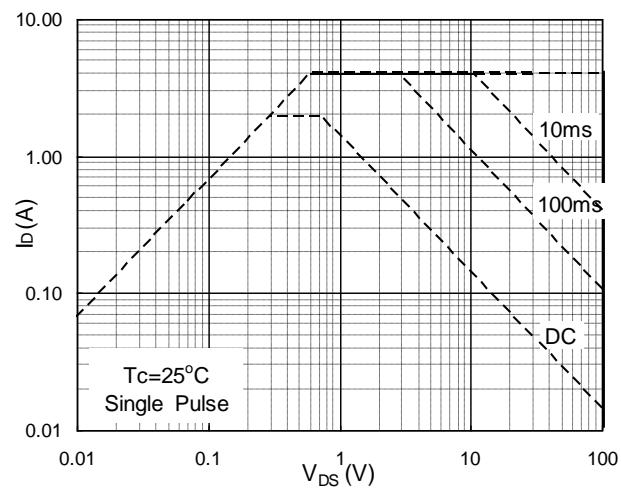
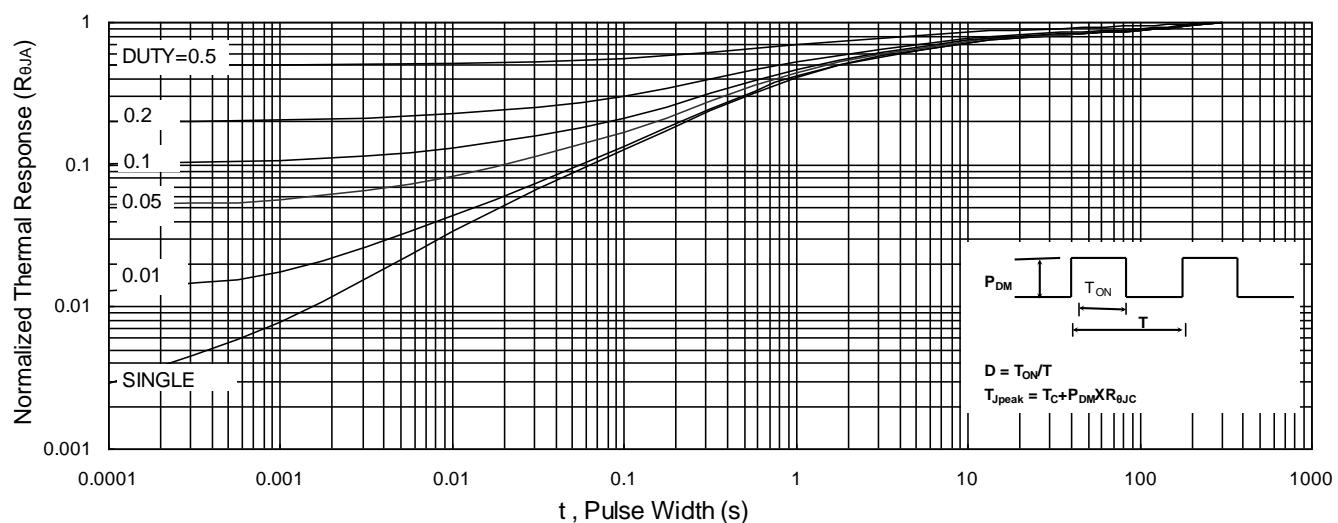
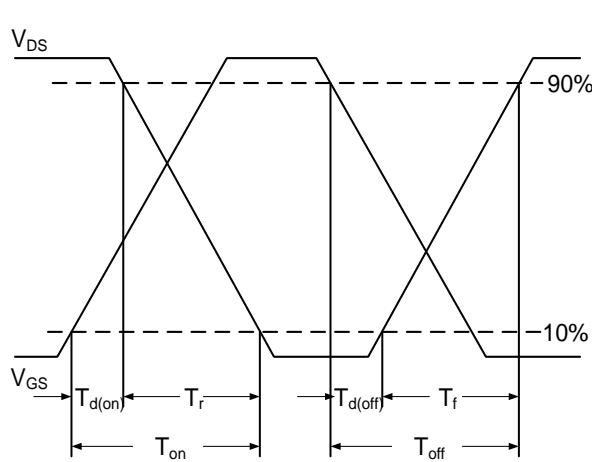
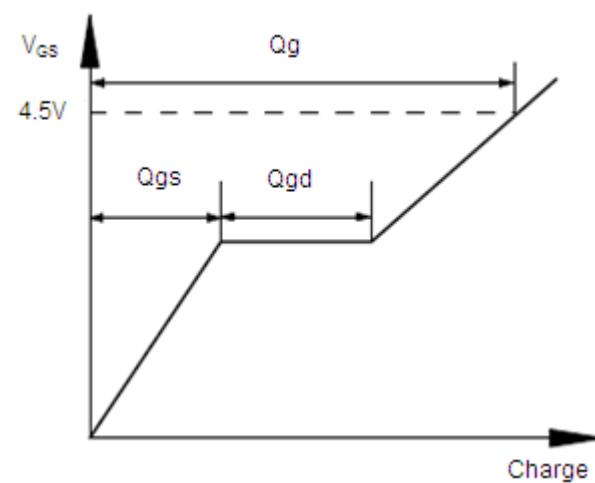
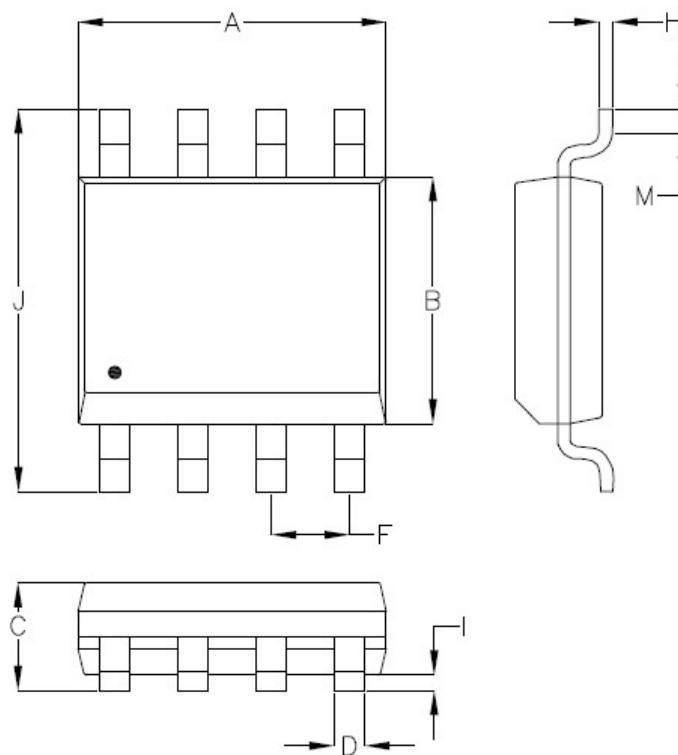


Fig.6 Normalized R_{DSON} vs. T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform

SOP-8L Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.700	5.150	0.185	0.203
B	3.700	4.100	0.146	0.161
C	1.23	1.753	0.048	0.069
D	0.310	0.510	0.012	0.020
F	1.070	1.470	0.042	0.058
H	0.160	0.254	0.006	0.010
I	0.050	0.254	0.002	0.010
J	5.750	6.250	0.226	0.246
M	0.400	1.270	0.016	0.050

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