

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

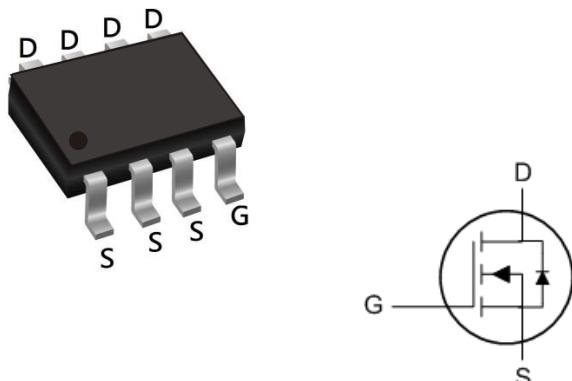
BVDSS	RDS(ON)	ID
60V	8.5mΩ	13A

Description

The JHS6032 is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

The JHS6032 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	13	A
I _D @T _A =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	8	A
I _{DM}	Pulsed Drain Current ²	60	A
EAS	Single Pulse Avalanche Energy ³	80	mJ
I _{AS}	Avalanche Current	40	A
P _D @T _A =25°C	Total Power Dissipation ⁴	2.7	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹ (t≤10S)	---	45	°C/W
	Thermal Resistance Junction-ambient ¹ (Steady State)	---	80	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	60	---	---	V
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=10\text{A}$	---	---	8.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=8\text{A}$	---	---	12	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=10\text{A}$	---	50	---	S
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=10\text{A}$	---	57	---	nC
Q_{gs}	Gate-Source Charge		---	8.7	---	
Q_{gd}	Gate-Drain Charge		---	14	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=10\text{A}$	---	16.2	---	ns
T_r	Rise Time		---	41.2	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	56.4	---	
T_f	Fall Time		---	16.2	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=25\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	3307	---	pF
C_{oss}	Output Capacitance		---	201	---	
C_{rss}	Reverse Transfer Capacitance		---	151	---	

Diode Characteristics

I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	10	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	60	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $\text{I}_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$\text{I}_F=10\text{A}$, $d\text{I}/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	24	---	nS
			---	15	---	

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $\text{I}_{\text{AS}}=40\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_s , in real applications , should be limited by total power dissipation.

Typical Characteristics

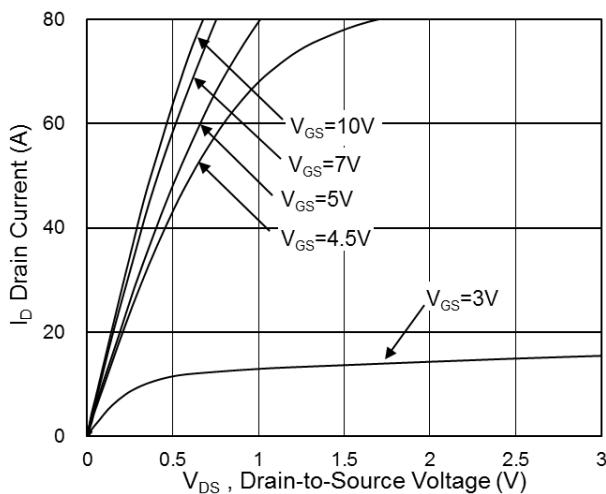


Fig.1 Typical Output Characteristics

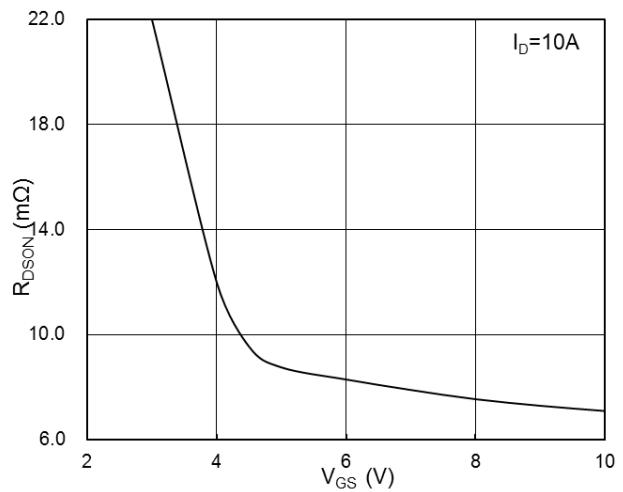


Fig.2 On-Resistance v.s Gate-Source Voltage

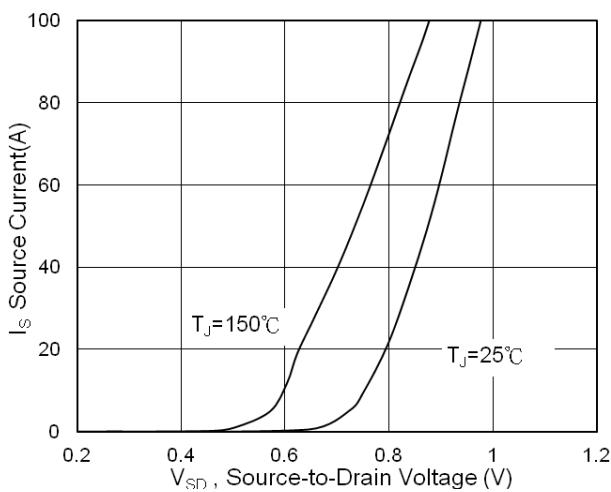


Fig.3 Forward Characteristics of Reverse

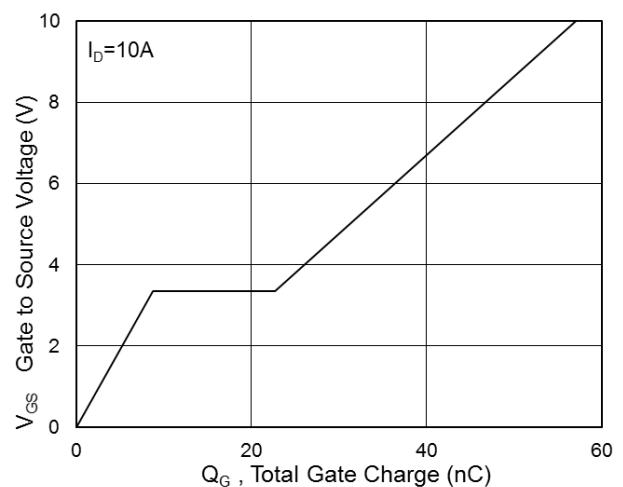


Fig.4 Gate-Charge Characteristics

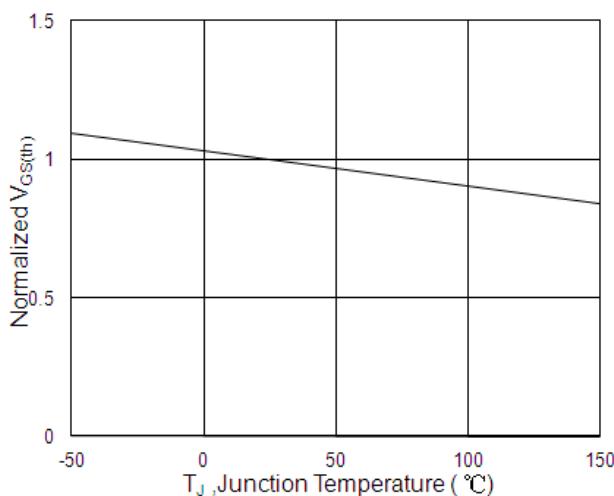


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

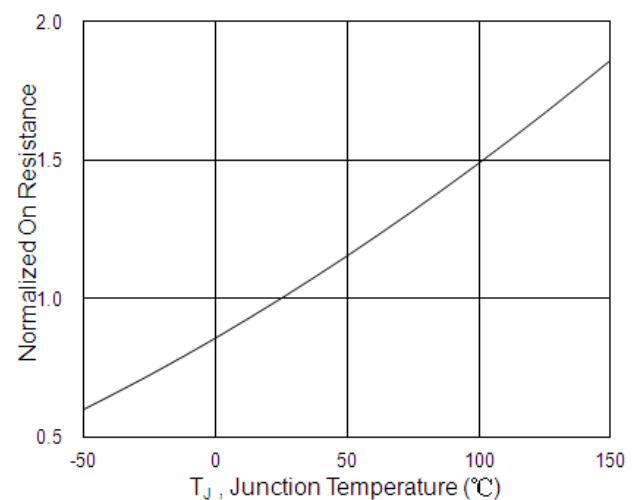
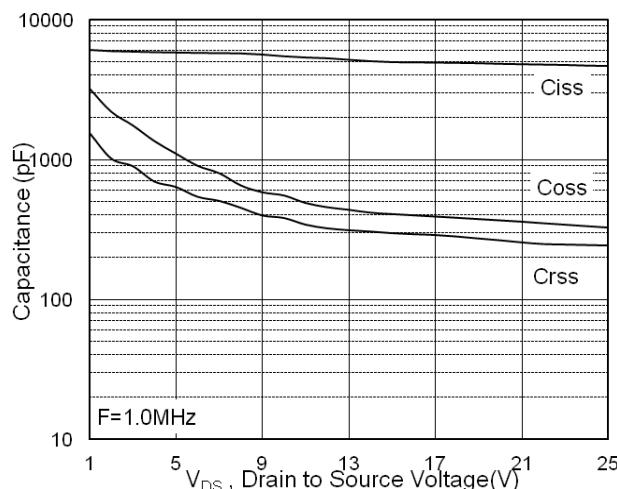
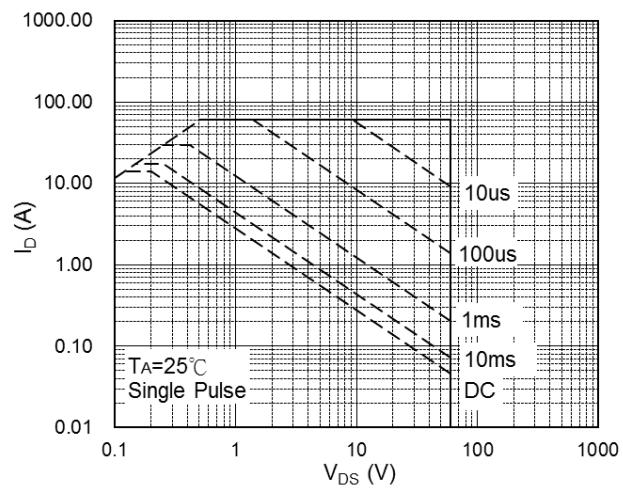
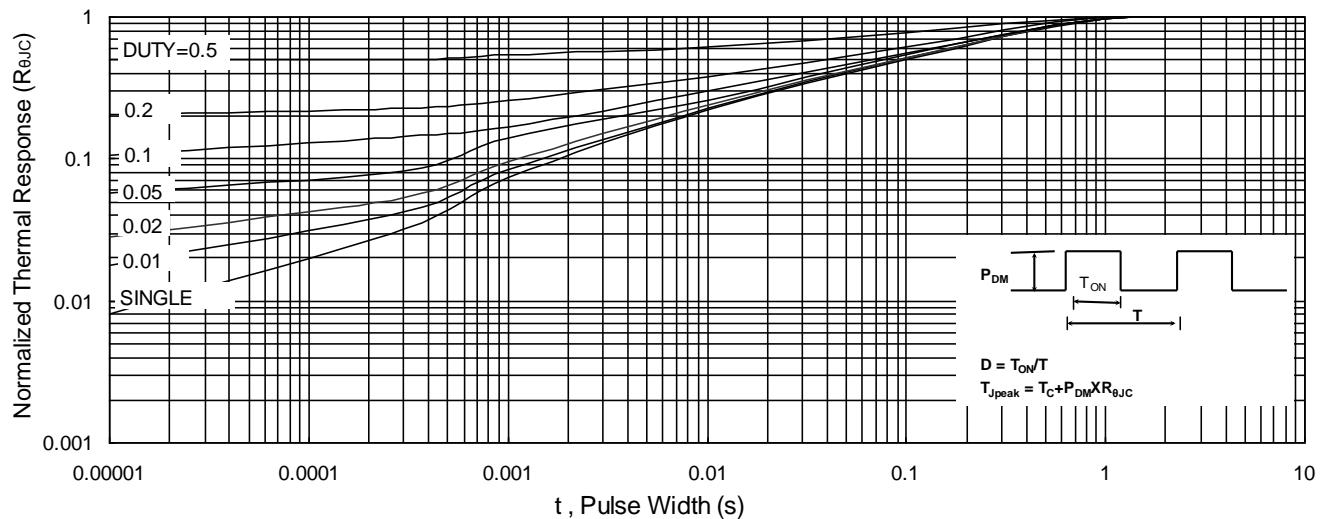
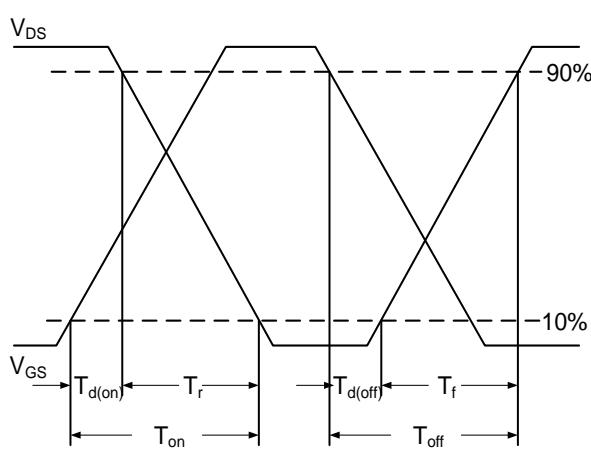
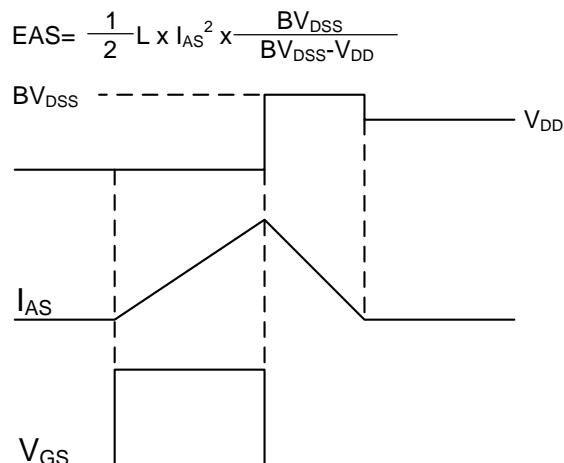
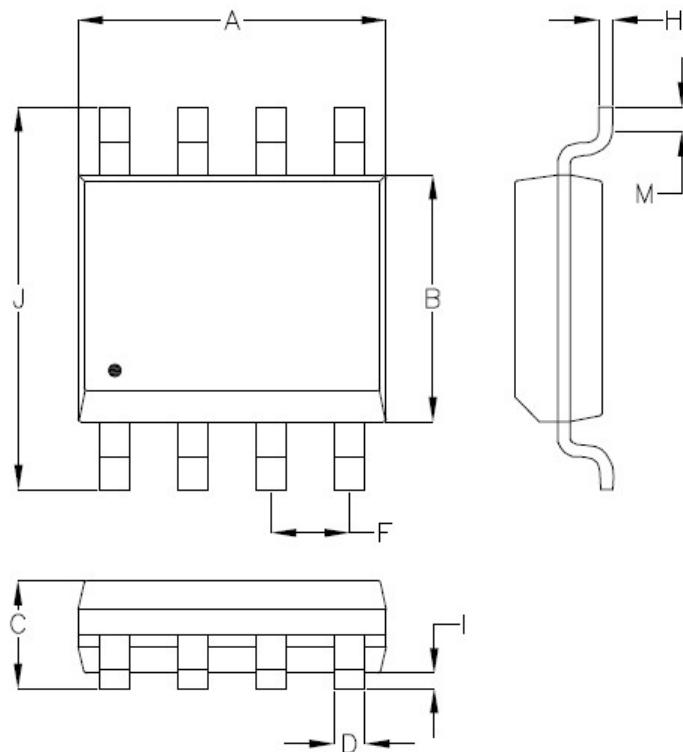


Fig.6 Normalized $R_{DS(on)}$ vs. T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Switching Waveform

SOP-8L Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.700	5.150	0.185	0.203
B	3.700	4.100	0.146	0.161
C	1.23	1.753	0.048	0.069
D	0.310	0.510	0.012	0.020
F	1.070	1.470	0.042	0.058
H	0.160	0.254	0.006	0.010
I	0.050	0.254	0.002	0.010
J	5.750	6.250	0.226	0.246
M	0.400	1.270	0.016	0.050

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