

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Excellent CdV/dt effect decline
- Green Device Available
- Advanced high cell density Trench technology

Product Summary

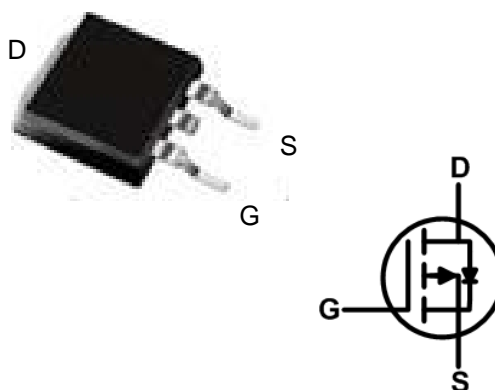
BVDSS	RDSON	ID
-40V	13mΩ	-52A

Description

The D52P04M is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The D52P04M meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-52	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-32	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-8	A
I_{DM}	Pulsed Drain Current ²	-105	A
EAS	Single Pulse Avalanche Energy ³	146	mJ
I_{AS}	Avalanche Current	-54	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	52.1	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.4	$^\circ C/W$

D52P04M

Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.023	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-18A$	---	10.5	13	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-12A$	---	15	20	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-18A$	---	24	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	7	14	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-12A$	---	27.9	---	nC
Q_{gs}	Gate-Source Charge		---	7.7	---	
Q_{gd}	Gate-Drain Charge		---	7.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	40	---	ns
T_r	Rise Time		---	35.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	100	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	3500	---	pF
C_{oss}	Output Capacitance		---	323	---	
C_{rss}	Reverse Transfer Capacitance		---	222	---	
Diode Characteristics						
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	-52	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	-105	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-54A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_S , in real applications , should be limited by total power dissipation.

Typical Characteristics

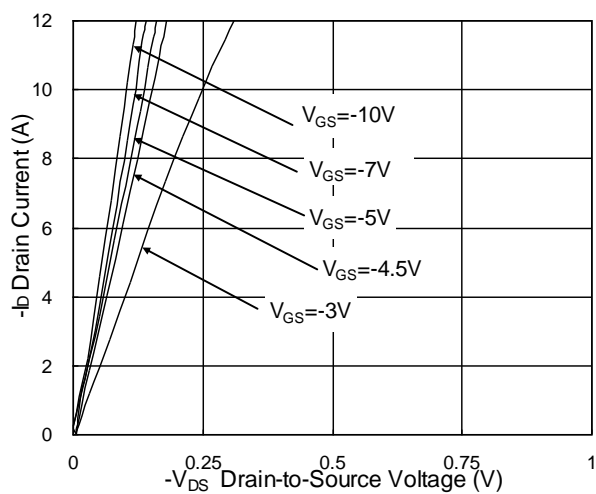


Fig.1 Typical Output Characteristics

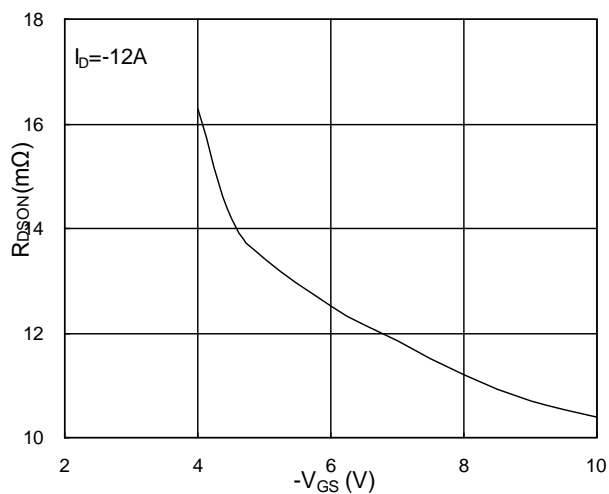


Fig.2 On-Resistance v.s Gate-Source

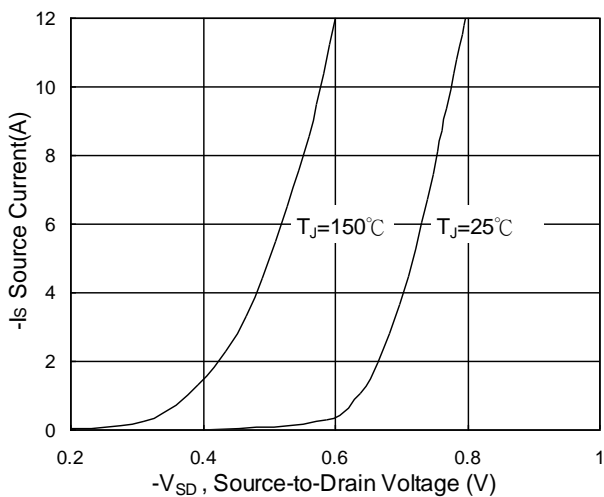


Fig.3 Forward Characteristics Of Reverse

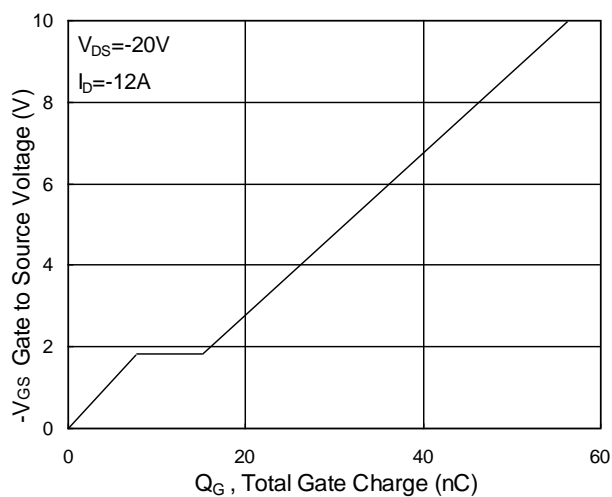


Fig.4 Gate-Charge Characteristics

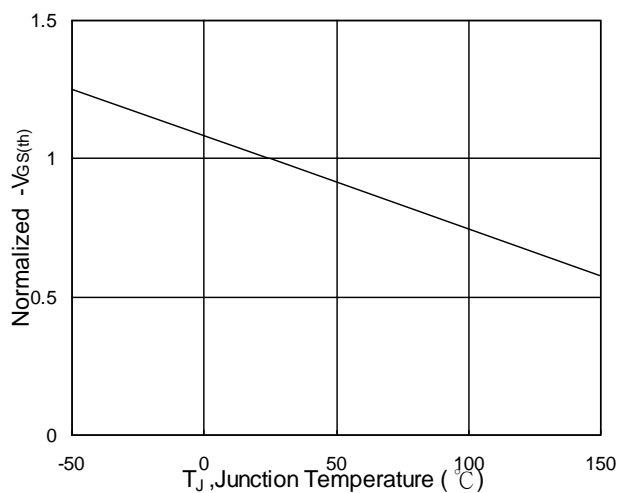


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

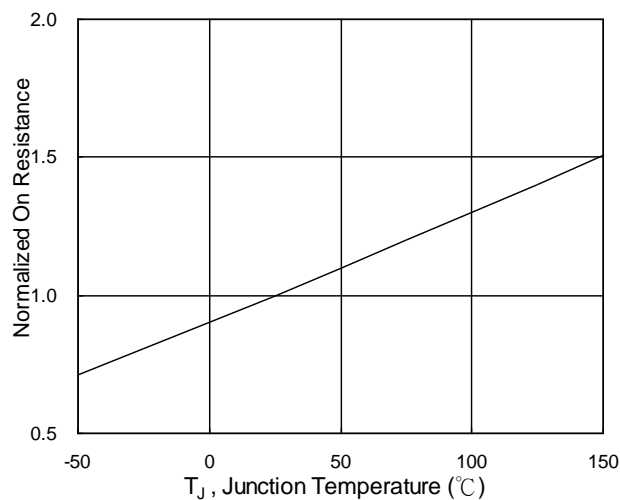


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

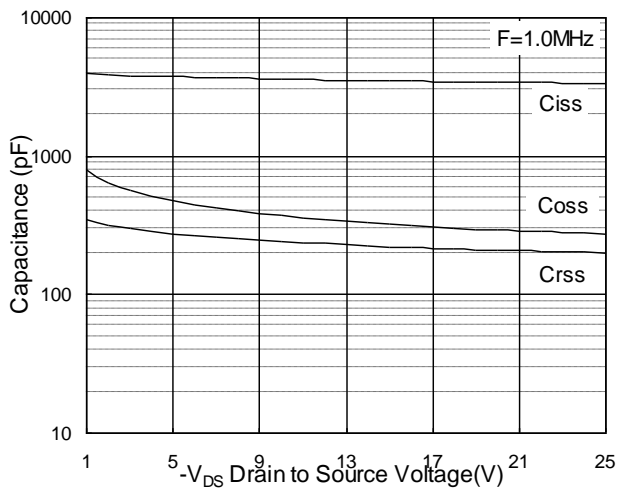


Fig.7 Capacitance

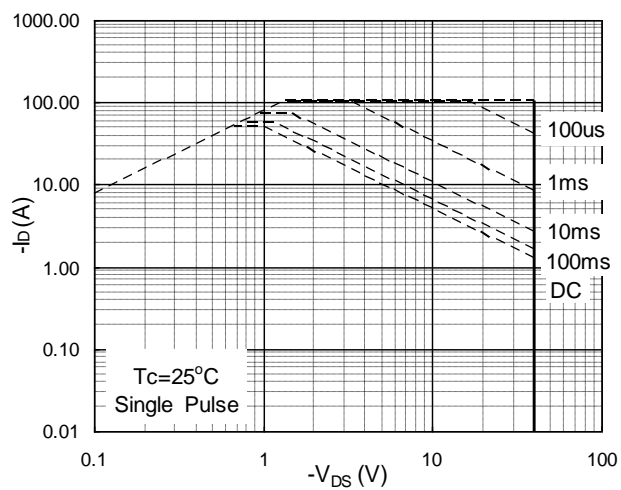


Fig.8 Safe Operating Area

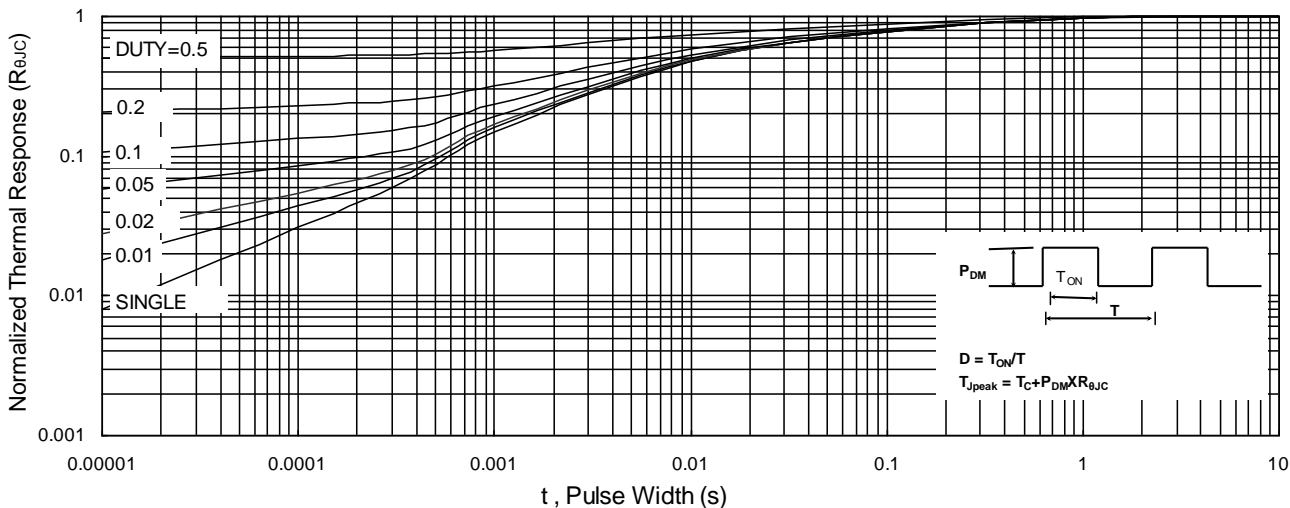


Fig.9 Normalized Maximum Transient Thermal Impedance

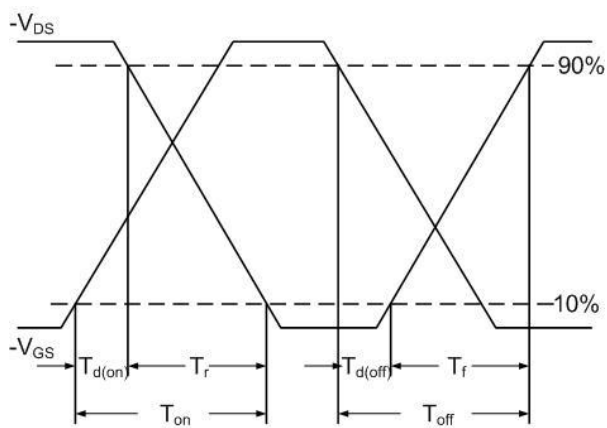


Fig.10 Switching Time Waveform

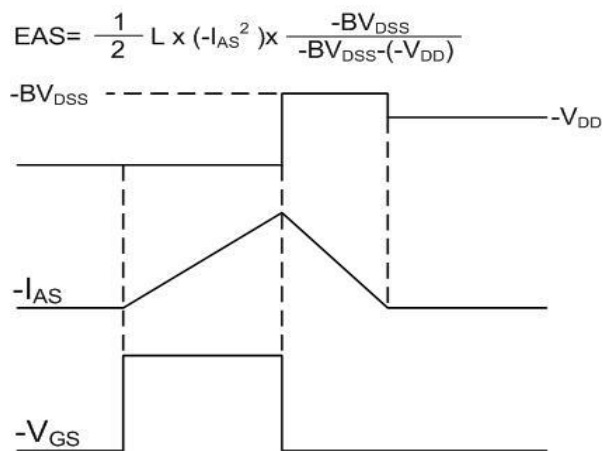
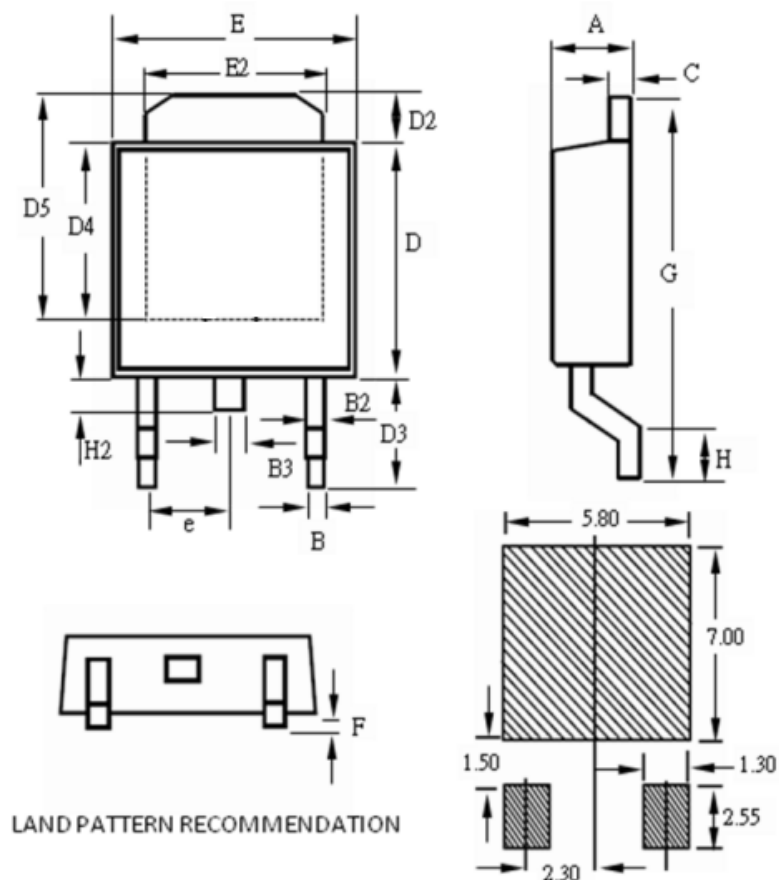


Fig.11 Unclamped Inductive Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$

TO-252 Package Outline



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.10	--	2.50	0.083	--	0.098
B	0.30	--	0.89	0.012	--	0.035
B2	0.40	--	1.14	0.016	--	0.045
B3	0.60	--	1.00	0.024	--	0.039
C	0.40	--	0.89	0.016	--	0.035
D	5.30	--	6.25	0.209	--	0.246
D2	0.50	--	1.70	0.020	--	0.067
D3	2.20	--	3.40	0.087	--	0.134
D4	4.32	--	--	0.170	--	--
D5	5.21	--	--	0.205	--	--
E	6.30	--	6.73	0.248	--	0.265
E2	4.80	--	5.46	0.189	--	0.215
F	0.00	--	0.30	0.000	--	0.012
G	9.20	--	10.41	0.362	--	0.410
H	0.90	--	1.95	0.035	--	0.077
H2	0.50	--	1.10	0.020	--	0.043
e	--	2.30	--	--	0.091	--

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