

### Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Excellent CdV/dt effect decline
- Green Device Available
- Advanced high cell density Trench technology

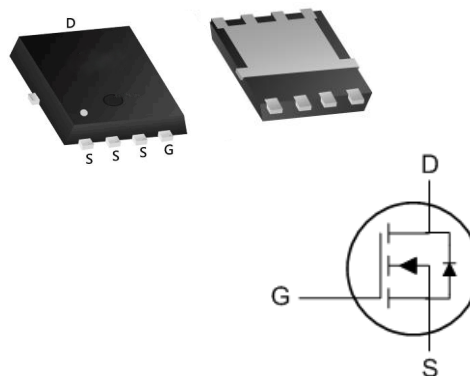
### Product Summary

BVDSS	RDS(on)	ID
60V	20mΩ	33A

### Description

The JHQ6006 is the high cell density trench N-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications. The JHQ6006 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

### DFN3X3 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	33	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	21	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	80	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	39.2	mJ
$I_{AS}$	Avalanche Current	28	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	42	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	75	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	3	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	60	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =8A	---	---	20	mΩ
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =6A	---	---	24	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	---	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =48V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =± 20V , V <sub>DS</sub> =0V	---	---	± 100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =8A	---	45	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz	---	1.7	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =30V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =8A	---	19.3	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	7.1	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	7.6	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V , V <sub>GS</sub> =10V , R <sub>G</sub> =3.3Ω, I <sub>D</sub> =8A	---	7.2	---	ns
T <sub>r</sub>	Rise Time		---	50	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	36.4	---	
T <sub>f</sub>	Fall Time		---	7.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz	---	2423	---	pF
C <sub>oss</sub>	Output Capacitance		---	145	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	97	---	
Diode Characteristics						
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	35	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	80	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C	---	---	1	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =8A , dI/dt=100A/μs ,	---	16.3	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>J</sub> =25°C	---	11	---	nC

Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ 3. The EAS data shows Max. rating. The test condition is  $V_{DD}=25V$ ,  $V_{GS}=10V$ ,  $L=0.1mH$ ,  $I_{AS}=28A$ 4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature5. The data is theoretically the same as  $I_D$  and  $I_S$ , in real applications, should be limited by total power dissipation.

Typical Characteristics

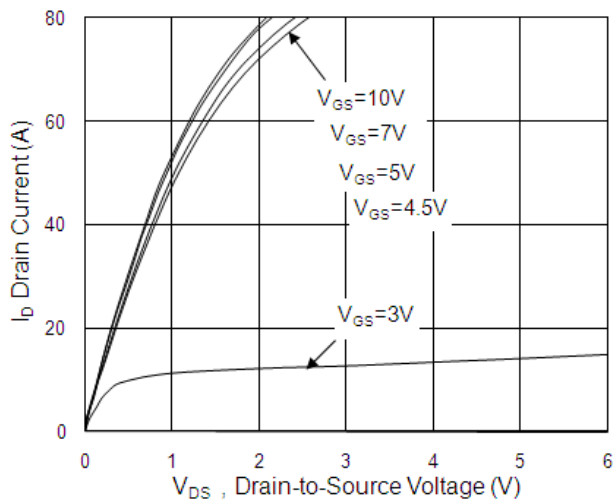


Fig.1 Typical Output Characteristics

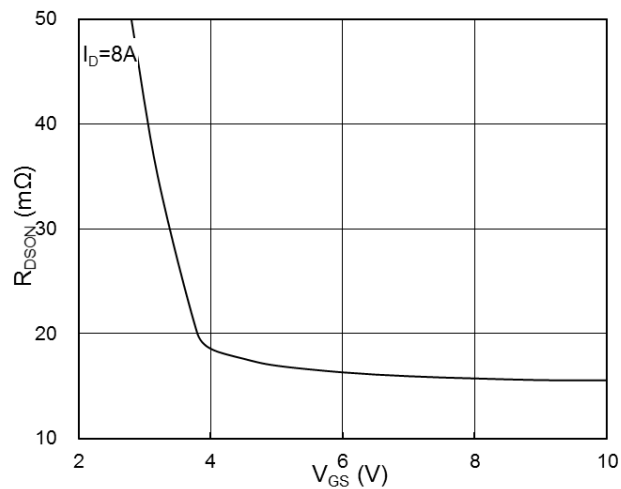


Fig.2 On-Resistance vs. Gate-Source Voltage

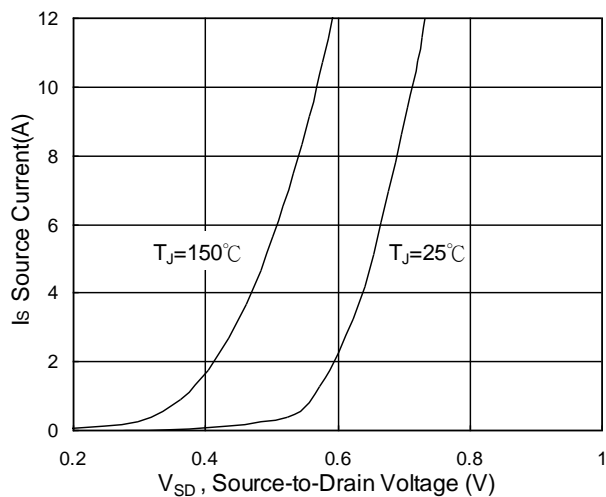


Fig.3 Forward Characteristics of Reverse

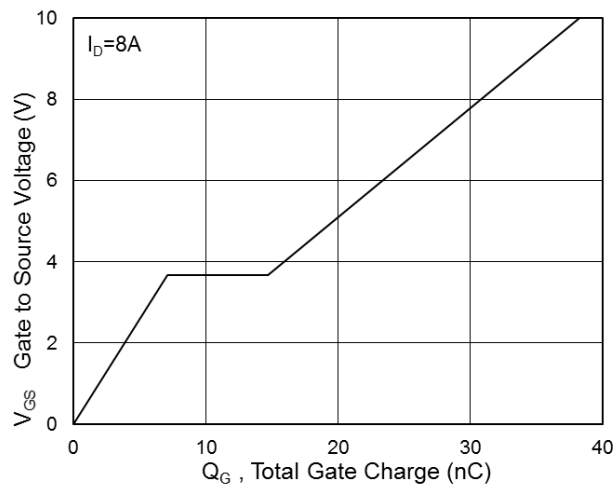


Fig.4 Gate-Charge Characteristics

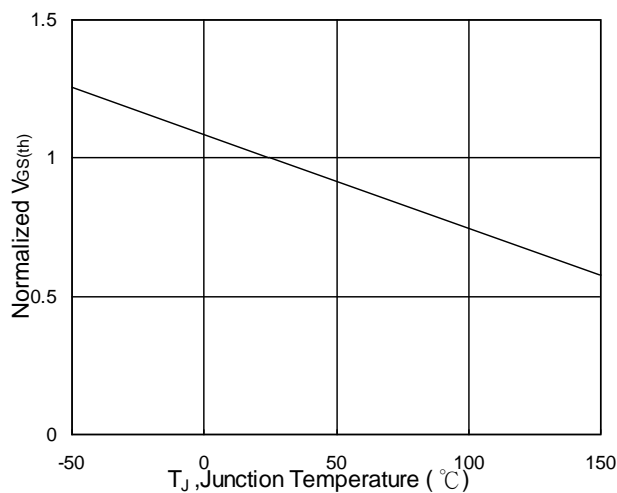


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

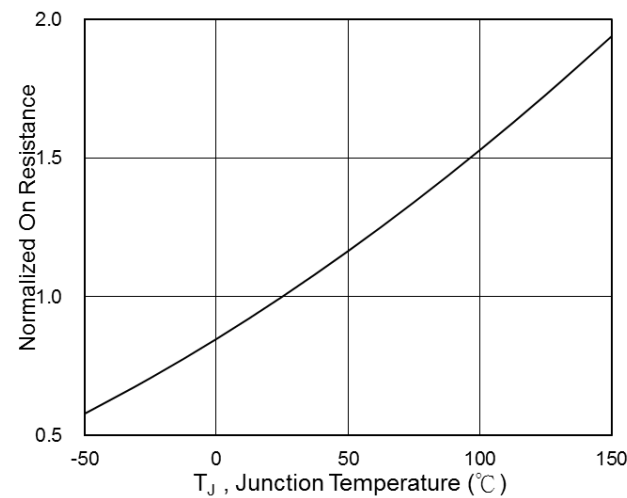
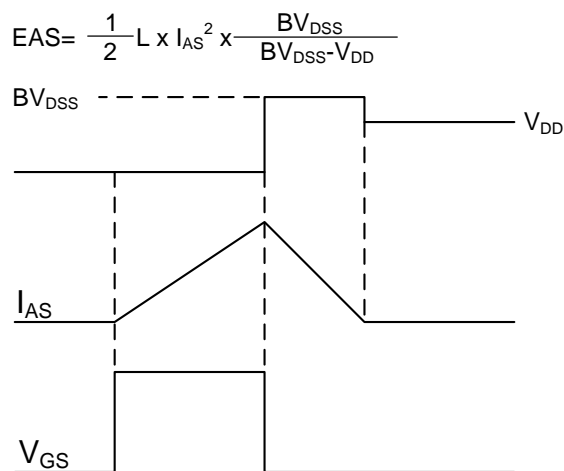
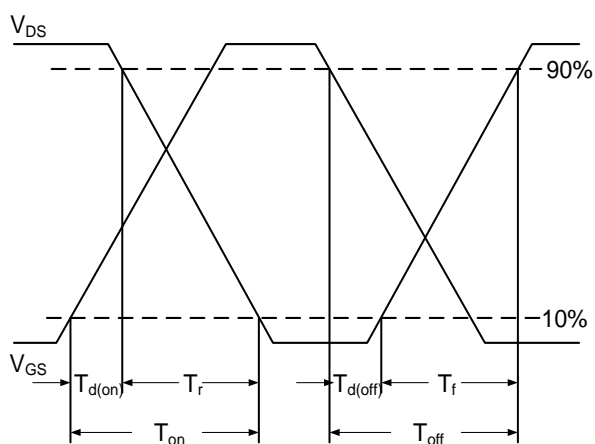
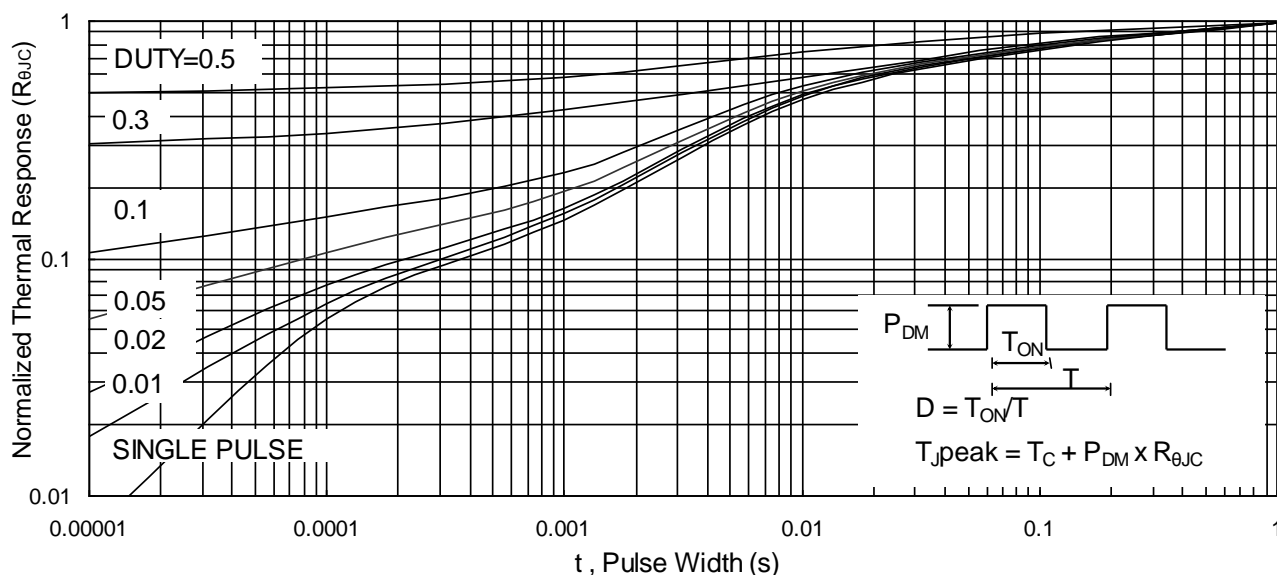
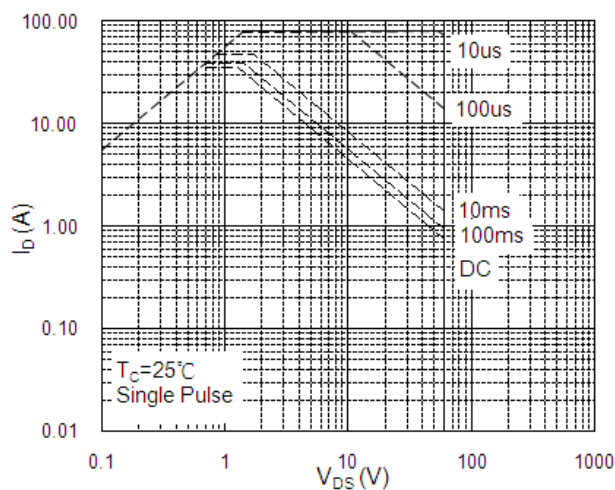
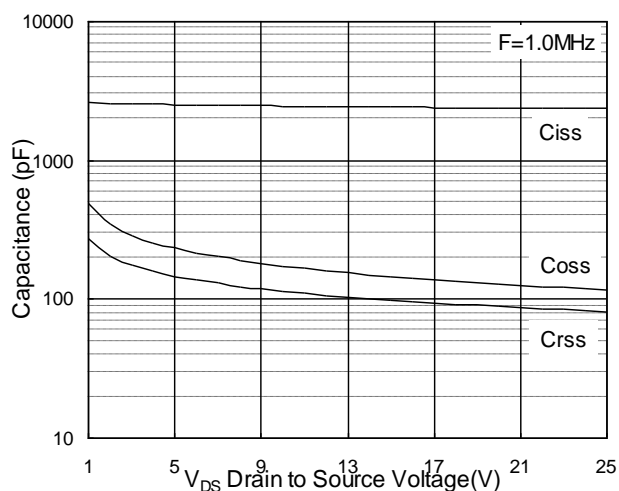
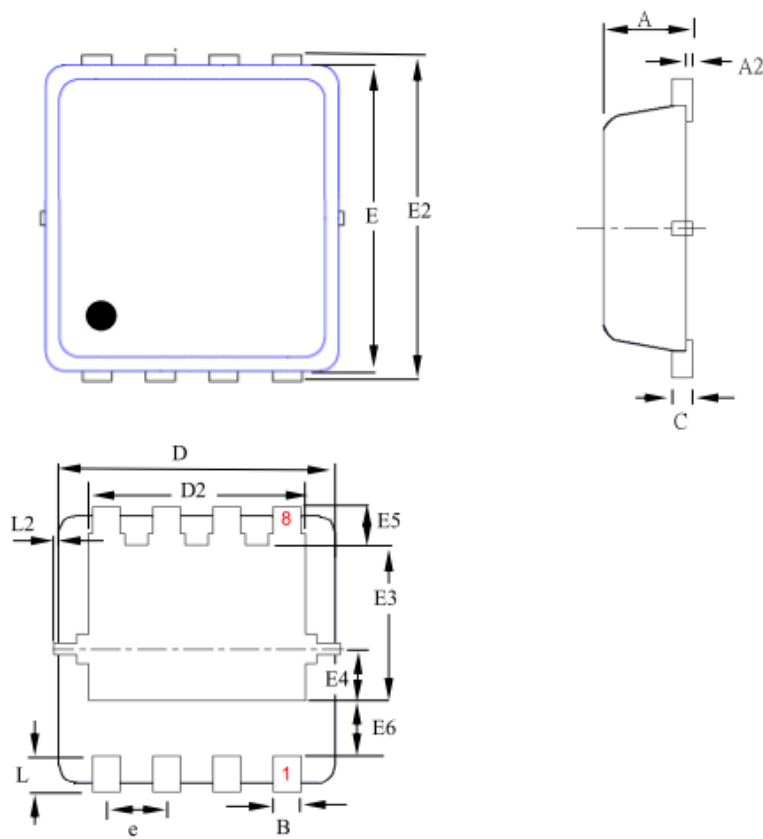


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



DFN3\*3 Package Outline Dimensions



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A2	0.00	--	0.05	0.000	--	0.002
B	0.24	0.30	0.35	0.009	0.012	0.014
C	0.10	0.15	0.25	0.004	0.006	0.010
D	2.90	3.00	3.20	0.114	0.118	0.126
D2	2.15	2.35	2.59	0.085	0.093	0.102
E	2.90	3.00	3.12	0.114	0.118	0.123
E2	3.05	3.20	3.45	0.120	0.126	0.136
E3	1.55	1.75	1.95	0.061	0.069	0.077
E4	0.48	0.58	0.68	0.019	0.023	0.027
E5	0.28	0.43	0.58	0.011	0.017	0.023
E6	0.43	0.63	0.87	0.017	0.025	0.034
L	0.30	0.40	0.50	0.012	0.016	0.020
L2	0.00	--	0.10	0.000	--	0.004
e	--	0.65	--	--	0.026	--

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