

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

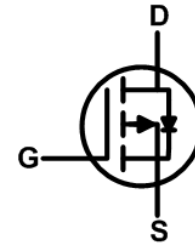
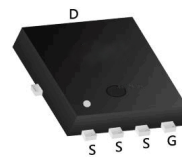
BVDSS	RDSON	ID
-30V	20mΩ	-32A

Description

The JHQ3103 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The JHQ3103 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

DFN3X3 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	-30		V
V_{GS}	Gate-Source Voltage	±25		V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, V_{GS} @ -10V ¹	-32		A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, V_{GS} @ -10V ¹	-20		A
$I_D@T_A=25^{\circ}C$	Continuous Drain Current, V_{GS} @ -10V ¹	-12.2	-7.7	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current, V_{GS} @ -10V ¹	-9.8	-6.2	A
I_{DM}	Pulsed Drain Current ²	-65		A
EAS	Single Pulse Avalanche Energy ³	72.2		mJ
I_{AS}	Avalanche Current	-38		A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	29		W
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ⁴	4.2	1.67	W
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	75	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	30	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	4.32	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.022	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-15A	---	---	20	mΩ
		V _{GS} =-4.5V, I _D =-10A	---	---	32	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	---	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±25V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-15A	---	19	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-15A	---	12.5	---	nC
Q _{gs}	Gate-Source Charge		---	5.4	---	
Q _{gd}	Gate-Drain Charge		---	5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-15A	---	4.4	---	ns
T _r	Rise Time		---	11.2	---	
T _{d(off)}	Turn-Off Delay Time		---	34	---	
T _f	Fall Time		---	18	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1345	---	pF
C _{oss}	Output Capacitance		---	194	---	
C _{rss}	Reverse Transfer Capacitance		---	158	---	
Diode Characteristics						
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-32	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-65	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	I _F =-15A, dI/dt=100A/μs, T _J =25°C	---	12.4	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-38A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_S , in real applications , should be limited by total power dissipation.

Typical Characteristics

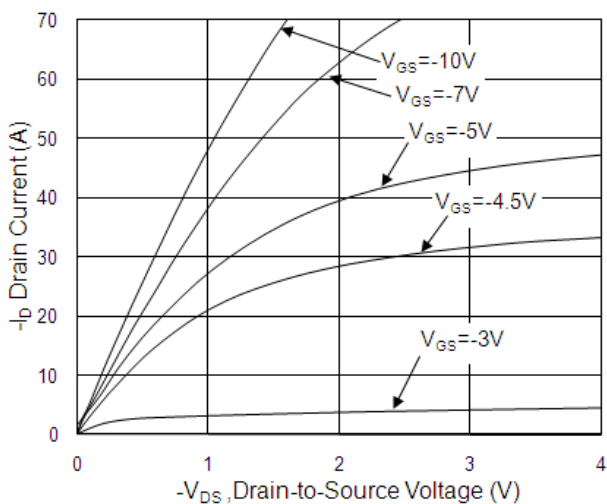


Fig.1 Typical Output Characteristics

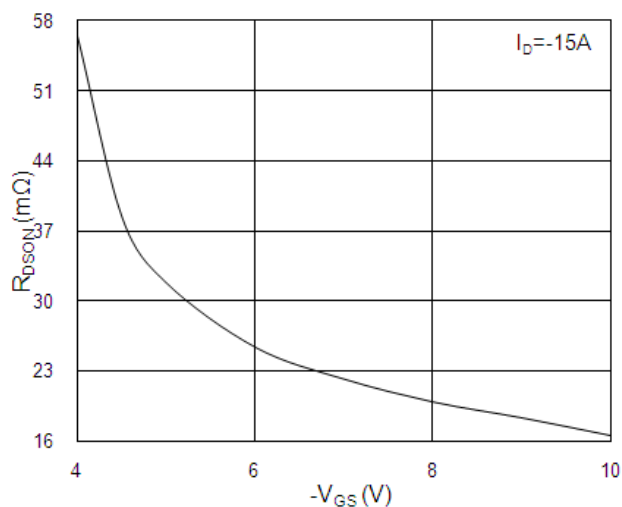


Fig.2 On-Resistance v.s Gate-Source

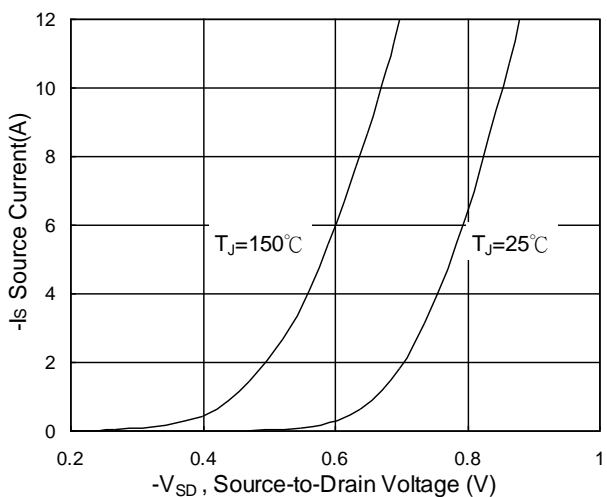


Fig.3 Forward Characteristics of Reverse

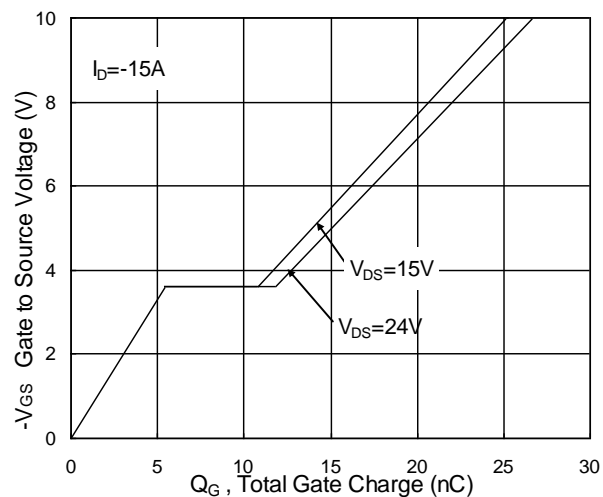


Fig.4 Gate-Charge Characteristics

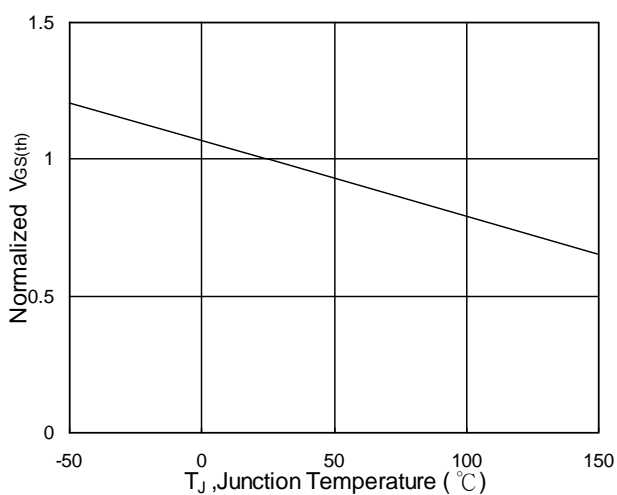


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

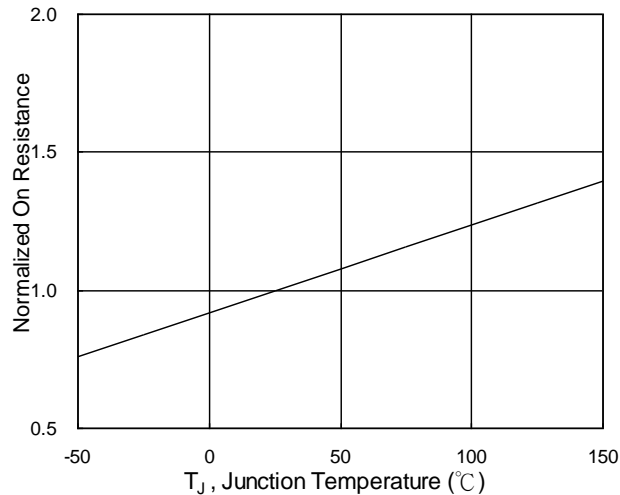


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

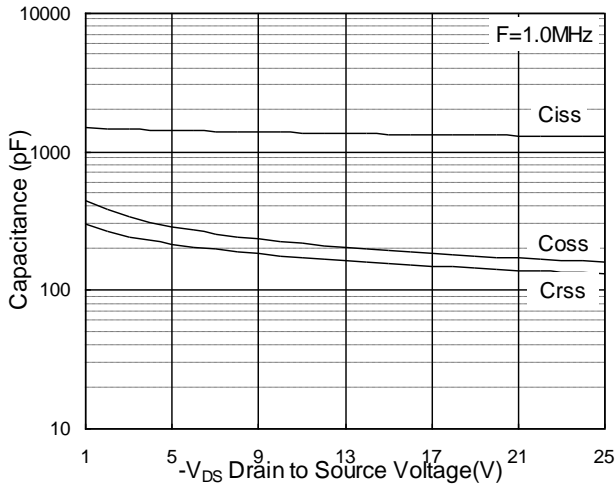


Fig.7 Capacitance

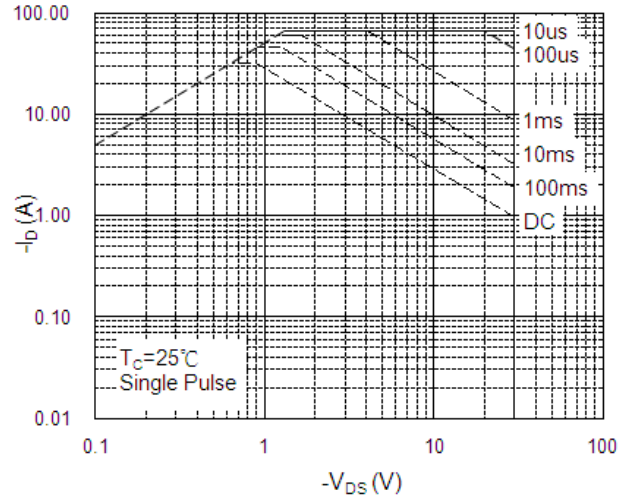


Fig.8 Safe Operating Area

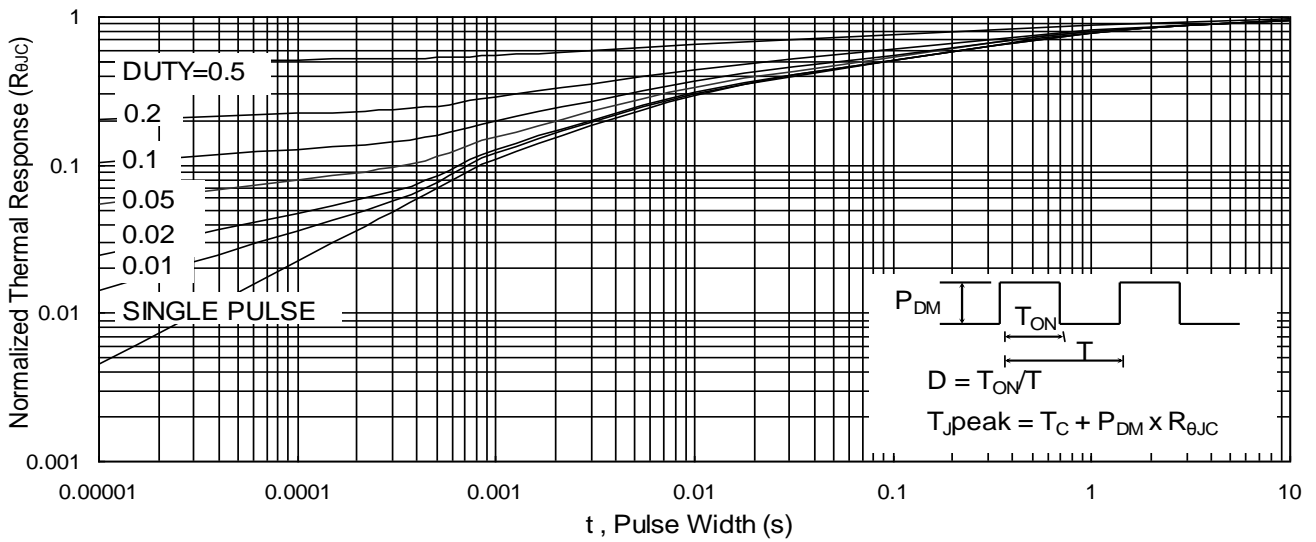


Fig.9 Normalized Maximum Transient Thermal Impedance

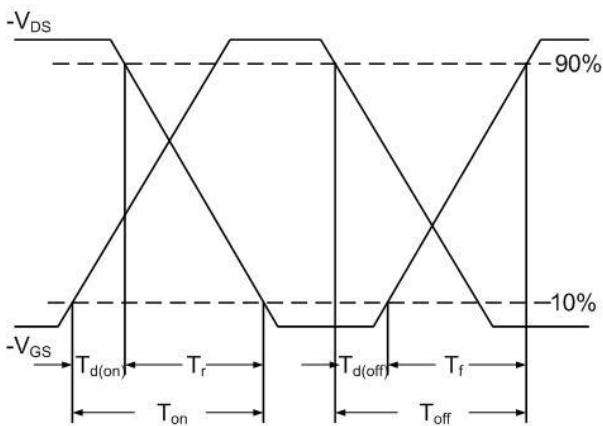


Fig.10 Switching Time Waveform

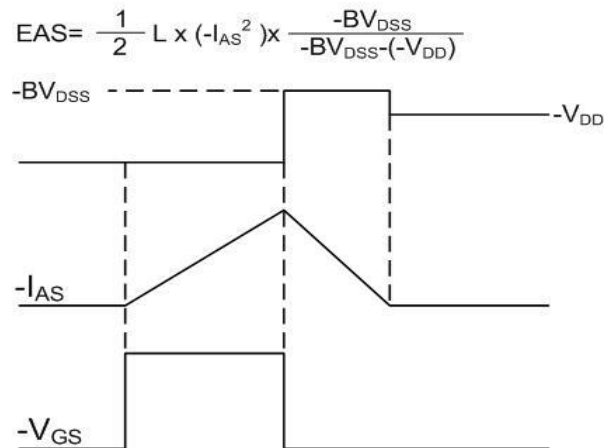
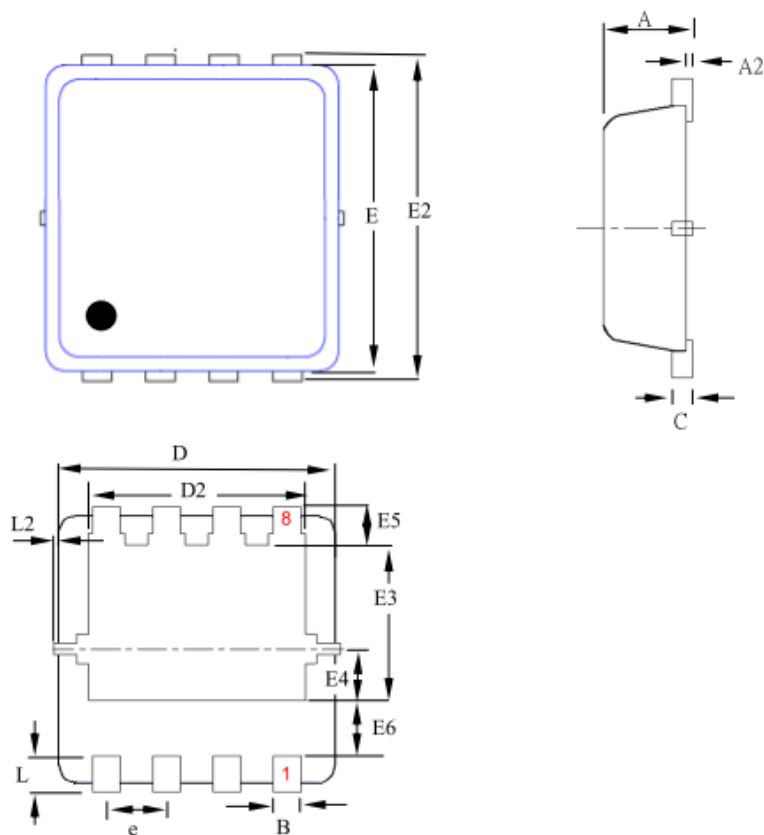


Fig.11 Unclamped Inductive Switching Waveform

DFN3*3 Package Outline Dimensions



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A2	0.00	--	0.05	0.000	--	0.002
B	0.24	0.30	0.35	0.009	0.012	0.014
C	0.10	0.15	0.25	0.004	0.006	0.010
D	2.90	3.00	3.20	0.114	0.118	0.126
D2	2.15	2.35	2.59	0.085	0.093	0.102
E	2.90	3.00	3.12	0.114	0.118	0.123
E2	3.05	3.20	3.45	0.120	0.126	0.136
E3	1.55	1.75	1.95	0.061	0.069	0.077
E4	0.48	0.58	0.68	0.019	0.023	0.027
E5	0.28	0.43	0.58	0.011	0.017	0.023
E6	0.43	0.63	0.87	0.017	0.025	0.034
L	0.30	0.40	0.50	0.012	0.016	0.020
L2	0.00	--	0.10	0.000	--	0.004
e	--	0.65	--	--	0.026	--

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