

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

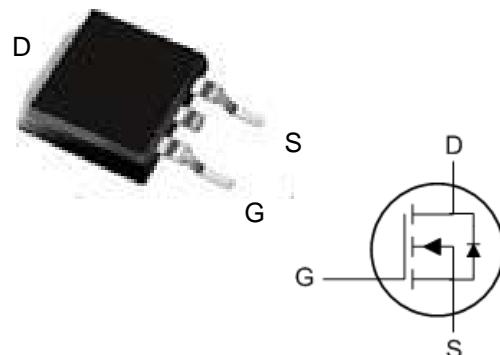
BVDSS	RDS(on)	ID
100V	22mΩ	45A

Description

The D45N10M is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The D45N10M meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	45	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	28	A
I _{DM}	Pulsed Drain Current ²	100	A
EAS	Single Pulse Avalanche Energy ³	84	mJ
I _{AS}	Avalanche Current	41	A
P _D @T _C =25°C	Total Power Dissipation ⁴	90	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.4	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	100	---	---	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.096	---	$^\circ\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=30\text{A}$	---	18	22	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	2.5	---	4.5	V
$\Delta V_{\text{GS}(\text{th})}$	$V_{\text{GS}(\text{th})}$ Temperature Coefficient		---	-5.5	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=30\text{A}$	---	27	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.9	3.8	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=80\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=30\text{A}$	---	27.6	38.6	nC
Q_{gs}	Gate-Source Charge		---	11.4	16	
Q_{gd}	Gate-Drain Charge		---	7.9	11.1	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=30\text{A}$	---	15.6	31.2	ns
T_r	Rise Time		---	17.2	31	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	16.8	33.6	
T_f	Fall Time		---	9.2	18.4	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1890	2645	pF
C_{oss}	Output Capacitance		---	268	375	
C_{rss}	Reverse Transfer Capacitance		---	67	94	

Diode Characteristics

I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}$, Force Current	---	---	45	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	100	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=30\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	34	---	nS
Q_{rr}	Reverse Recovery Charge		---	47	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DS}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=41\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

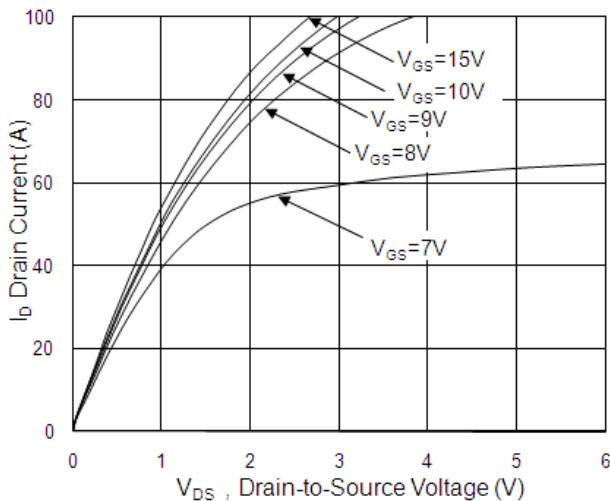


Fig.1 Typical Output Characteristics

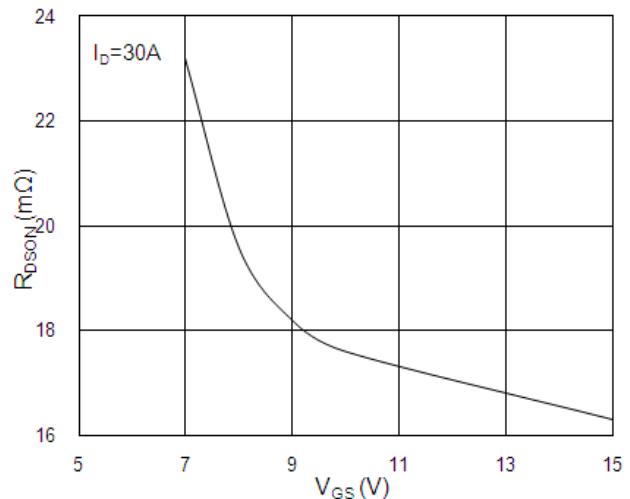


Fig.2 On-Resistance v.s Gate-Source

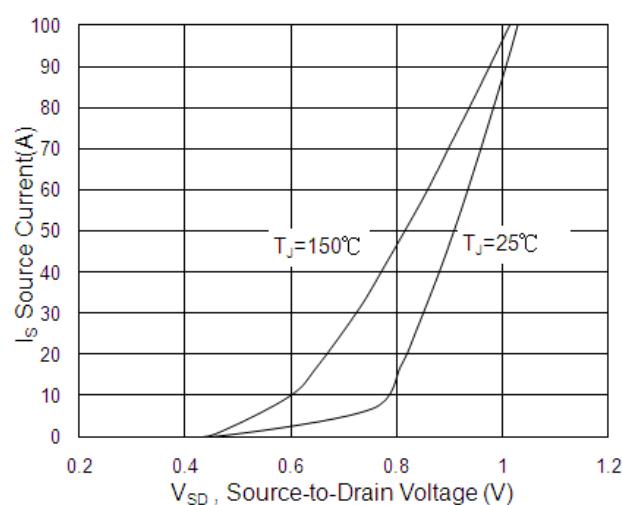


Fig.3 Forward Characteristics of Reverse

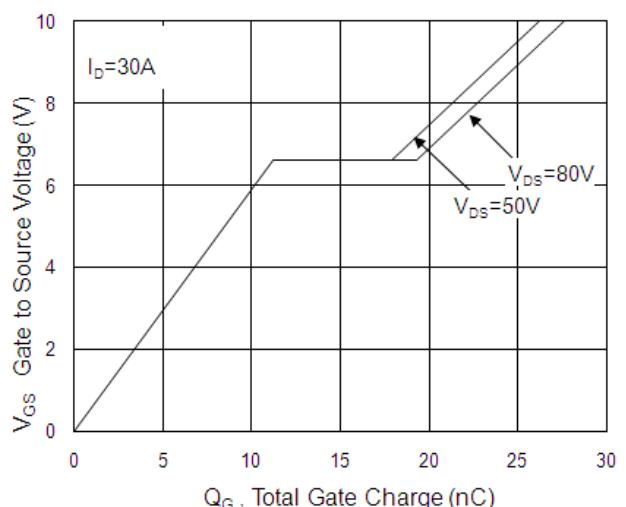


Fig.4 Gate-Charge Characteristics

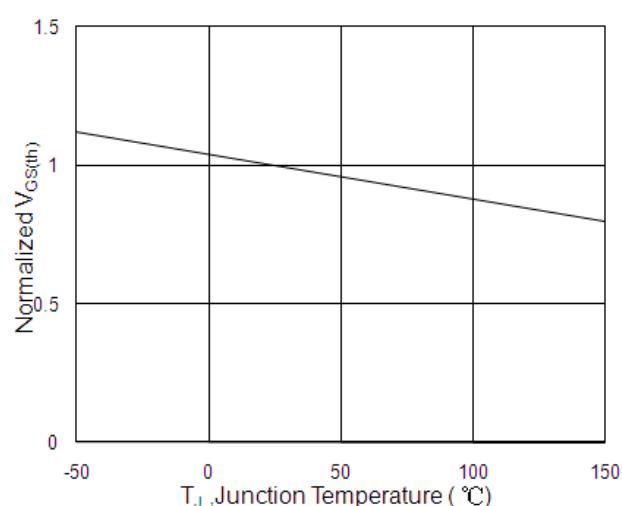


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

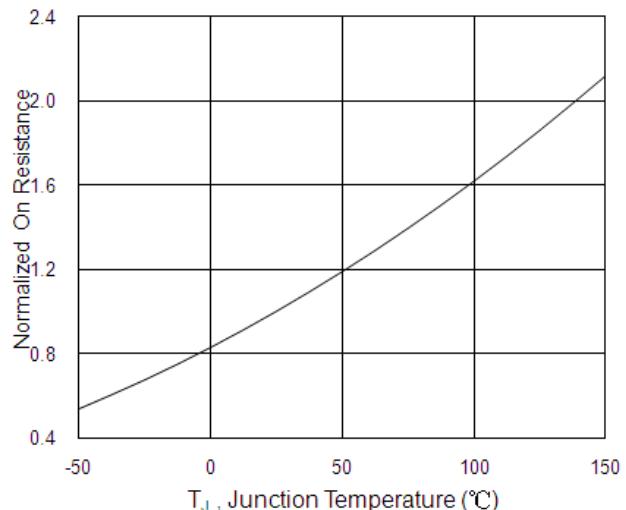


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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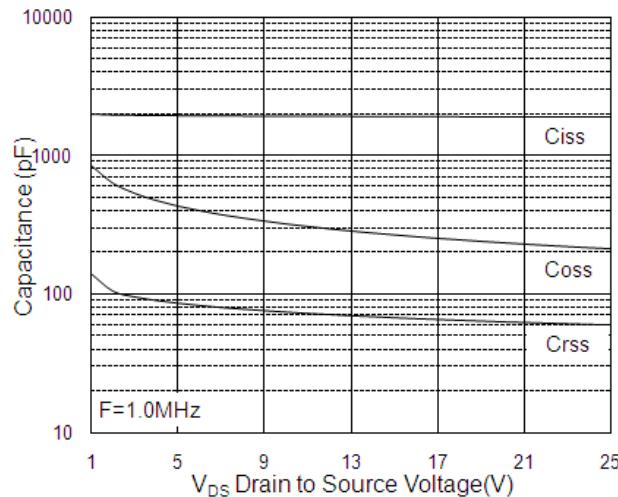


Fig.7 Capacitance

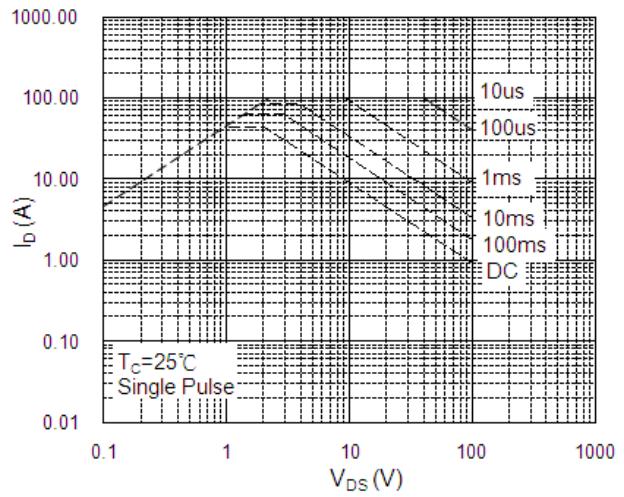


Fig.8 Safe Operating Area

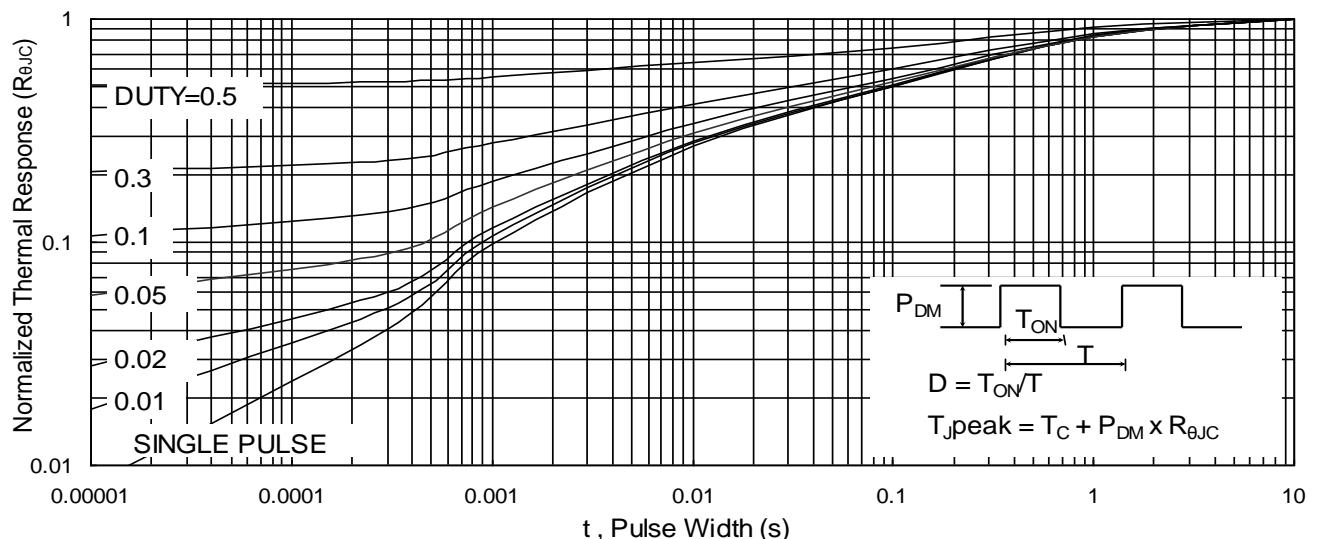


Fig.9 Normalized Maximum Transient Thermal Impedance

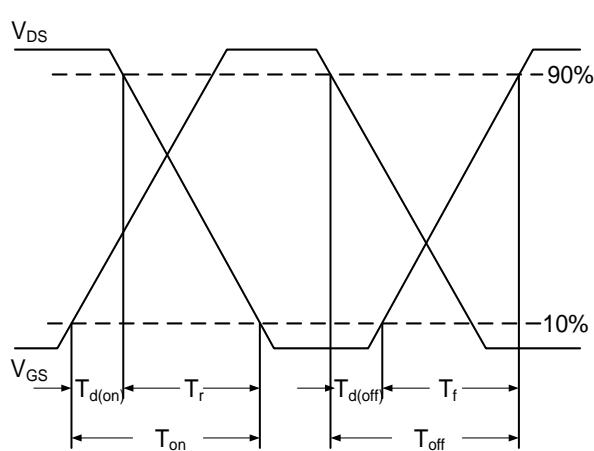


Fig.10 Switching Time Waveform

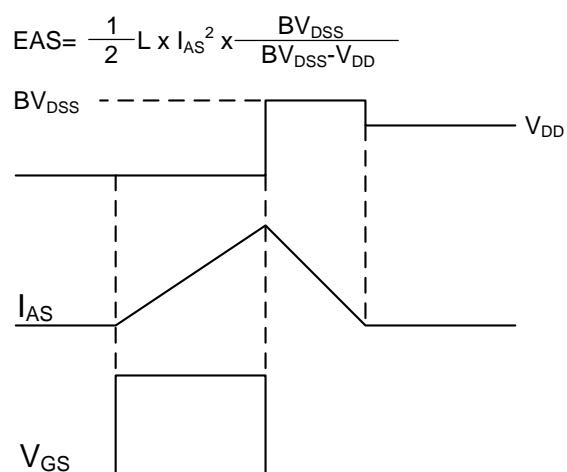
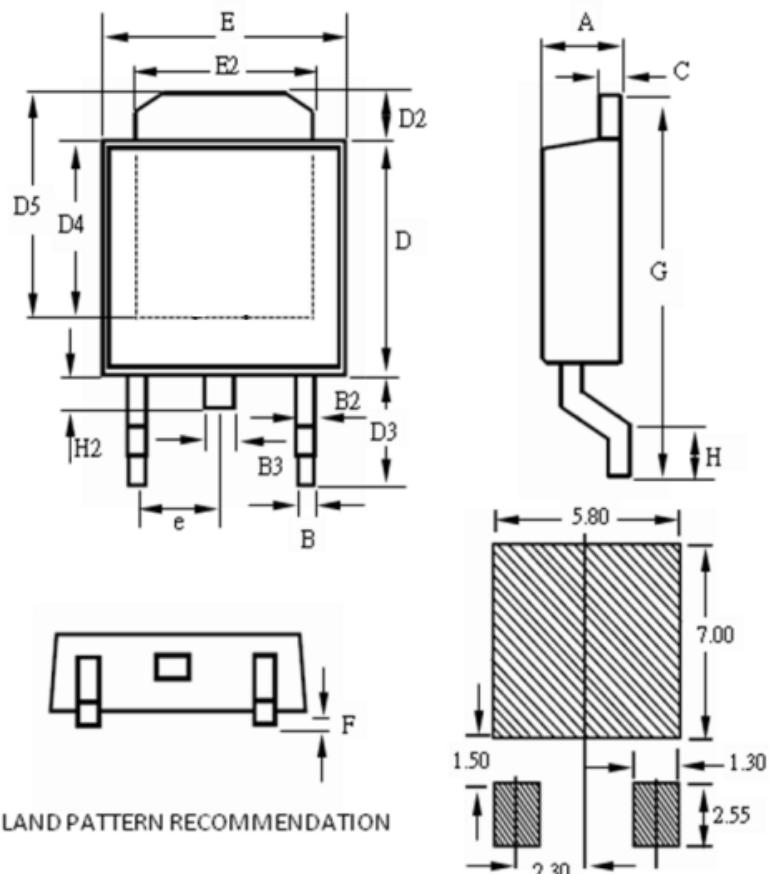


Fig.11 Unclamped Inductive Switching Waveform

TO-252 Package Outline



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.10	--	2.50	0.083	--	0.098
B	0.30	--	0.89	0.012	--	0.035
B2	0.40	--	1.14	0.016	--	0.045
B3	0.60	--	1.00	0.024	--	0.039
C	0.40	--	0.89	0.016	--	0.035
D	5.30	--	6.25	0.209	--	0.246
D2	0.50	--	1.70	0.020	--	0.067
D3	2.20	--	3.40	0.087	--	0.134
D4	4.32	--	--	0.170	--	--
D5	5.21	--	--	0.205	--	--
E	6.30	--	6.73	0.248	--	0.265
E2	4.80	--	5.46	0.189	--	0.215
F	0.00	--	0.30	0.000	--	0.012
G	9.20	--	10.41	0.362	--	0.410
H	0.90	--	1.95	0.035	--	0.077
H2	0.50	--	1.10	0.020	--	0.043
e	--	2.30	--	--	0.091	--

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