

Features

- Advanced Trench MOS Technology
- Low Gate Charge
- Low $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

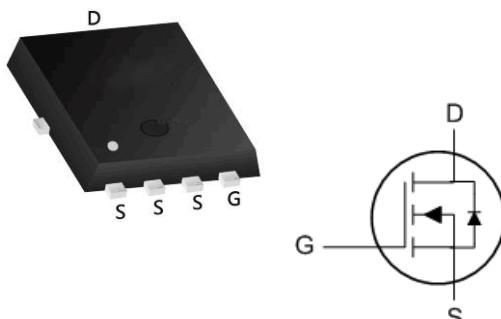
Product Summary

BVDSS	RDS(on)	ID
30V	3.9mΩ	73A

Applications

- Power Management in Desktop Computer or DC/DC Converters.
- Isolated DC/DC Converters in Telecom and Industrial.

DFN5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	73	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	46	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	80	mJ
I_{AS}	Avalanche Current	40	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	37.8	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	55	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.3	°C/W

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=250\mu\text{A}$	30	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_{\text{D}}=20\text{A}$	---	3.2	3.9	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_{\text{D}}=15\text{A}$	---	4.9	6.1	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_{\text{D}}=250\mu\text{A}$	1.2	1.7	2.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=30\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_{\text{D}}=20\text{A}$	---	75	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	0.7	1.65	2.6	Ω
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=4.5\text{V}$, $I_{\text{D}}=20\text{A}$	---	14.7	---	nC
Q_{gs}	Gate-Source Charge		---	5.8	---	
Q_{gd}	Gate-Drain Charge		---	3.5	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_{\text{G}}=3\Omega$	---	7.5	---	ns
T_r	Rise Time		---	20.2	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	21.6	---	
T_f	Fall Time		---	4.4	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1476	---	pF
C_{oss}	Output Capacitance		---	556	---	
C_{rss}	Reverse Transfer Capacitance		---	70	---	
Diode Characteristics						
I_s	Continuous Source Current ^{1.5}	$V_G=V_D=0\text{V}$, Force Current	---	---	30	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=40\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_{D} and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

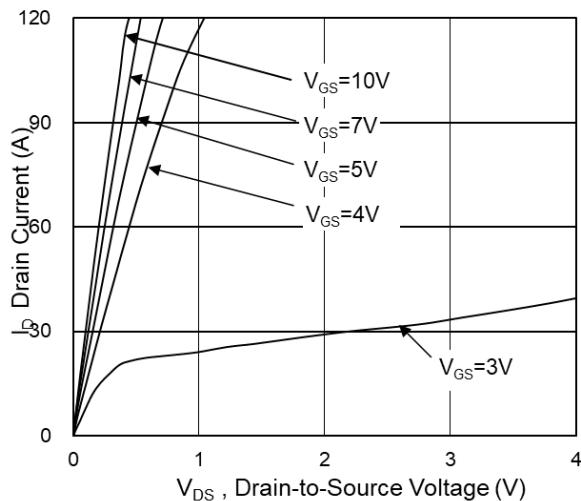


Fig.1 Typical Output Characteristics

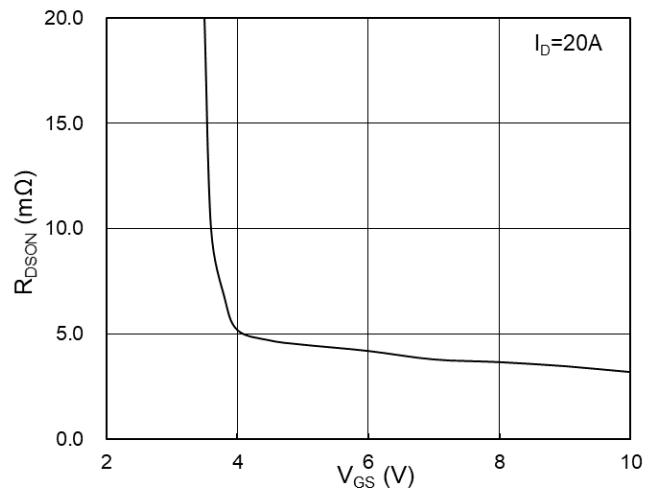


Fig.2 On-Resistance vs G-S Voltage

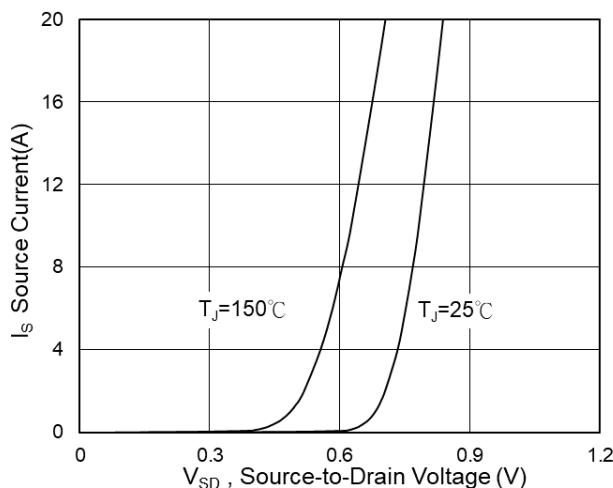


Fig.3 Source Drain Forward Characteristics

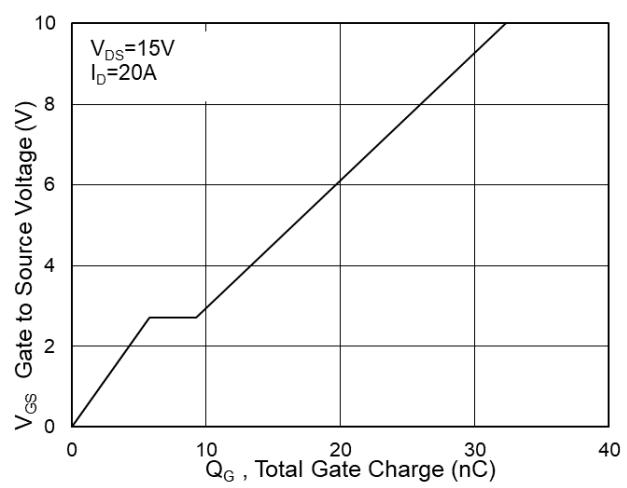


Fig.4 Gate-Charge Characteristics

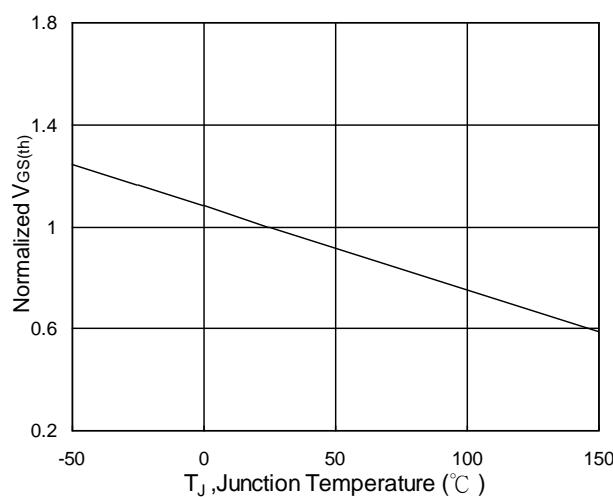


Fig.5 Normalized $V_{GS(th)}$ vs T_J

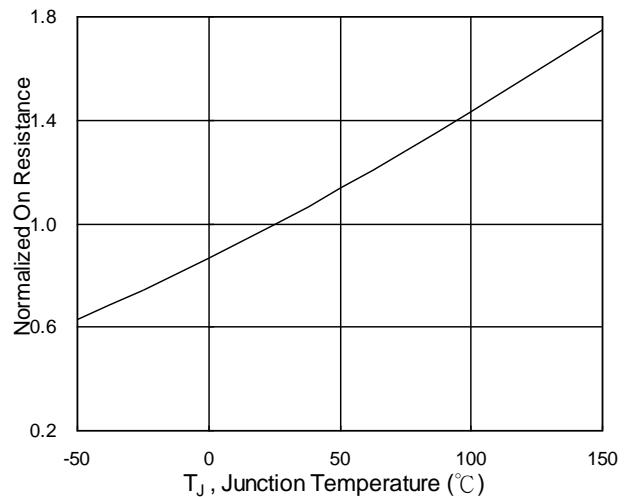


Fig.6 Normalized $R_{DS(on)}$ vs T_J

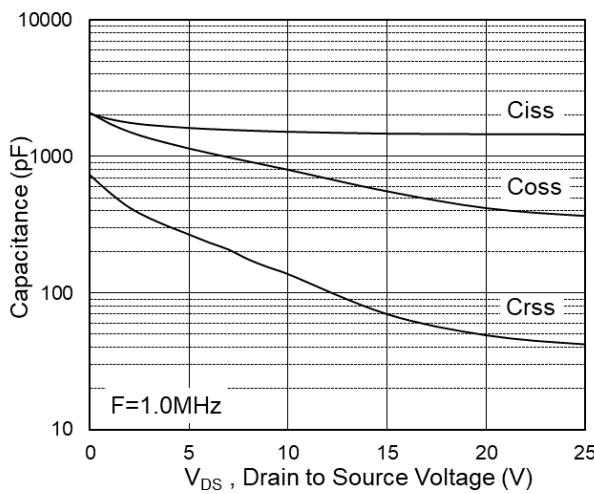


Fig.7 Capacitance

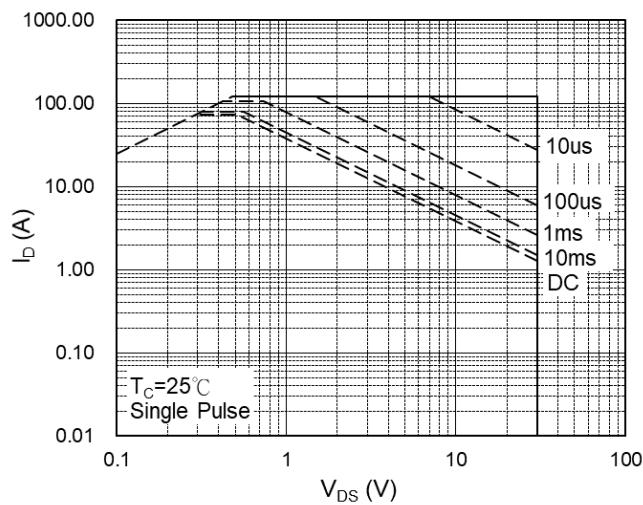


Fig.8 Safe Operating Area

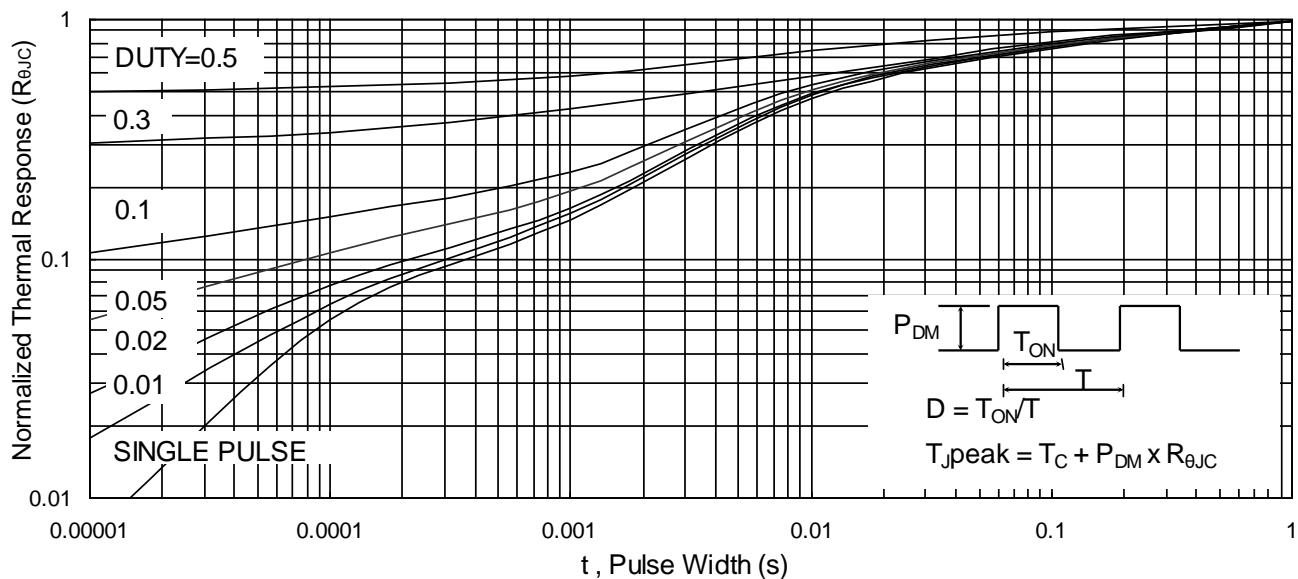


Fig.9 Normalized Maximum Transient Thermal Impedance

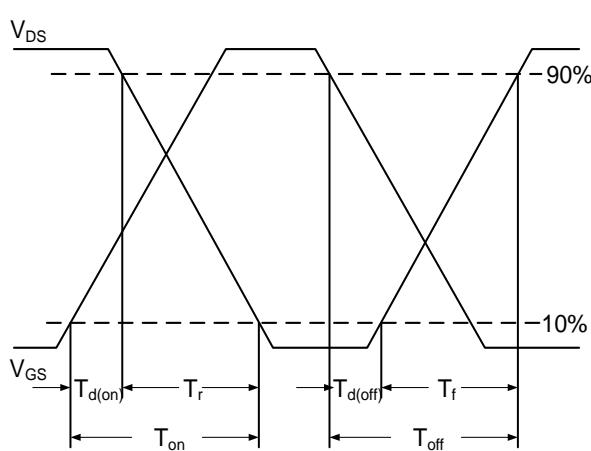


Fig.10 Switching Time Waveform

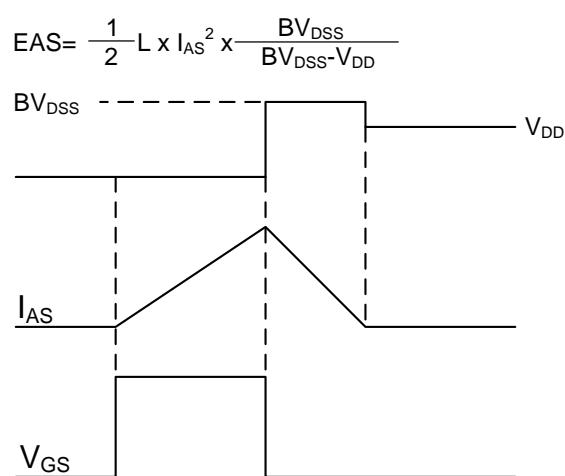
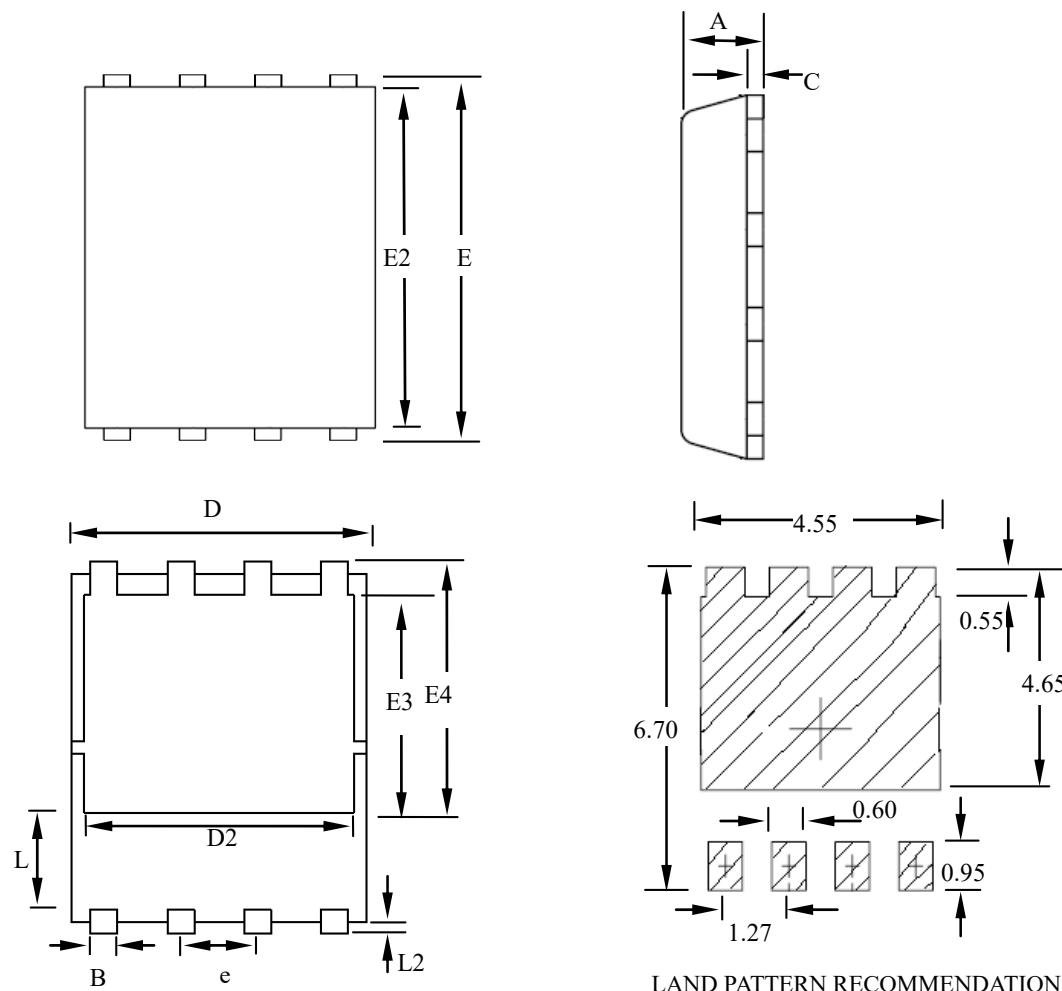


Fig.11 Unclamped Inductive Switching Wave

DFN5×6 Outline



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	--	1.20	0.031	--	0.047
B	0.30	--	0.51	0.012	--	0.020
C	0.15	--	0.35	0.006	--	0.014
D	4.80	--	5.30	0.189	--	0.209
D2	3.61	--	4.35	0.142	--	0.171
E	5.90	--	6.35	0.232	--	0.250
E2	5.42	--	5.90	0.213	--	0.232
E3	3.23	--	3.90	0.127	--	0.154
E4	3.69	--	4.55	0.145	--	0.179
L	0.61	--	1.80	0.024	--	0.071
L2	0.05	--	0.36	0.002	--	0.014
e	--	1.27	--	--	0.050	--

Friendship Reminder

■ JiNan JingHeng (hereinafter referred to as JH) reserves the right to make changes to this document and its products and specifications at anytime without notice.

■ Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

■ JH makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does JH assume any liability for application assistance or customer product design.

■ JH does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

■ No license is granted by implication or otherwise under any intellectual property rights of JH.

■ JH's products are not authorized for use as critical components in life support devices or systems without express written approval of JH.