

FEATURES

- $R_{DS(ON)} < 8.0m\Omega$ @ $V_{GS}=4.5V$
- $R_{DS(ON)} < 6.0m\Omega$ @ $V_{GS}=10V$
- 100% UIS Tested
- 100% ΔV_{DS} Tested

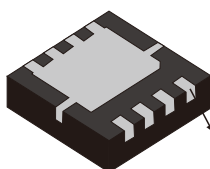


Product Summary			
V_{DS}	$R_{DS(on)}$ (m Ω) Typ	I_D (A)	Q_g (Typ)
30V	3.9 @ 10V	50	46.3nc
	6.0 @ 4.5V		

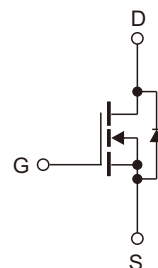
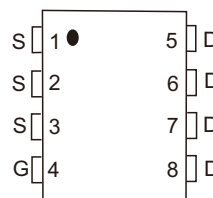
MECHANICAL DATA

- Case: DFN3.3 \times 3.3
- Terminals: Plated solderable per MIL-STD-750, method 2026
- Mounting Position: Any

DFN3.3 \times 3.3



Pin1



N-channel MOSFET

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameters		Symbol	Value	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}C$	I_D	50	A
	$T_C=100^{\circ}C$		35	
Pulsed Drain Current (Note 1)		I_{DM}	190	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	225	mJ
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	30	W
	$T_C=100^{\circ}C$		15	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	5	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^{\circ}C$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V, T _c =25°C	-	-	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	± 100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 4.5V, I _D =15A	-	6.0	8.0	mΩ
		V _{GS} = 10V, I _D =15A	-	3.9	6.0	
Dynamic						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	2191	-	pF
Output Capacitance	C _{oss}		-	300	-	
Reverse Transfer Capacitance	C _{rss}		-	247	-	
Total Gate Charge	Q _g	V _{DS} = 15V, V _{GS} =10V, I _D =20A	-	46.3	-	nC
Gate-Source Charge	Q _{gs}		-	8.8	-	
Gate-Drain Charge	Q _{gd}		-	9.2	-	
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, R _L =0,75Ω, R _{GEN} =3Ω	-	11	-	ns
Turn-on Rise Time	t _r		-	80	-	
Turn-off Delay Time	t _{D(off)}		-	39	-	
Turn-off Fall Time	t _f		-	92	-	
Drain-Source Body-Diode Characteristics						
Maximum Body-Diode Continuous Current	I _S		-	-	50	A
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Reverse Recovery Time	t _{rr}	I _F =20A	-	11	-	ns
Reverse Recovery Charge	Q _{RR}	di/dt=500A/μs	-	1.6	-	nC

Notes : 1 Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2 Repetitive Rating: Pulse width limited by maximum junction temperature

Typical Characteristics Diagrams

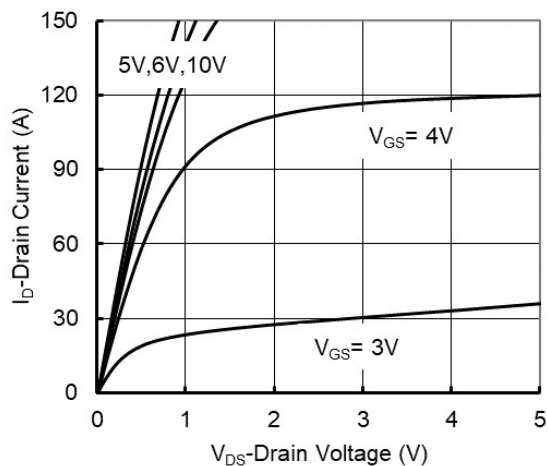


Figure 1. Output Characteristics

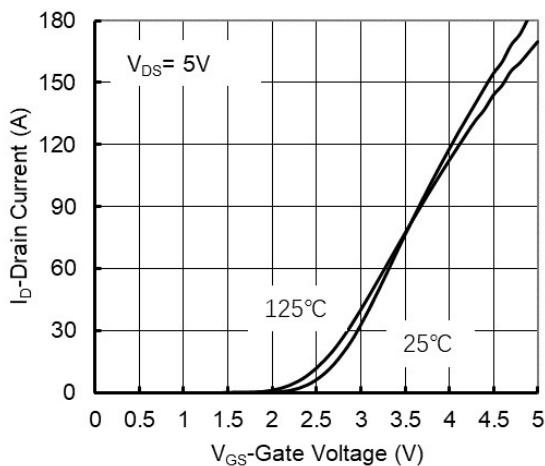


Figure 2. Transfer Characteristics

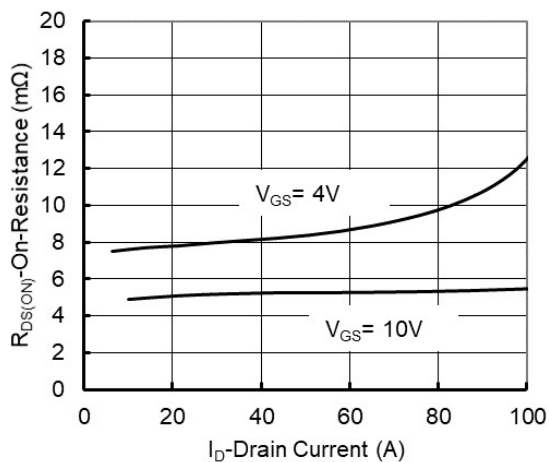


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

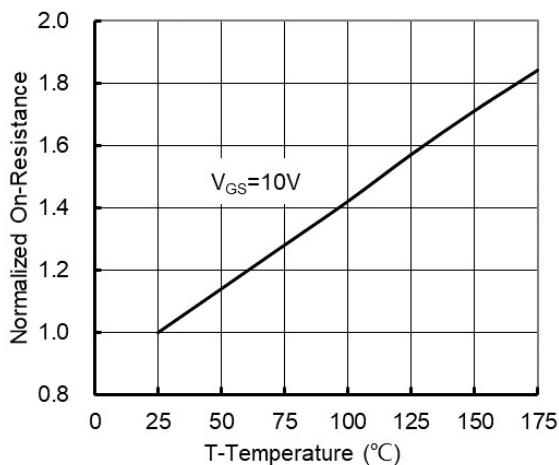


Figure 4. On-Resistance vs. Junction Temperature

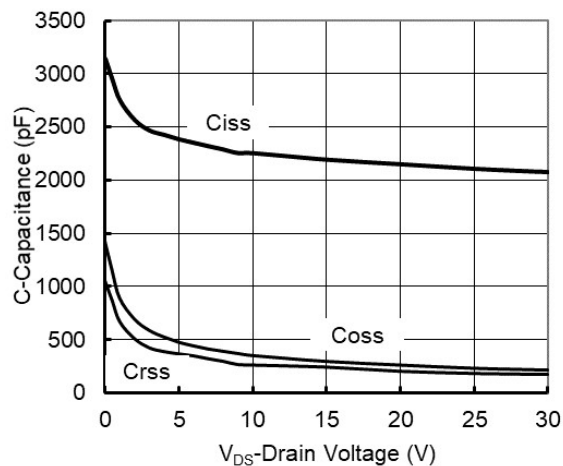


Figure 5. Capacitance Characteristics

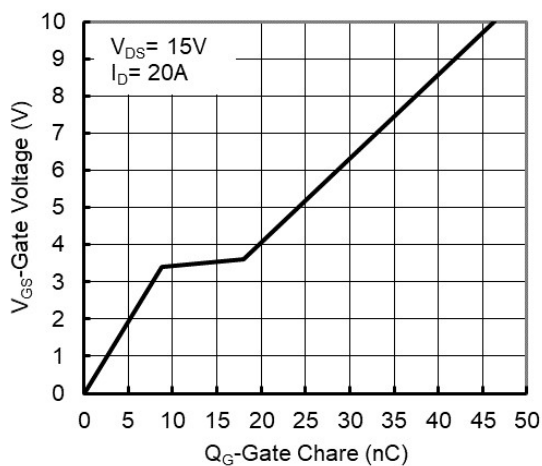


Figure 6. Gate Charge

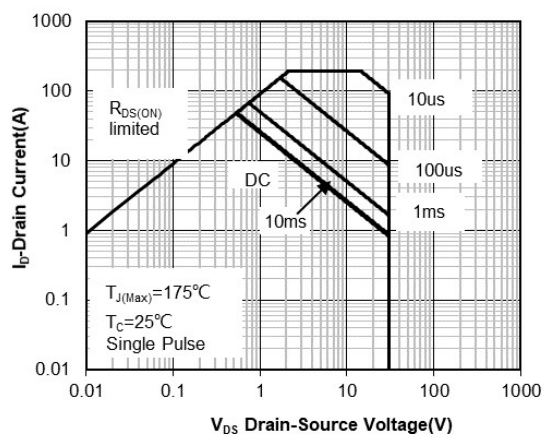


Figure 7. Safe Operation Area

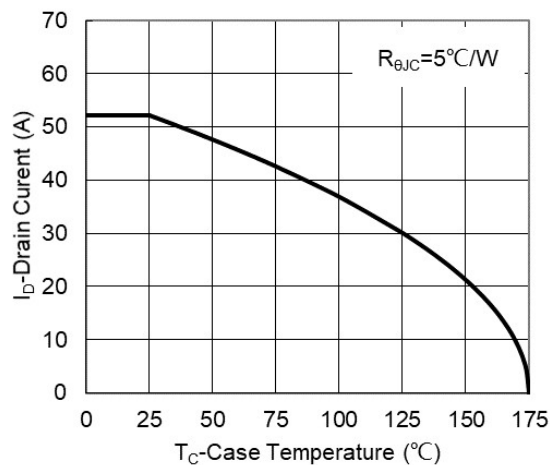


Figure 8. Maximum Continuous Drain Current vs Case Temperature

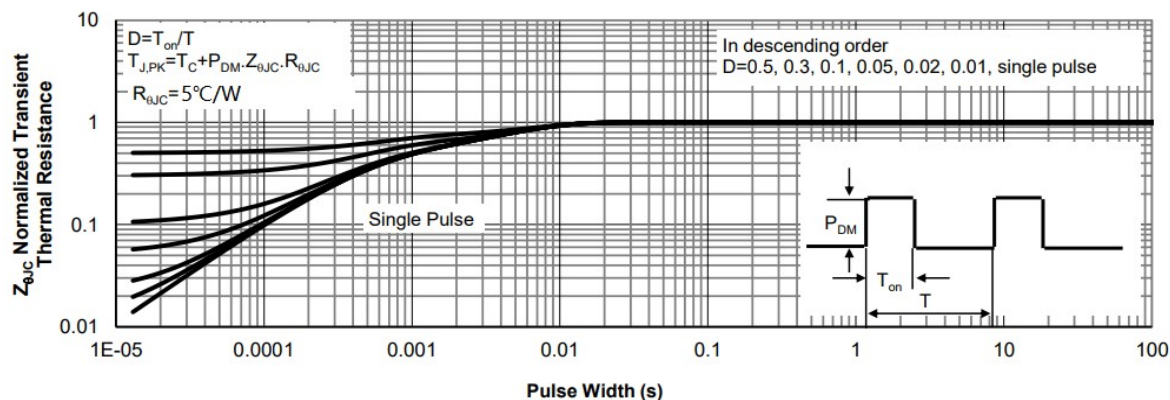
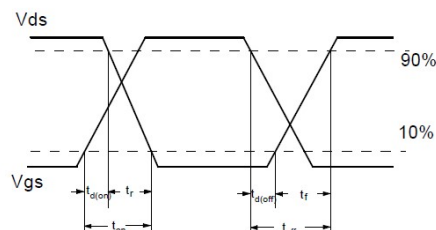
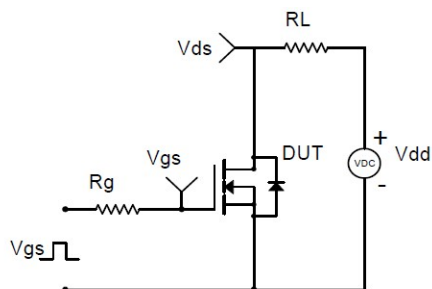
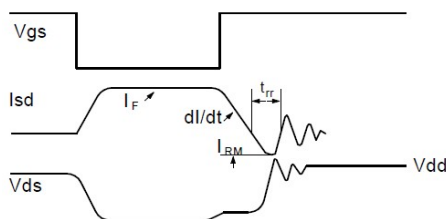
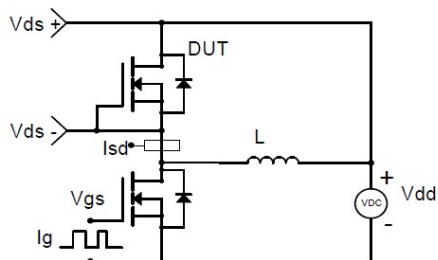


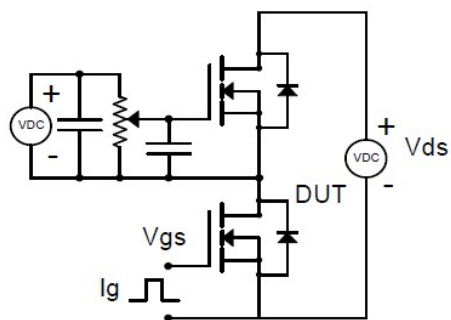
Figure 9. Normalized Maximum Transient Thermal Impedance



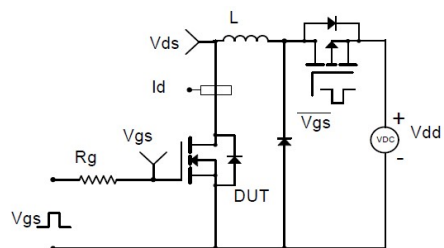
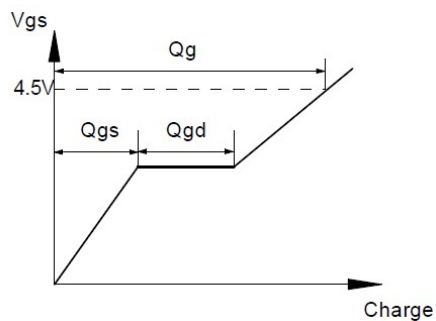
Resistive Switching Test Circuit & Waveforms



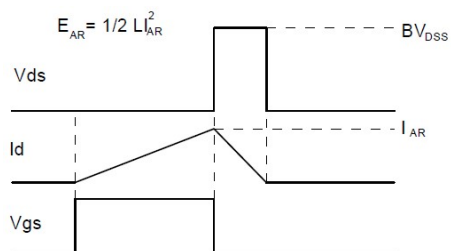
Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

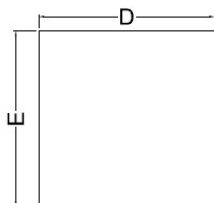


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

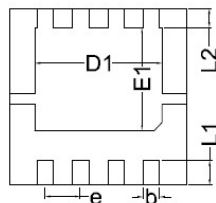


PACKAGE OUTLINE DIMENSIONS

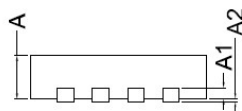
DFN3.3*3.3



Top View
正面视图

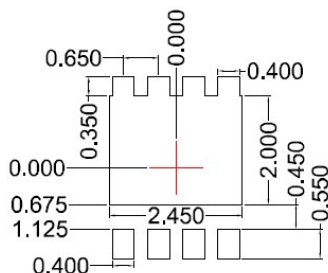


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.

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