

Features

- Fast switching
- Uses advanced SGT technology
- Low gate charge and Low on-resistance
- 100% avalanche tested

Product Summary			
V _{DS}	R _{DS(on)} (mΩ) Typ	I _D (A)	Q _g (Typ)
100V	6.7 @ 10V 50A	80	15nc

TO-252
DS80N10G3M



Mechanical Data

- Case:TO-252 Package

Application

- Motor control and drives
- DC-DC converters
- Battery management
- General purpose applications

Ordering Information

Part No.	Package Type	Package	Quality(box)
DS80N10G3M	TO-252	Tape & Reel	2500

Block Diagram

Pin Definition:

1. Gate
2. Drain
3. Source

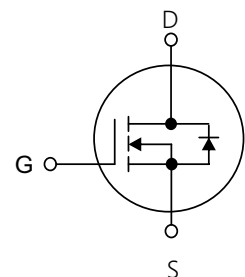


Table1 Absolute Maximum Ratings (T_c=25°C, unless otherwise specified)

Parameter	Symbol	DS80N10G3M	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous (Note 5) Drain Current	I _D	T _c =25°C 80	A
		T _c =100°C 52	
Pulsed Drain Current (Note 1)	I _{DM}	320	A
Single Pulse Avalanche Energy(Note 2)	E _{AS}	462	mJ
Power Dissipation T _c =25°C	P _D	114	W
Operating Junction and Storage Temperature	T _J /T _{STG}	-55~+150	°C

※ limited by maximum junction temperature

Table 2. Thermal Characteristics

Parameter	Symbol	DS80N10G3M	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	60	$^{\circ}\text{C/W}$
Thermal resistance Junction to Case	$R_{\theta JC}$	1.1	$^{\circ}\text{C/W}$

 Table 3. Electrical Characteristics ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V,I _D =250μA	100	-	-	V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =20V,V _{DS} =0V	-	-	100	nA
	Reverse		V _{GS} = -20V,V _{DS} =0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} ,I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V,I _D =50A	-	6.7	7.8	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C _{ISS}	V _{DS} =40V,V _{GS} =0V,f=1MHz	-	3646	-	pF
Output Capacitance		C _{OSS}		-	387	-	pF
Reverse Transfer Capacitance		C _{RSS}		-	19	-	pF
Switching Characteristics (Note 4)							
Turn-On Delay Time		t _{d(on)}	V _{DD} =50V, V _{GS} =10V,R _G =3Ω,	-	18	-	ns
Turn-On Rise Time		t _r		-	42	-	ns
Turn-Off Delay Time		t _{d(off)}		-	31	-	ns
Turn-Off Fall Time		t _f		-	8	-	ns
Total Gate Charge		Q _G	V _{DD} =50V,I _D =25A, V _{GS} =10V	-	15	-	nC
Gate-Source Charge		Q _{GS}		-	8	-	nC
Gate-Drain Charge		Q _{GD}		-	14	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V,I _S =50A	-	-	1.2	V
Maximum Continuous Drain-Source Diode Forward Current		I _S		-	-	80	A
Reverse Recovery Time		t _{rr}	V _{GS} =0V,I _F =20A dI _F /dt=500A/μs(Note 1)	-	71	-	ns
Reverse Recovery Charge		Q _{RR}		-	123	-	nC

Notes: 1 Repetitive Rating:Pulse width limited by maximum junction temperature

 2 $L=0.5\text{mH}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

 3 Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

4 Guaranteed by design, not subject to production

5 The maximum current is limited by the package.

Typical Characteristics Diagrams

Figure 1. Output Characteristics

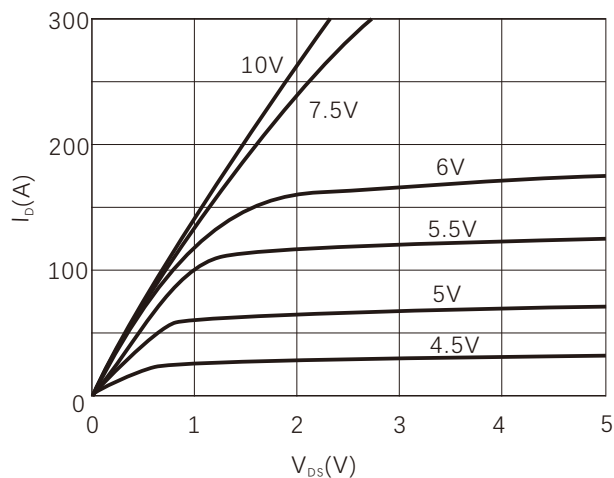


Figure 2. Transfer Characteristics

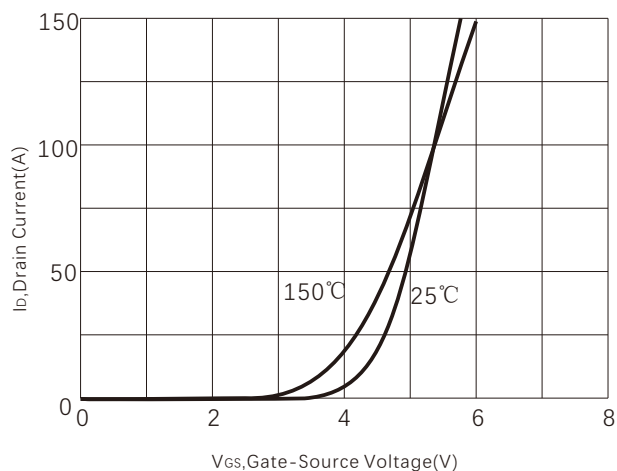


Figure 3. Normalized $R_{DS(ON)}$ vs Temperature

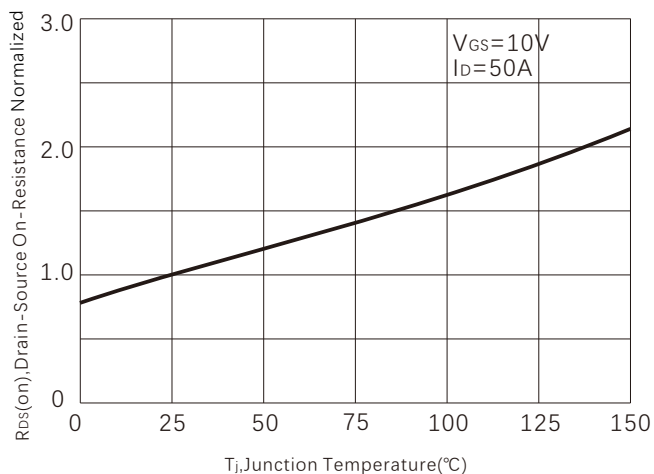


Figure 4. Capacitance

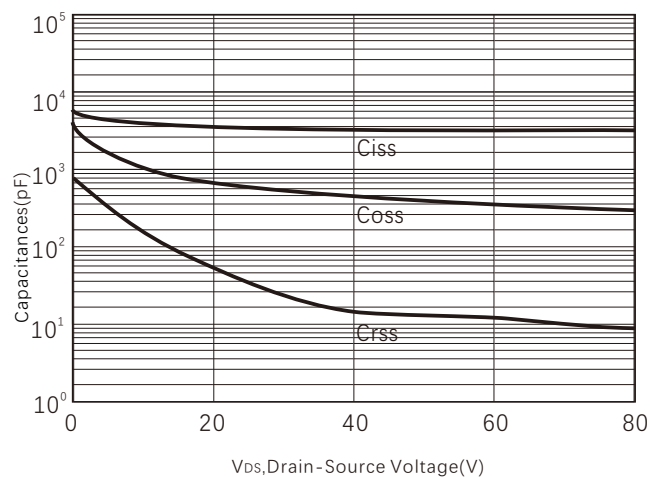


Figure 5. Gate charge

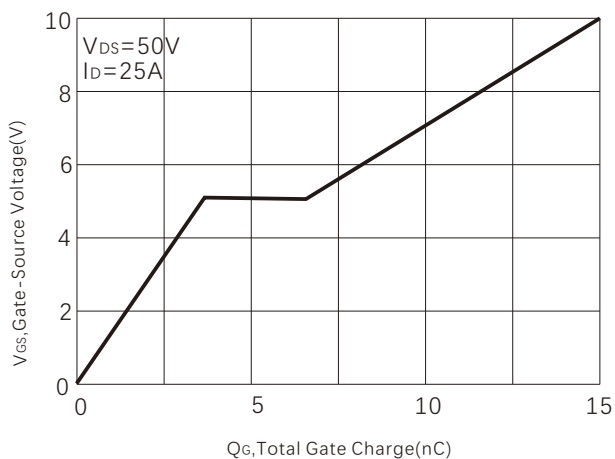


Figure 6. Source-Drain Diode Forward Voltage

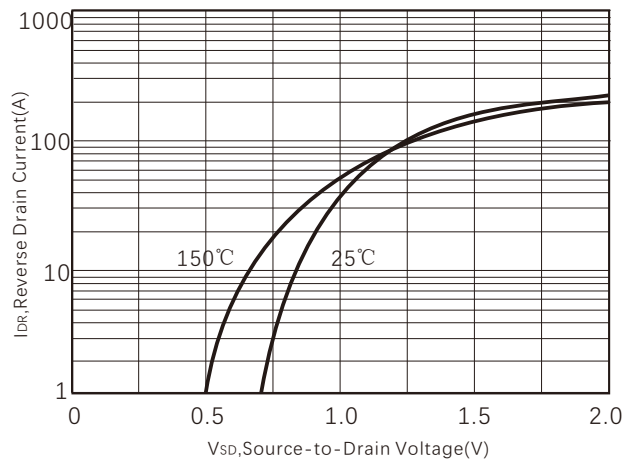


Figure7.Maximum Drain Current vs Temperature

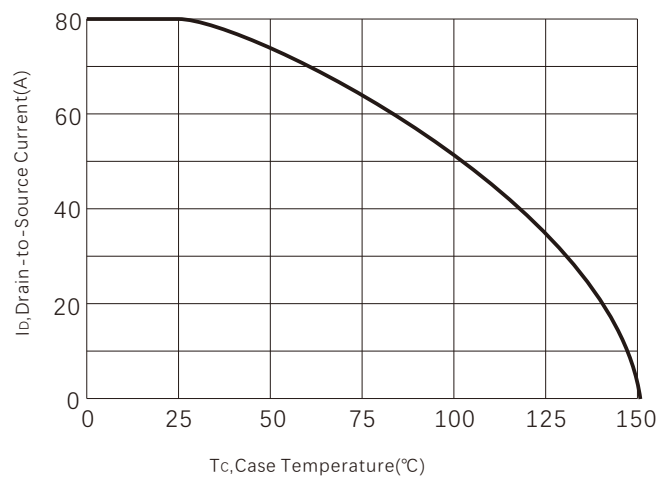


Figure 8. Power dissipation

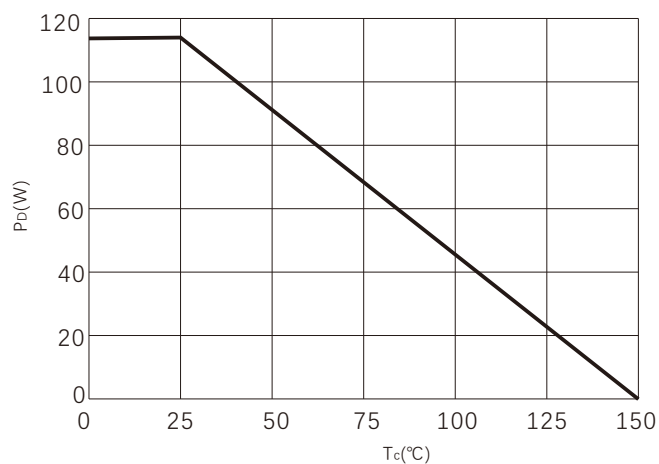


Figure 9.

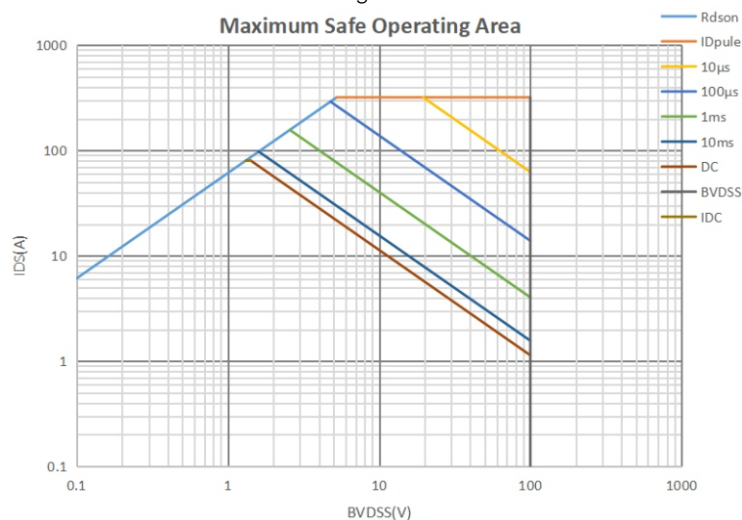
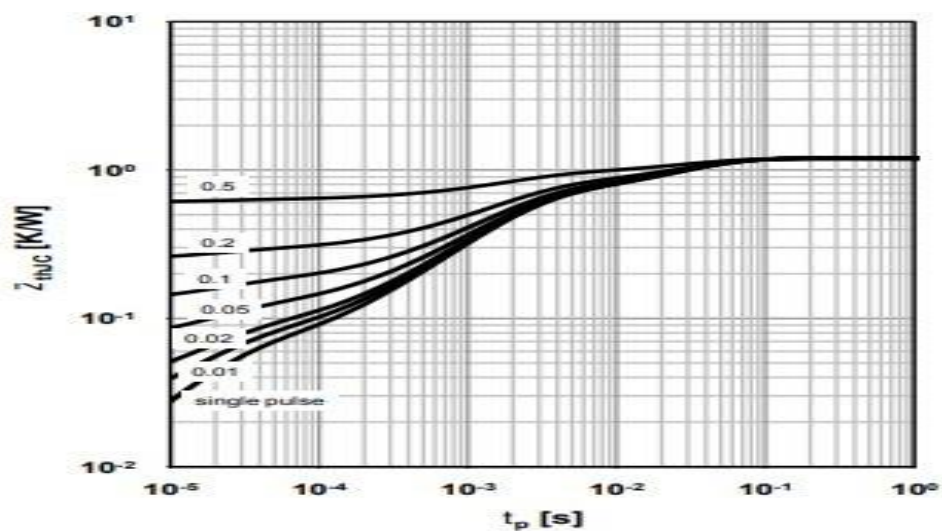
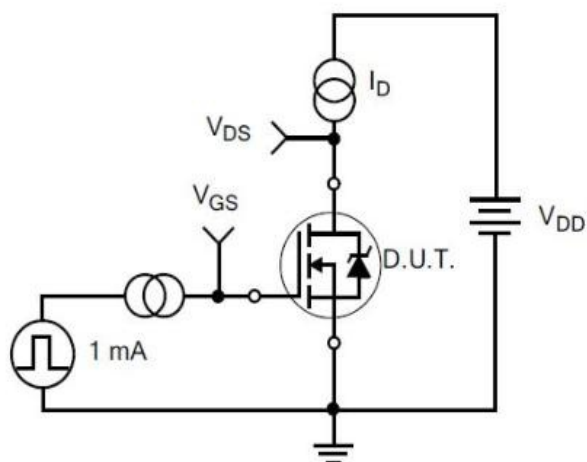


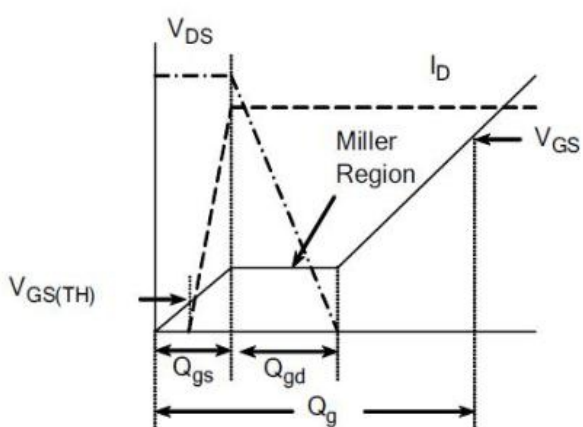
Figure 10. Maximum Transient Thermal Impedance



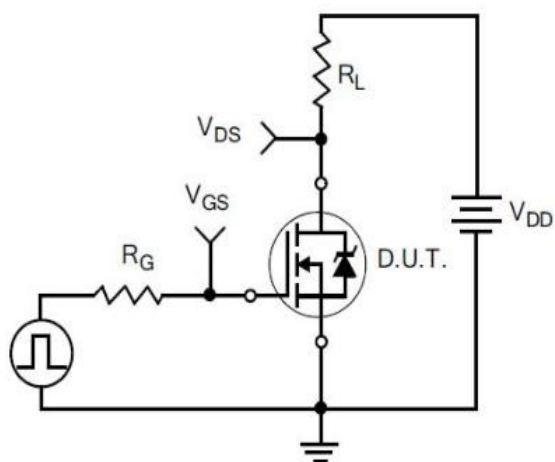
Typical Test Circuit



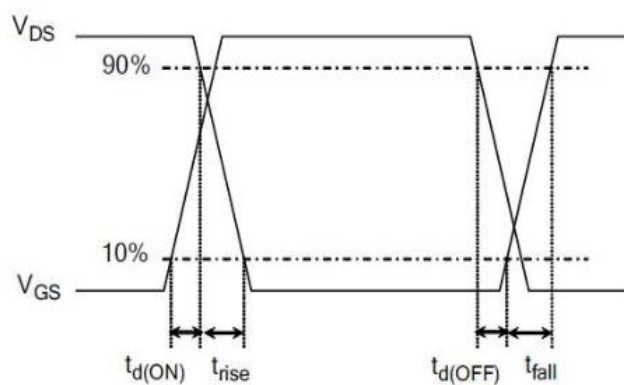
1) Gate Charge Test Circuit



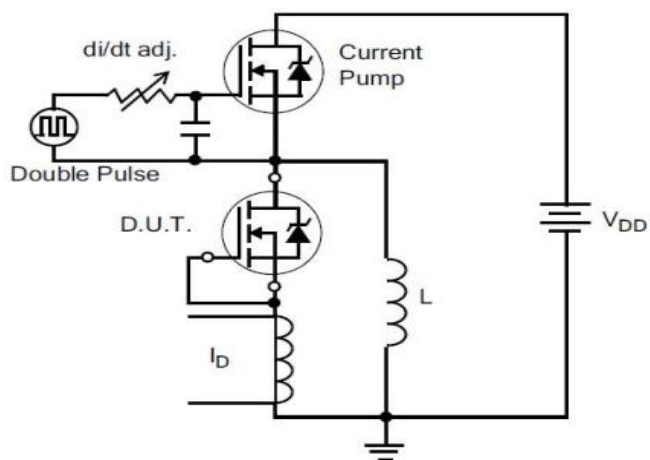
2) . Gate Charge Waveform



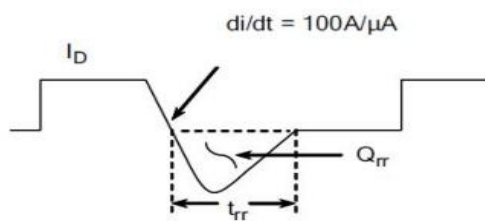
3) Resistive Switching Test Circuit



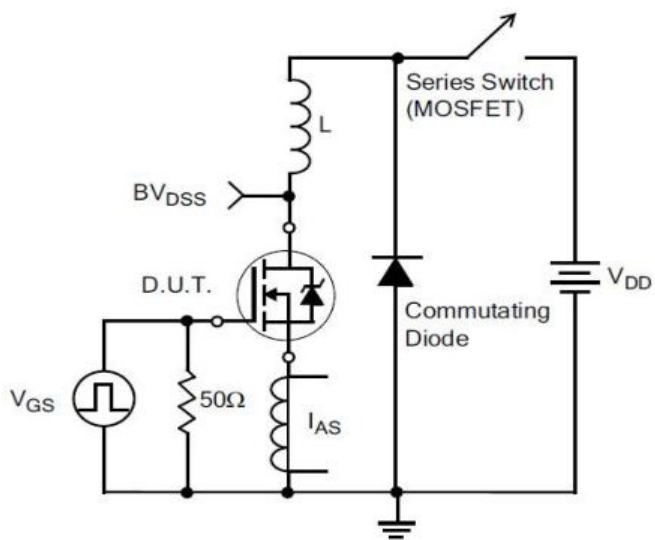
4) Resistive Switching Waveforms



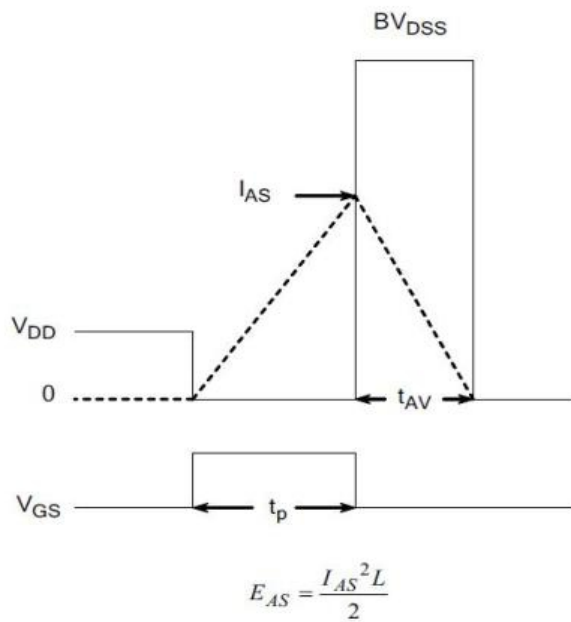
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



7) . Unclamped Inductive Switching Test Circuit



8) Unclamped Inductive Switching Waveforms

Product Names Rules

X X X N E X X X X X

Process Type:
VDMOS:default
Super junction:SJ
Low Voltage trench:D
Low Voltage SGT:DS

Rated Current Code
With 1-3 Digital,
For Ex ample:
4A:4,
10A:10,
0.8A:08

Channel Code
N channel:N
P channel:P

Package Code
TO-220:Default
ITO-220:F
TO-262:E
TO-263:D
TO-252:M
TO-251:N
TO-263-7L:D7

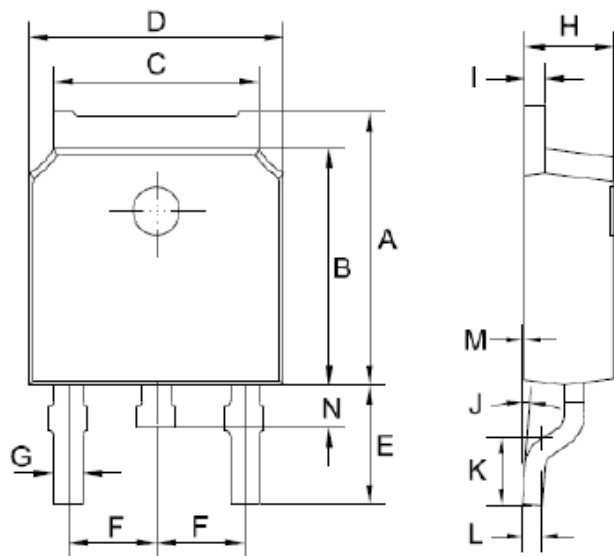
VGS(th)
VGS(th)=2-4V:G3
Other:Default

Rated Voltage Code
With 2 Digital,For Example:
600V:60
60V:06

Special Function Code
G-S ESD Protection:E
No Protection:Default

Dimensions

TO-252 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	6.85	7.25	0.270	0.285
B	5.8	6.3	0.228	0.248
C	5	5.53	0.197	0.218
D	6.3	6.8	0.248	0.268
E	2.6	3.3	0.102	0.130
F	2.19	2.39	0.086	0.094
G	0.45	0.85	0.018	0.033
H	2.2	2.4	0.087	0.094
I	0.41	0.61	0.016	0.024
J	0°	8°	0°	8°
K	1.45	1.85	0.057	0.073
L	0.41	0.61	0.016	0.024
M	0	0.12	0.000	0.005
N	0.6	1	0.024	0.039

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