SEMICONDUCTOR

SJ11N65G

650V N-Channel Super Junction Power MOSFET

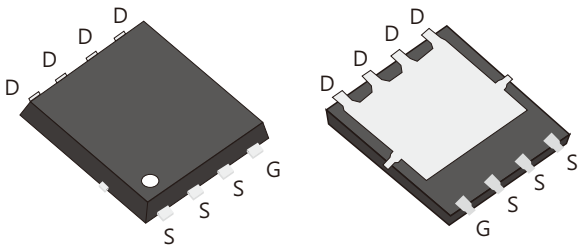
Genaral Description

This N-channel enhanced vdmosfets, is using advanced super junction technology and design to provide excellent Rds(on) with low gate charge. Which accords with the RoHS standard.

Product Summary			
V_{DS}	$R_{DS(on)}$(Ω)Typ	I_D(A)	Qg(Typ)
650V	0.36 @ 10V,5.5A	11	12nc

DFN5×6

SJ11N65G



Features

- Low on-resistance
- Ultra low gate charge and input capacitance
- 100% avalanche tested
- Rohs compliant

Mechanical Data

- Case:DFN5×6 Package

Application

- Switched mode power supplies(SMPS)
- Uninterruptible power supply(UPS)
- Power factor correction(PFC).

Ordering Information

Part No.	Package Type	Package	Quality(box)
SJ11N65G	DFN5×6	Tape & Reel	5000

Pin Definition:

1. Gate
2. Drain
3. Source

Block Diagram

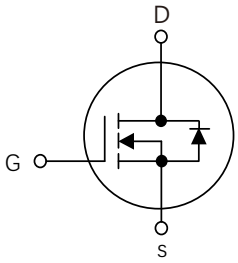


Table1 Absolute Maximum Ratings (Tc=25℃,unless otherwise specified)

Parameters		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Contionous Drain Current	Tc=25°C	I_D	11	A
	Tc=100°C		7	
Pulsed Drain Current (Note 1)		I_{DM}	33	A
Single Pulse Avalanche Energy(Note 2)		EAS	120	mJ
Avalanche Current(Note 2)		IAR	2	A
Power Dissipation Tc=25°C		P_D	63	W
Operating Junction and Storage Temperature		TJ/TSTG	-55 ~ +150	℃

Table 2.Thermal Characteristics

Parameters	Symbol	Value	Unit
Thermal resistance Junction to Ambient,Typ	$R_{\theta JA}$	62	℃/W
Thermal resistance Junction to Case,Typ	$R_{\theta JC}$	1.98	℃/W

Table 3. Electrical Chatacteristics (T_J=25℃, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	650			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=650V,V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V			100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=5.5A		0.36	0.42	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=50V,V_{GS}=0V,f=100kHz		602		pF
Output Capacitance		C_{OSS}			59		pF
Reverse Transfer Capacitance		C_{RSS}			3.6		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=400V,I_D=6A, V_{GS}=10V,R_G=2Ω		15		ns
Turn-On Rise Time		tr			18		ns
Turn-Off Delay Time		td(off)			60		ns
Turn-Off Fall Time		tf			15		ns
Total Gate Charge		Q_G	V_{DS}=400V,I_D=6A, V_{GS}=10V		12		nC
Gate-Source Charge		Q_{GS}			3.1		nC
Gate-Drain Charge		Q_{GD}			5.2		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=11A			1.3	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I_S				11	A
Reverse Recovery Time		trr	V_R=400V,I_S=6A dI$_F$/dt=100A/μs(Note 4)		250		ns
Reverse Recovery Charge		Q_{RR}			2.2		μC

Notes: 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=80mH,V_{DD}=100V,V_{GS}=10V,Starting T_J=25°C
3 I_{SD}≤I_D,di/dt≤200A/μS,V_{DS}≤480V,starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%
5 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

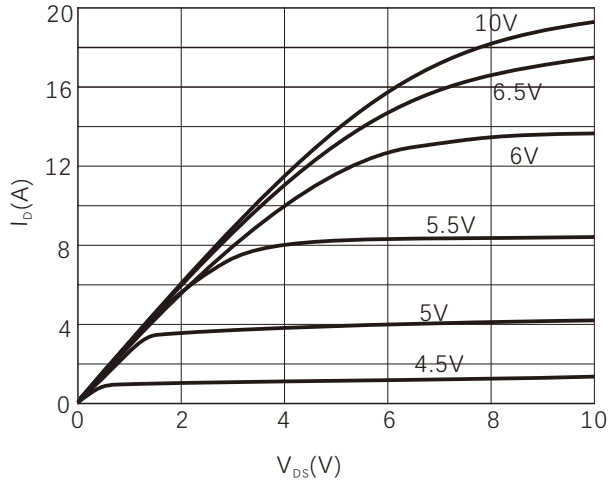


Figure 2. Transfer Characteristics

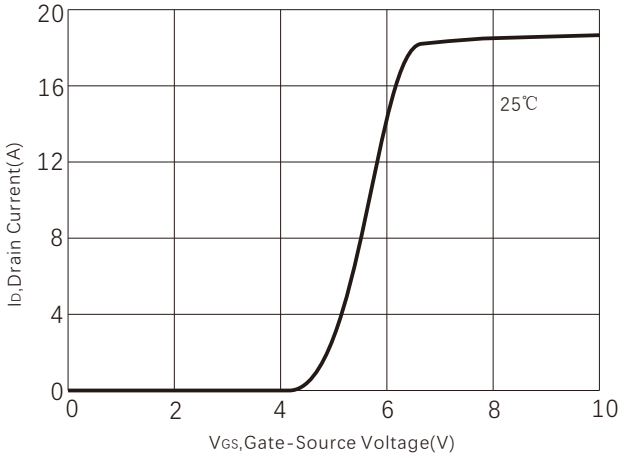


Figure 3. Power dissipation-ITO-220

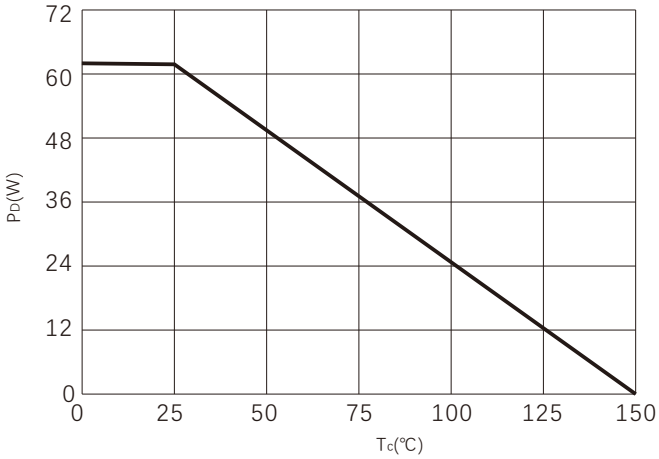


Figure 4. Capacitance

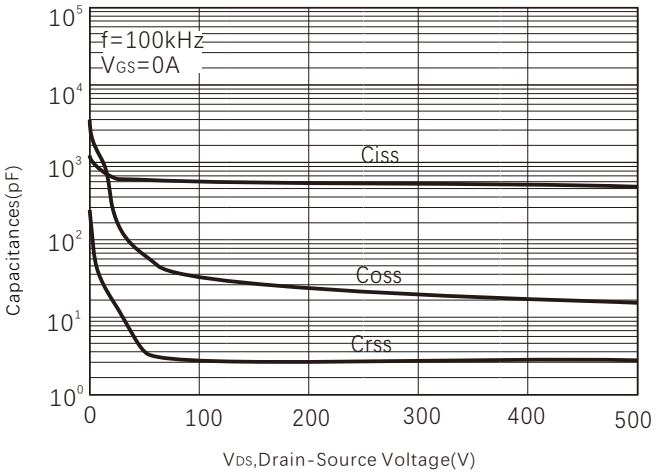


Figure 5.Gate charge

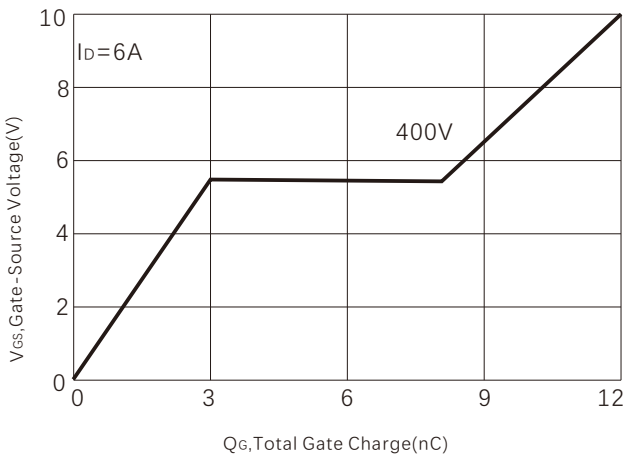


Figure 6.Source-Drain Diode Forward Voltage

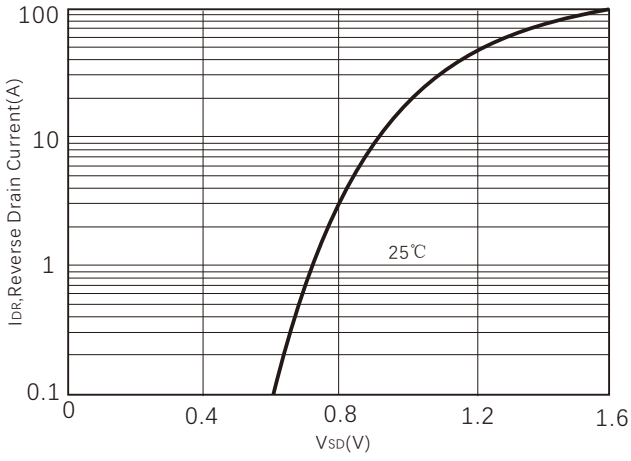


Figure7. $R_{DS(ON)}$ vs Junction Temperature

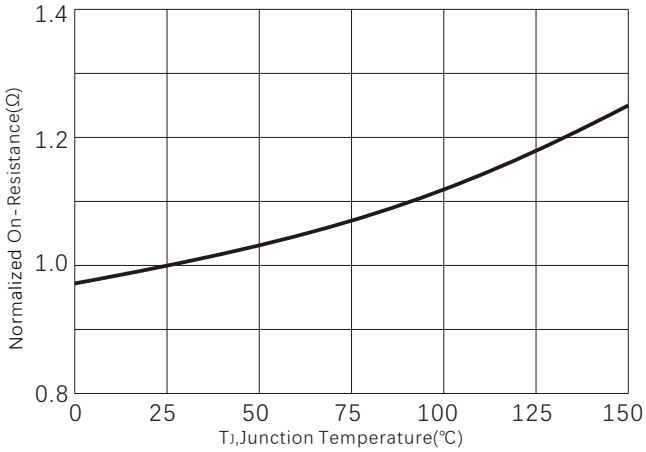


Figure 8.BV_{DSS} vs Junction Temperature

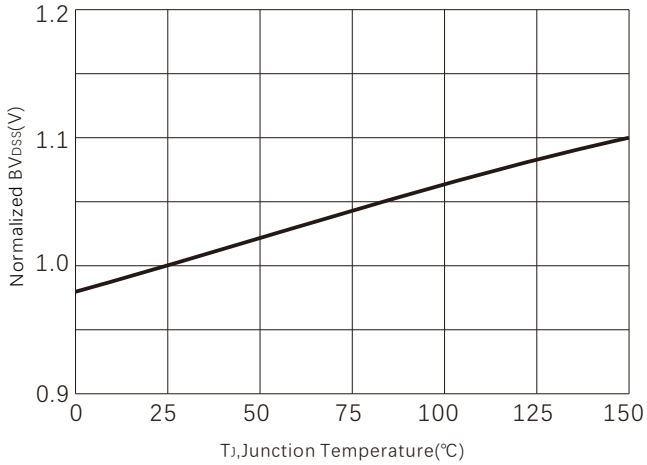


Figure 9. Safe operating area

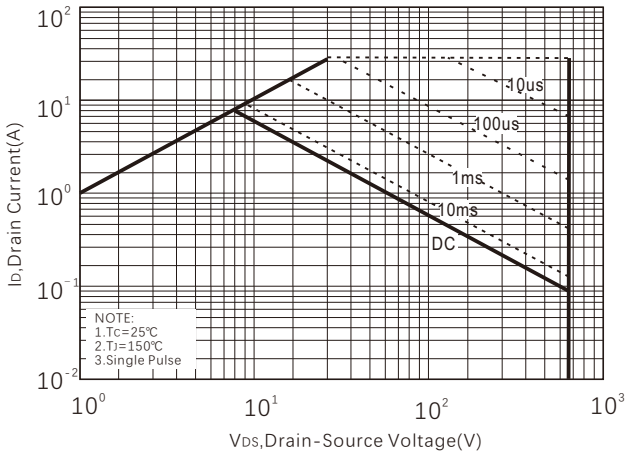


Figure10.Maximum Drain Current vs Temperature

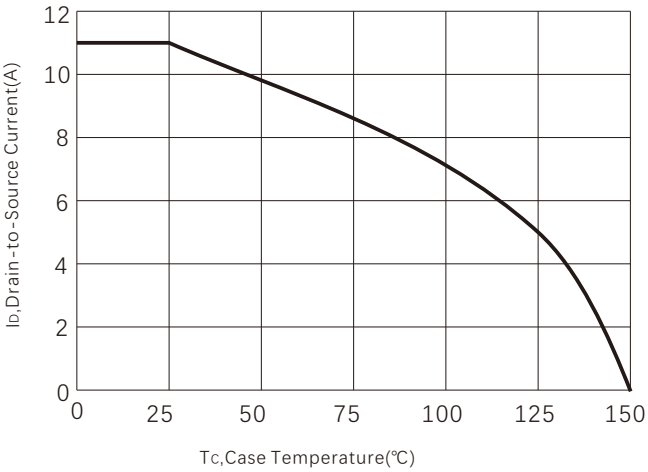
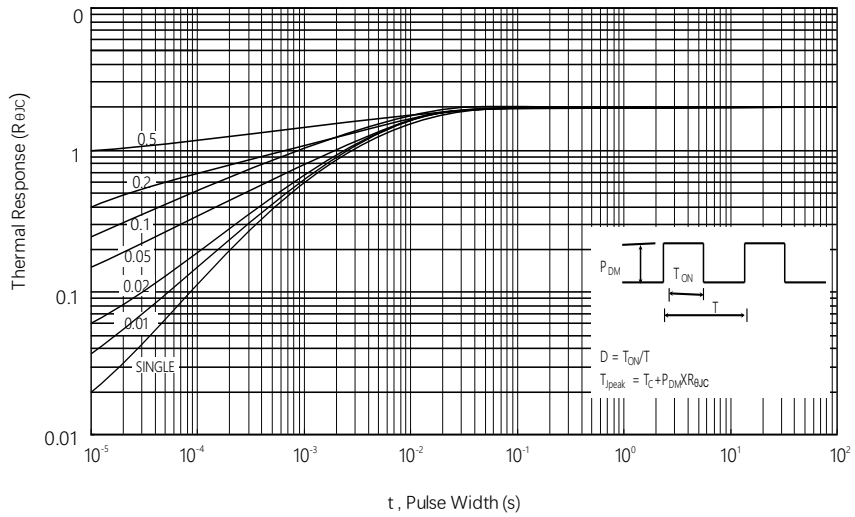
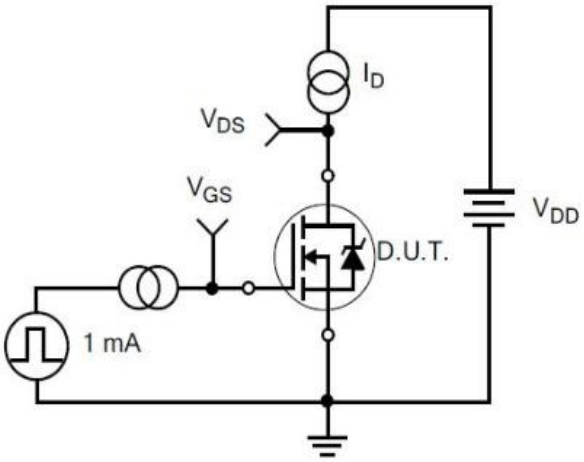


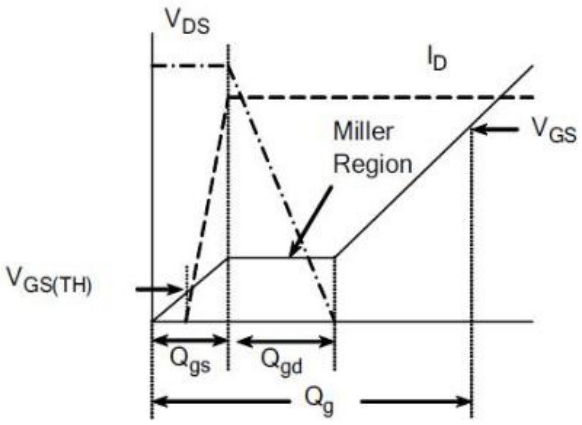
Figure 11. Maximum Transient Thermal Impedance



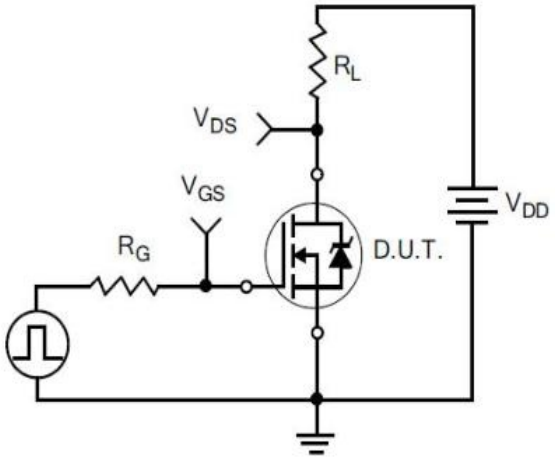
Typical Test Circuit



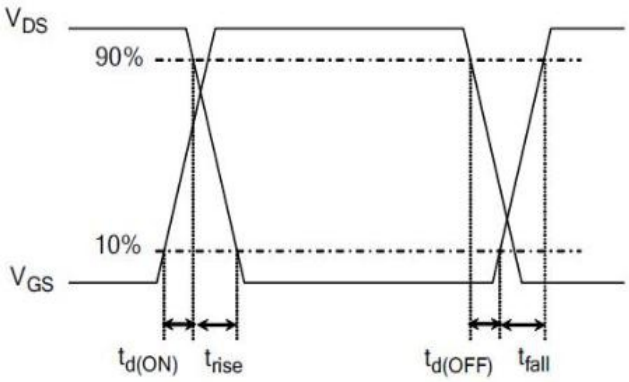
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

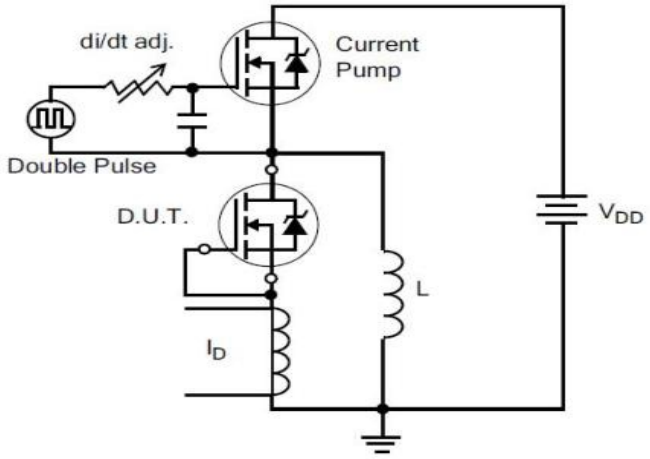


3) Resistive Switching Test Circuit

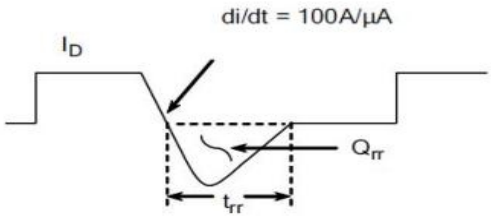


4) Resistive Switching Waveforms

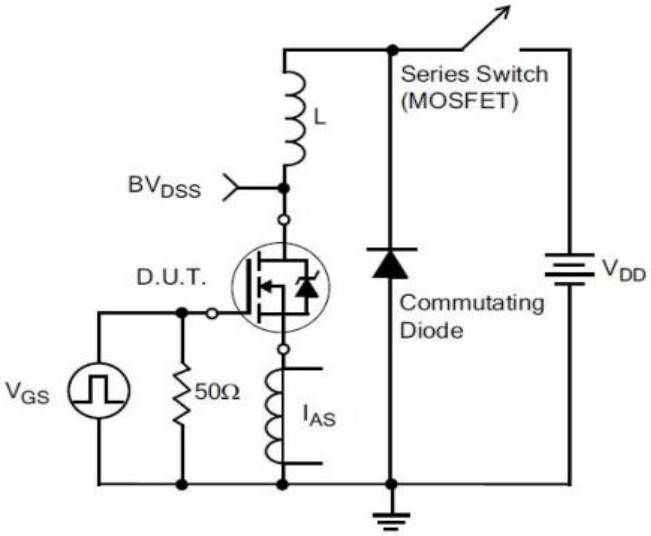
Typical Test Circuit



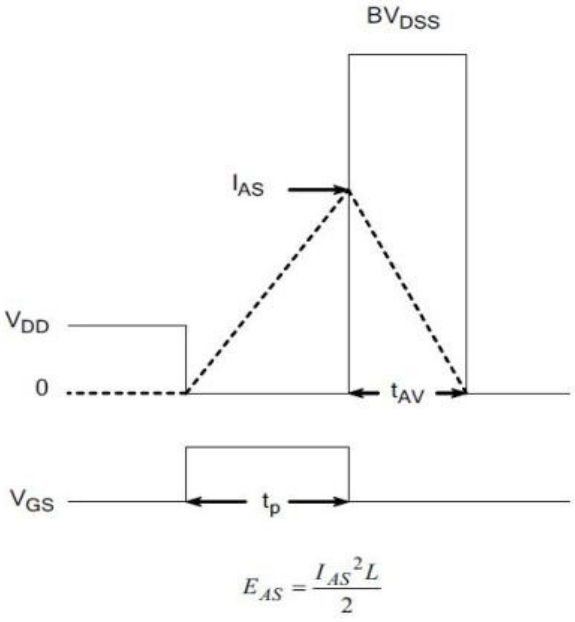
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



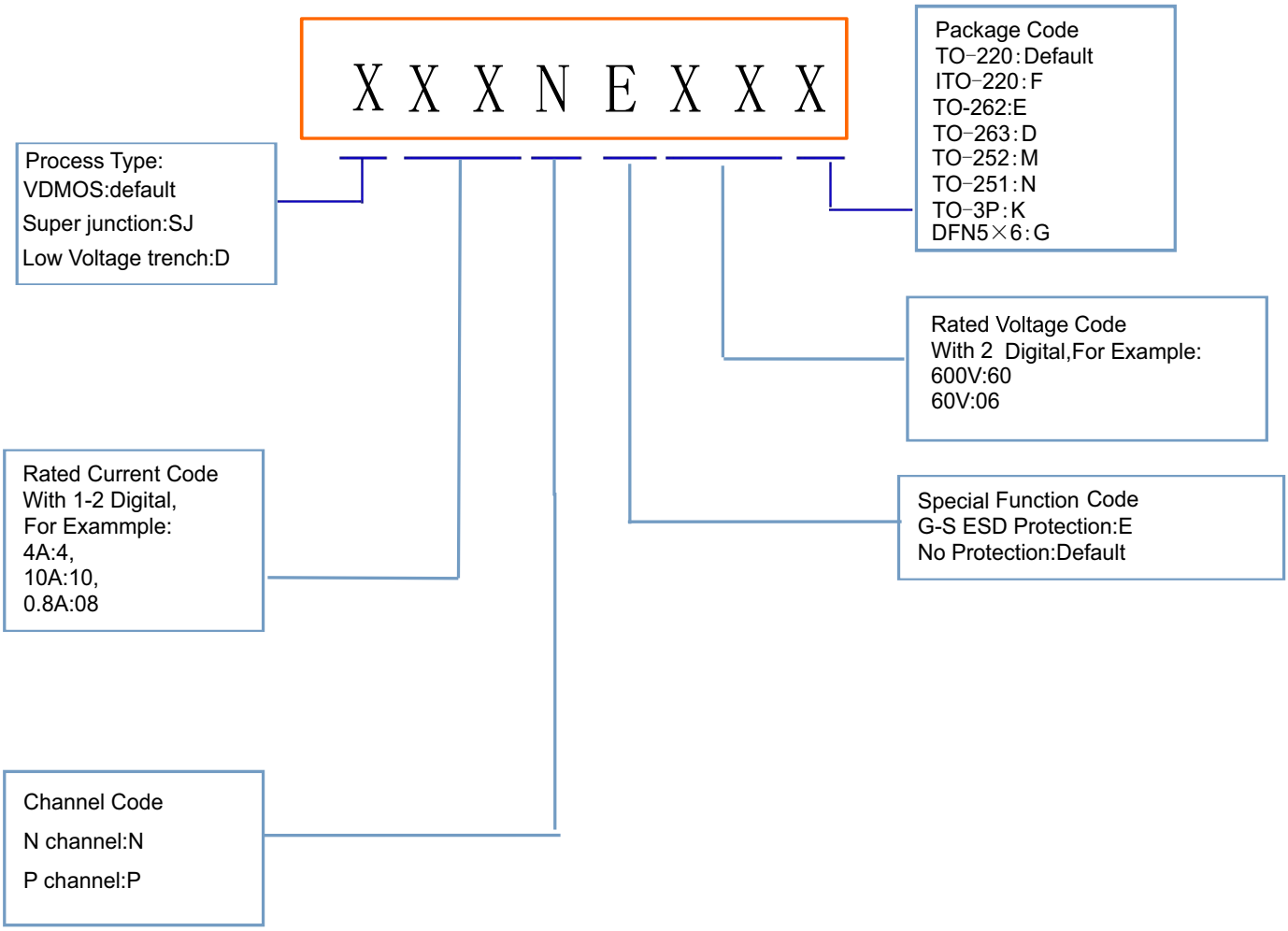
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

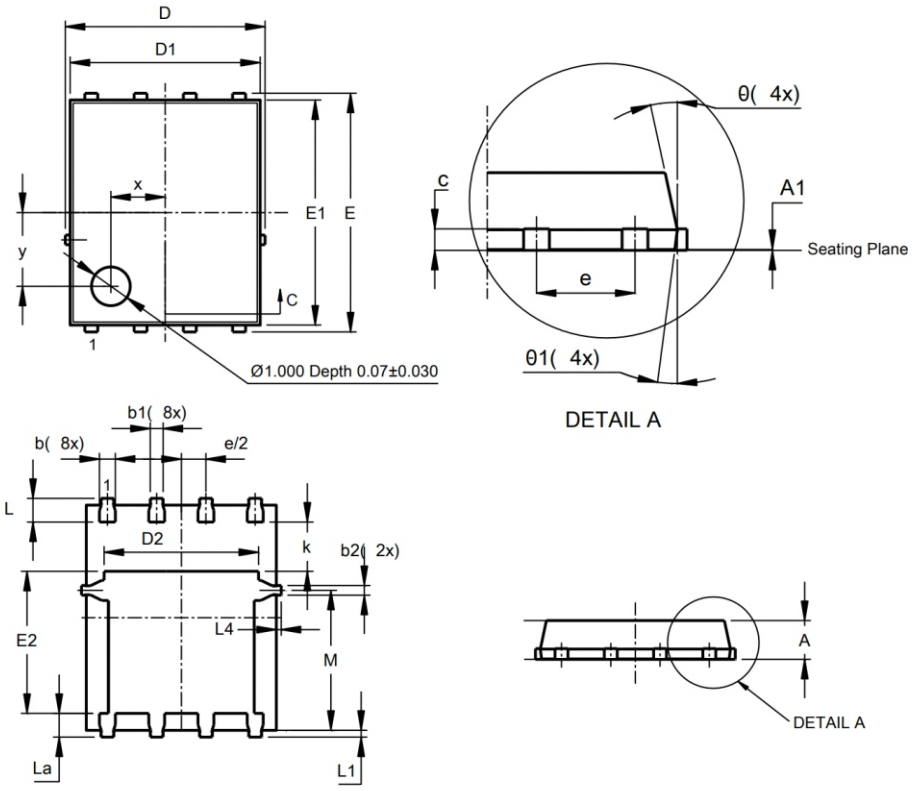
8) Unclamped Inductive Switching Waveforms

Product Names Rules



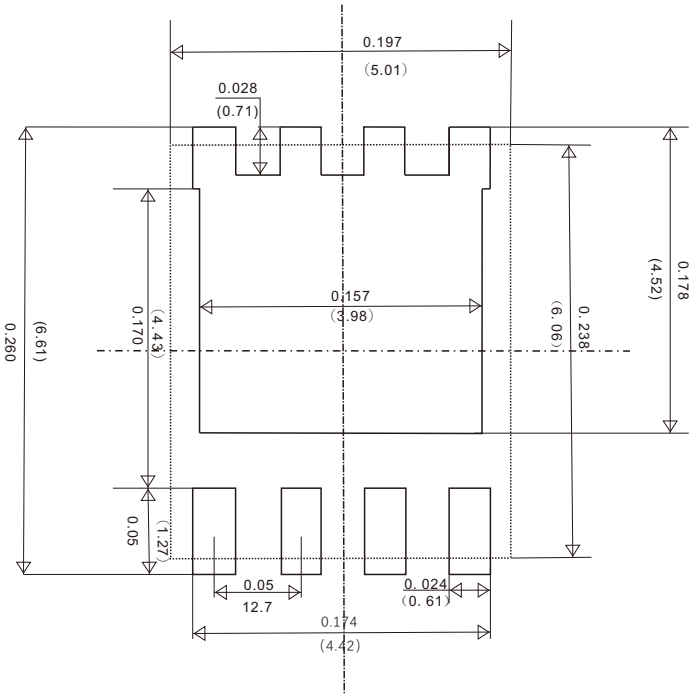
Dimensions

DFN5×6 PACKAGE OUTLINE DIMENSIONS



Dim	Min	Max	Type
A	0.90	1.10	1.00
b	0.23	0.41	0.32
b1	0.24	0.30	0.27
b2	0.16	0.32	0.23
c	0.17	0.27	0.22
D	-	-	5.01
D1	4.80	4.95	4.88
D2	-	-	3.98
E	-	-	6.06
E1	5.72	5.82	5.77
E2	3.42	3.52	3.47
k	-	-	1.33
L	0.56	0.66	0.61
La	0.57	0.67	0.63
L1	0.06	0.15	0.11
L4	-	-	0.06
M	3.00	3.20	3.08
Φ	10	11	10.39

Suggested Pad Layout



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