SEMICONDUCTOR

D018N10T

320A 100V N-Channel Enhancement Mode Power MOSFET

Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

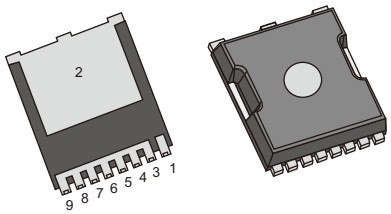
Product Summary			
V_{DS}	$R_{DS(on)}$ (mΩ) Typ	I_D (A)	Qg (Typ)
100V	1. 55 @ 10V 50A	320	165nc

Mechanical Data

- Case:TOLL Package

TOLL

D018N10T



Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

Ordering Information

Part No.	Package Type	Package	Quality(box)
D018N10T	TOLL	Tape & Reel	2000

Pin Definition:

1. Gate
2. Drain

3/4/5/6/7/8/9. Source

Block Diagram

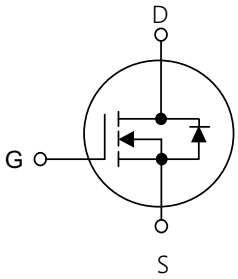


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	320	A
	T_C=100°C		208	
Pulsed Drain Current (Note 1)		I_{DM}	1200	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	2601	mJ
Power Dissipation	T_C=25°C	P_D	313	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient. Max	$R_{\theta JA}$	46	°C/W
Thermal resistance Junction to Case. Max	$R_{\theta JC}$	0.40	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	100	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	-	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=50A	-	1.55	1.8	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=50V,V_{GS}=0V,f=1MHz	-	14510	-	pF
Output Capacitance		C_{OSS}		-	1265	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	189	-	pF
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DS}=50V, V_{GS}=10V,R_G=3Ω,	-	37	-	ns
Turn-On Rise Time		t_R		-	112	-	ns
Turn-Off Delay Time		td(off)		-	85	-	ns
Turn-Off Fall Time		tf		-	115	-	ns
Total Gate Charge		Q_G	V_{DS}=50V,I_D=50A, V_{GS}=10V	-	165	-	nC
Gate-Source Charge		Q_{GS}		-	67	-	nC
Gate-Drain Charge		Q_{GD}		-	35	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=50A	-	-	1.2	V
Reverse Recovery Time		trr	I_F=30A,dI_F/dt=500A/μs	-	47	-	ns
Reverse Recovery Charge		Q_{RR}	I_F=30A,dI_F/dt=100A/μs	-	388	-	nC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L = 0.5mH, R_G = 25Ω,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

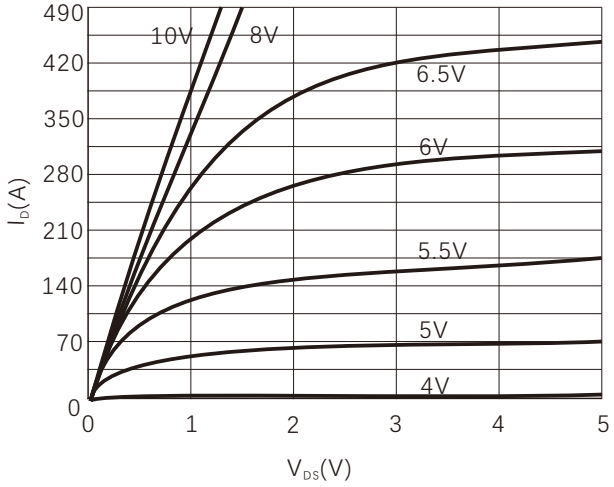


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

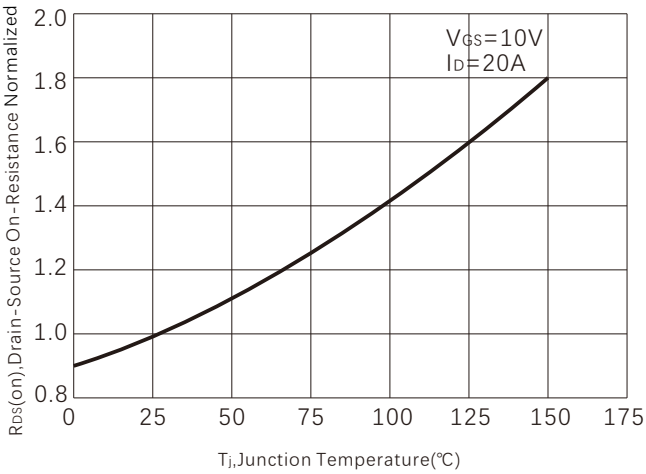


Figure 3.On-Resistance vs.Drain Current

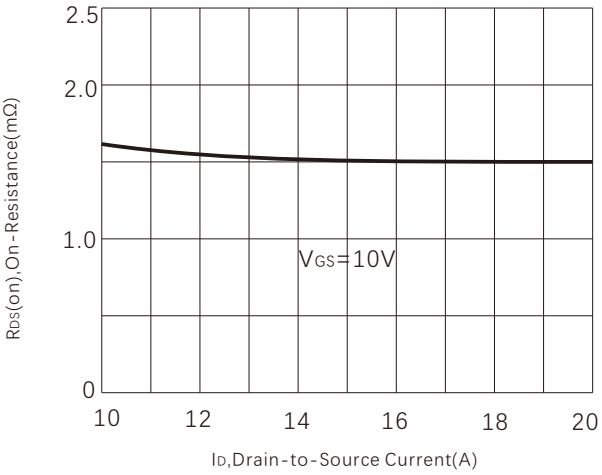


Figure 4. Capacitance

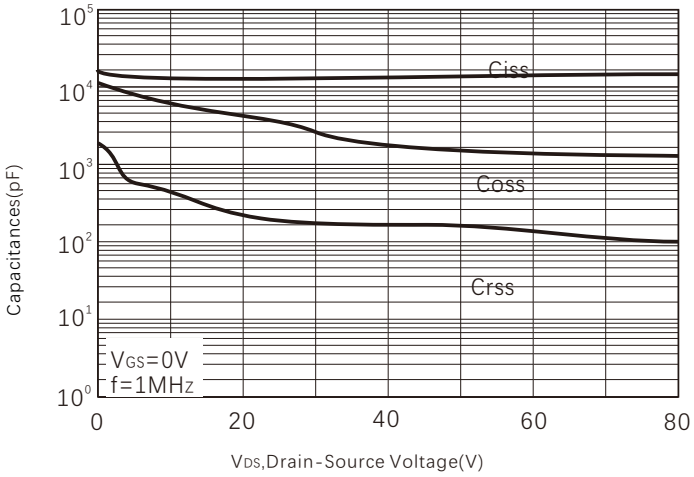


Figure 5.Gate charge

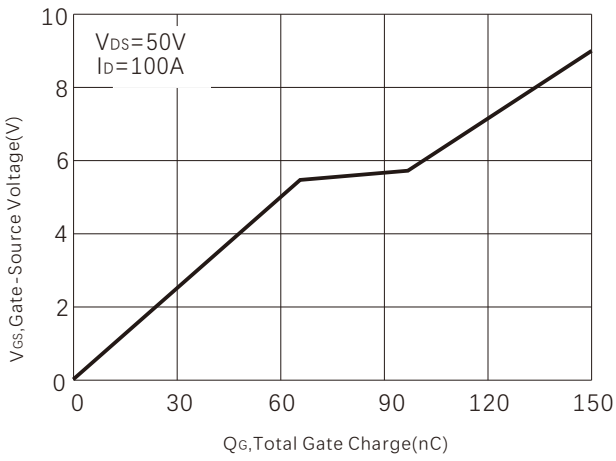


Figure 6.Source-Drain Diode Forward Voltage

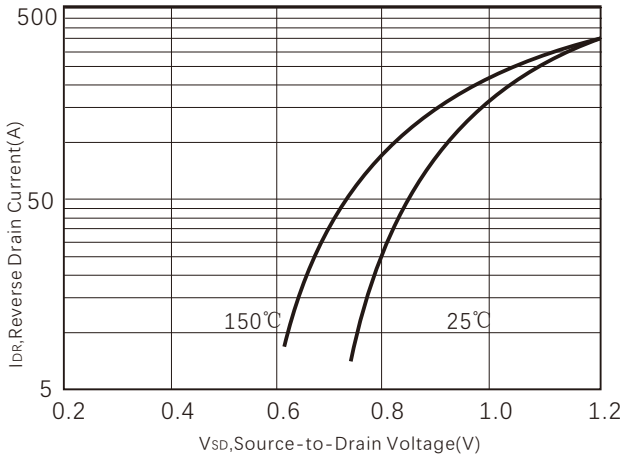


Figure7.Maximum Drain Current vs Temperature

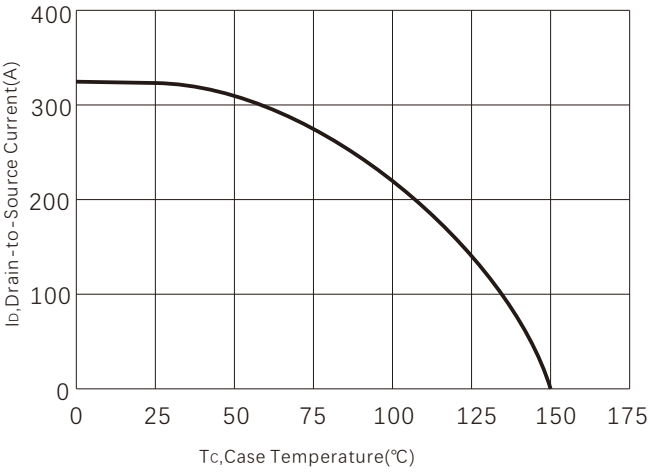


Figure 8. Power dissipation

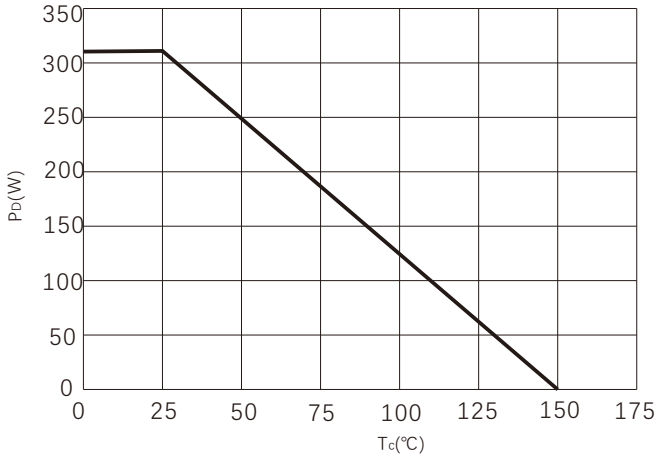


Figure 9. Safe operating area

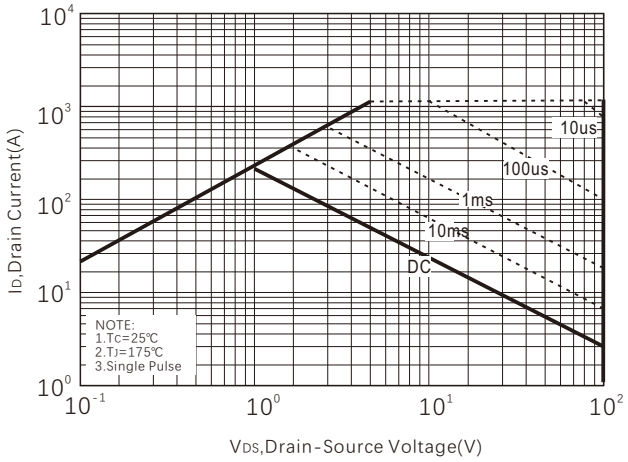
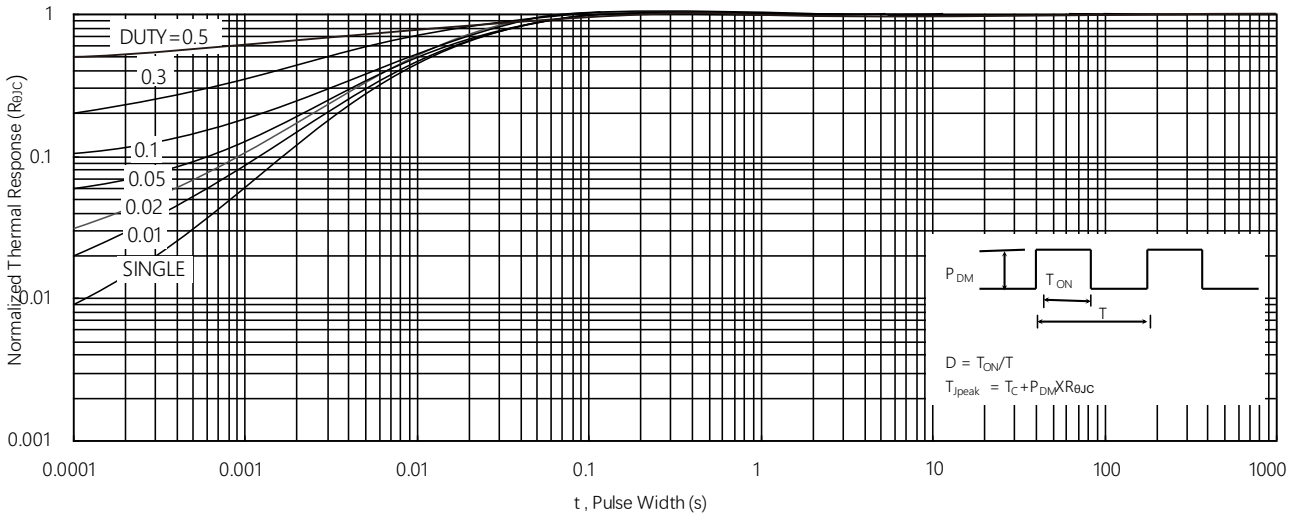
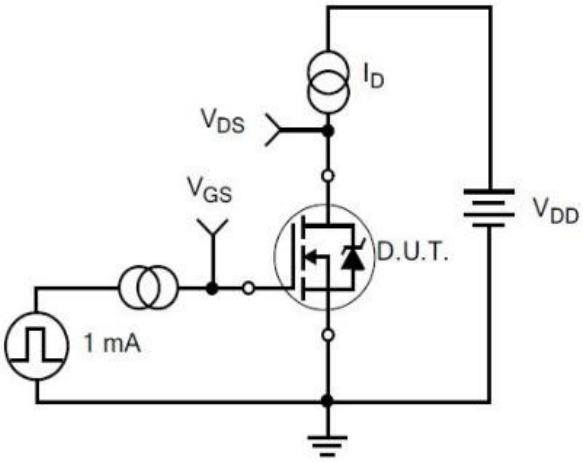


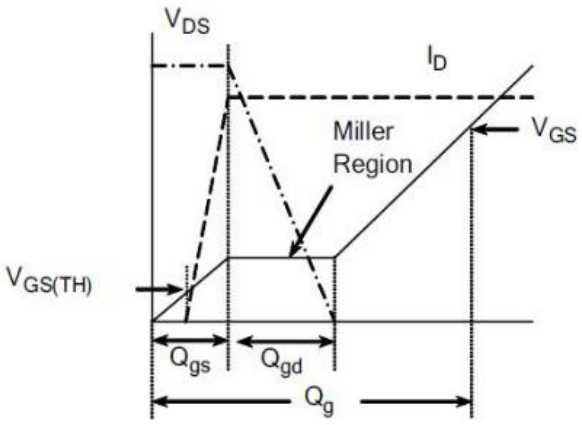
Figure 10.Normalized Maximum Transient Thermal Impedance



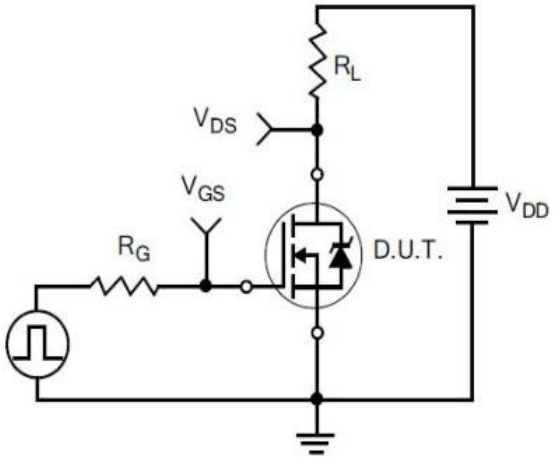
Typical Test Circuit



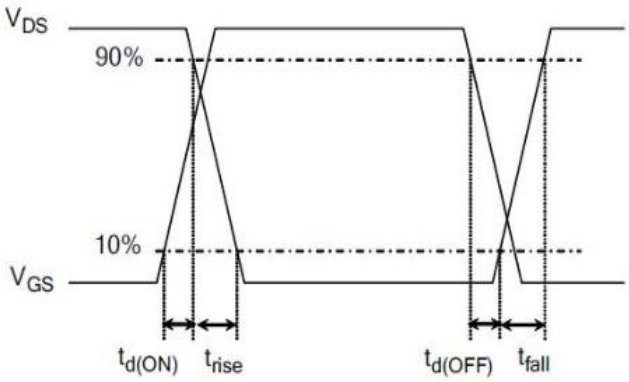
1) Gate Charge Test Circuit



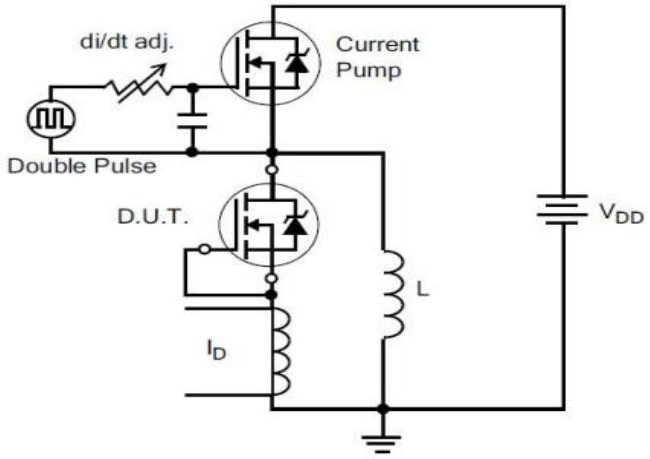
2) . Gate Charge Waveform



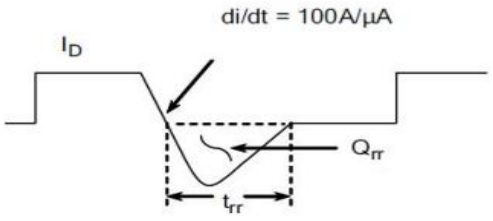
3) Resistive Switching Test Circuit



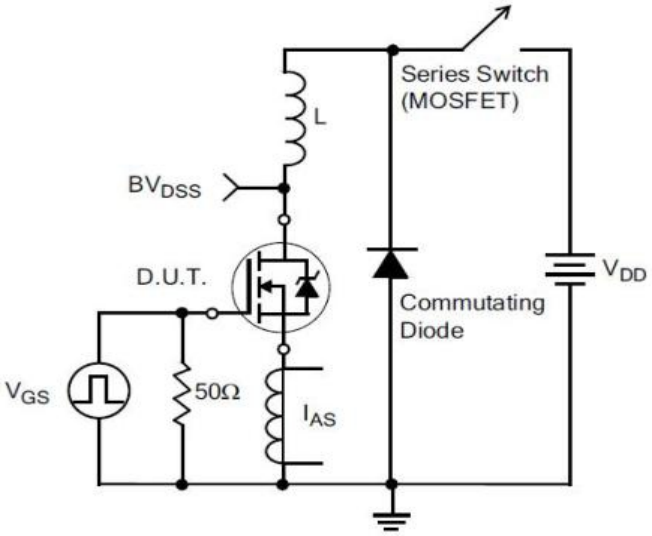
4) Resistive Switching Waveforms



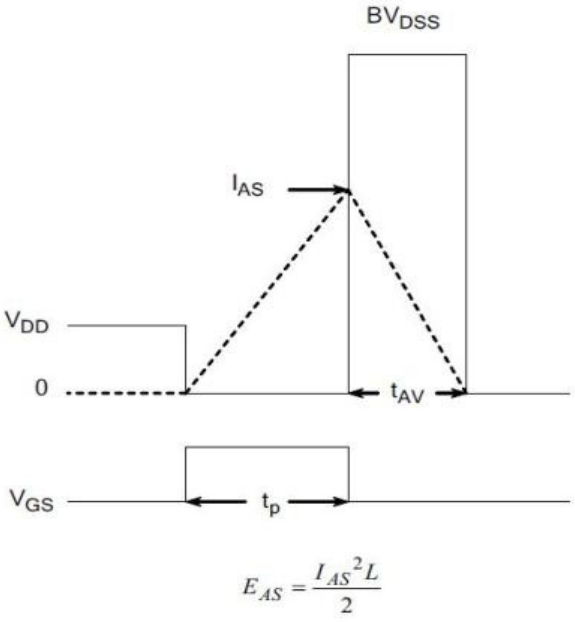
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



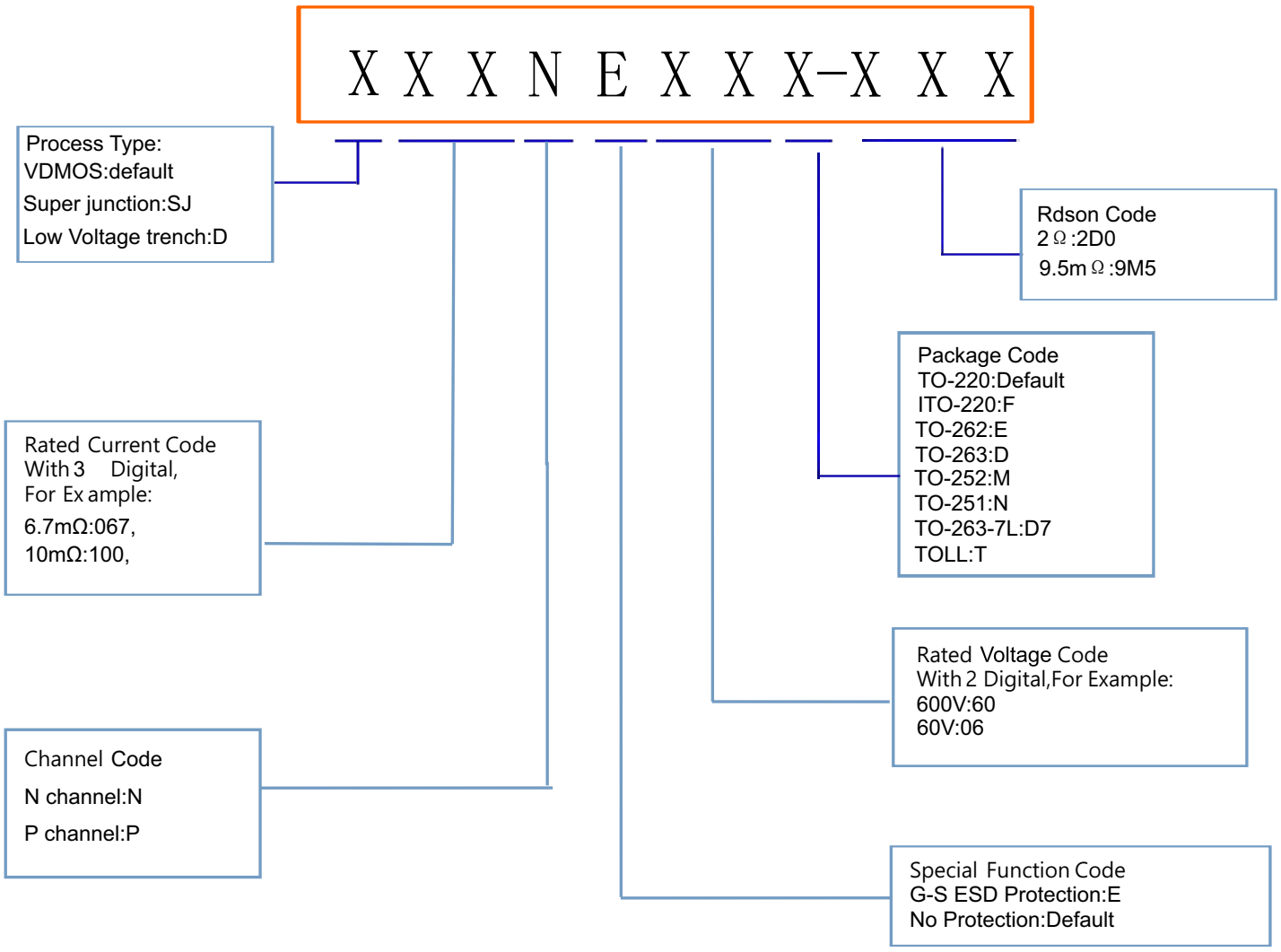
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

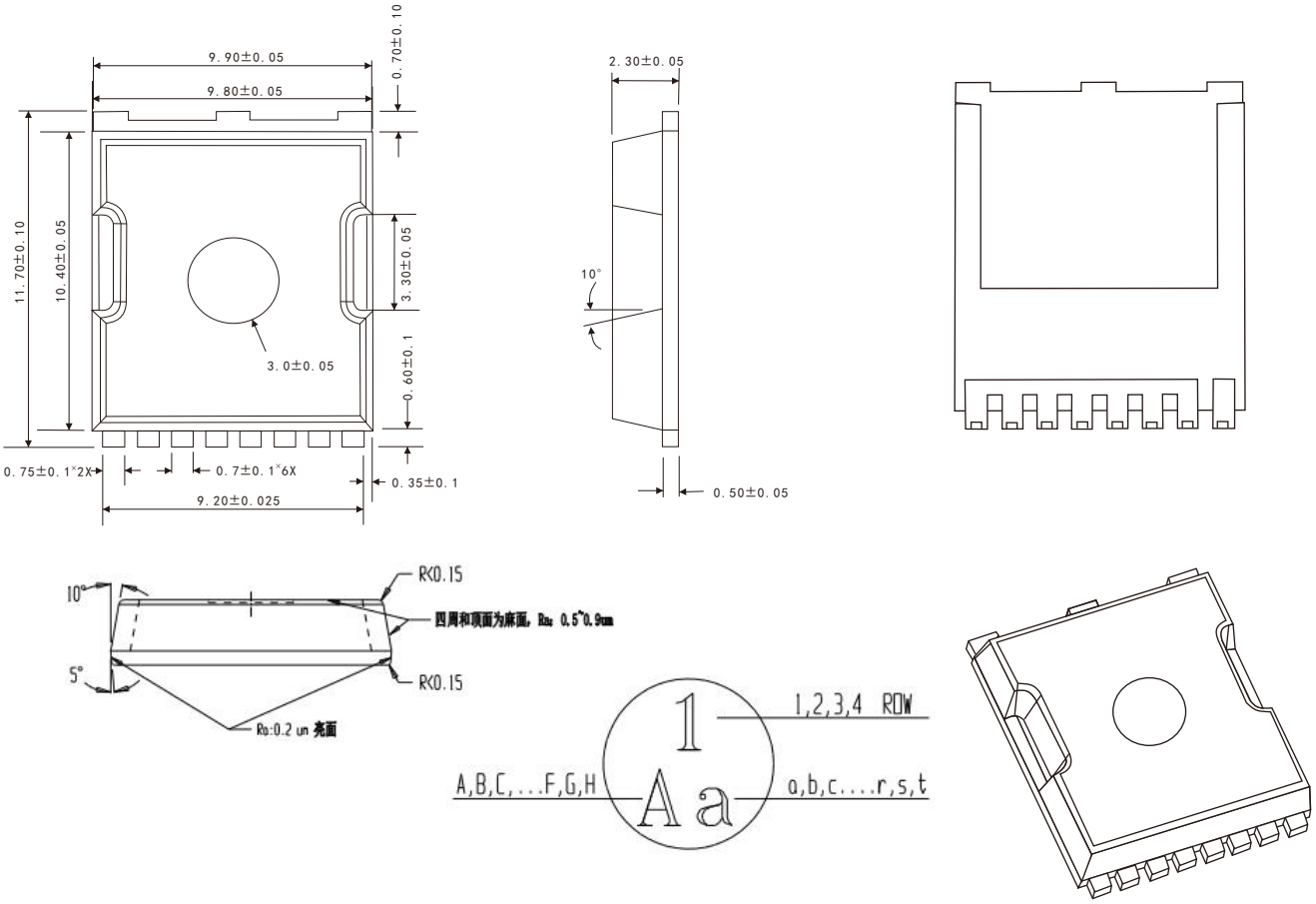
8) Unclamped Inductive Switching Waveforms

Product Names Rules

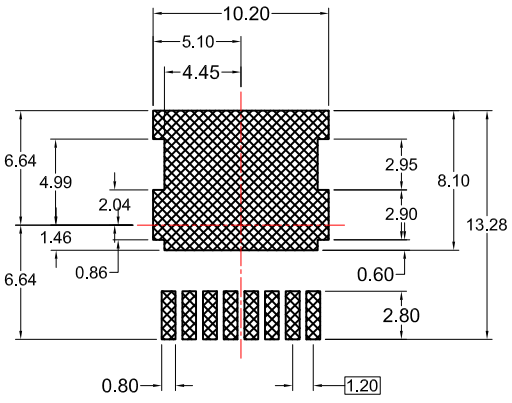


Dimensions

TOLL PACKAGE OUTLINE DIMENSIONS



Suggested Pad Layout



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