SEMICONDUCTOR

D190N10 Series

190A 100V N-Channel Enhancement Mode Power MOSFET

Features

- Uses advanced SGT technology
- Low on-resistance
- Low gate charge and input capacitance
- 100% avalanche tested

Product Summary			
V_{DS}	$R_{DS(on)}$ (mΩ) Typ	I_D (A)	Qg (Typ)
100V	3.3@10V, 50A	190	95nc

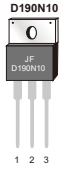
Mechanical Data

- Case:TO-220,TO-263 Package

Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

TO-220



TO-263

Ordering Information

Part No.	Package Type	Package	Quality(box)
D190N10	TO-220	Tube	1000
D190N10D	TO-263	Tape & Reel	800

Pin Definition:

1. Gate
2. Drain
3. Source

Block Diagram

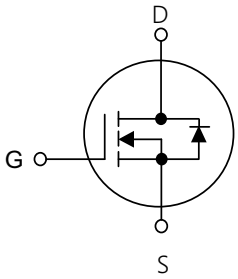


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	D190N10/D190N10D	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	190	A
	T_C=100°C		118	
Pulsed Drain Current (Note 1)		I_{DM}	480	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	1056	mJ
Power Dissipation T_C=25°C		P_D	225	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	D190N10/D190N10D	Unit
Thermal resistance Junction to Ambient.Max	$R_{\theta JA}$	60	°C/W
Thermal resistance Junction to Case.Max	$R_{\theta JC}$	0.55	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	100	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=25V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-25V,V_{DS}=0V	-	-	-100	nA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	-	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=50A	-	3.3	4.0	mΩ
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=50V,V_{GS}=0V,f=1MHz	-	7300	-	pF
Output Capacitance		C_{OSS}		-	2700	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	309	-	pF
Gate Resisitance		R_G	V_{DD}=0V,V_{GS}=0V,f=1MHz	-	1.6	-	Ω
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DD}=50V, V_{GS}=10V,R_L=3Ω,	-	32	-	ns
Turn-On Rise Time		t_R		-	45	-	ns
Turn-Off Delay Time		td(off)		-	52	-	ns
Turn-Off Fall Time		tf		-	31	-	ns
Total Gate Charge		Q_G	V_{DS}=50V,I_D=50A, V_{GS}=10V	-	95	-	nC
Gate-Source Charge		Q_{GS}		-	25	-	nC
Gate-Drain Charge		Q_{GD}		-	21	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=50A	-	-	1.2	V
Maximum Continuous Drain-Source Diode Forward Current		I_S		-	-	190	A
Reverse Recovery Time		trr	V_{GS}=0V, I_{SD}=30A dI$_F$/dt=500A/μs (Note 1)	-	85	-	ns
Reverse Recovery Charge		Q_{RR}		-	254	-	nC

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L = 0.5mH, R_G = 25Ω,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%
4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

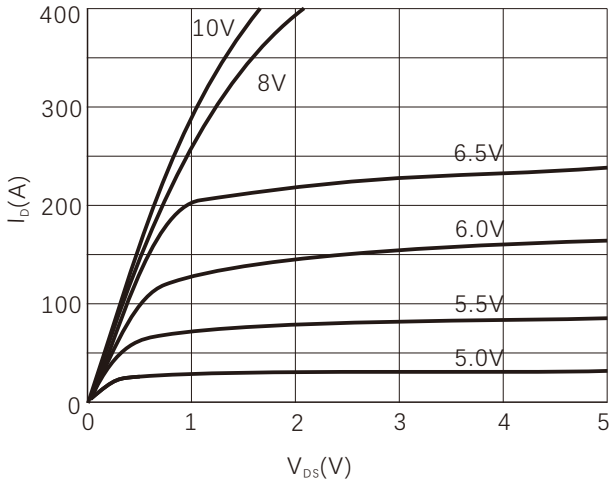


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

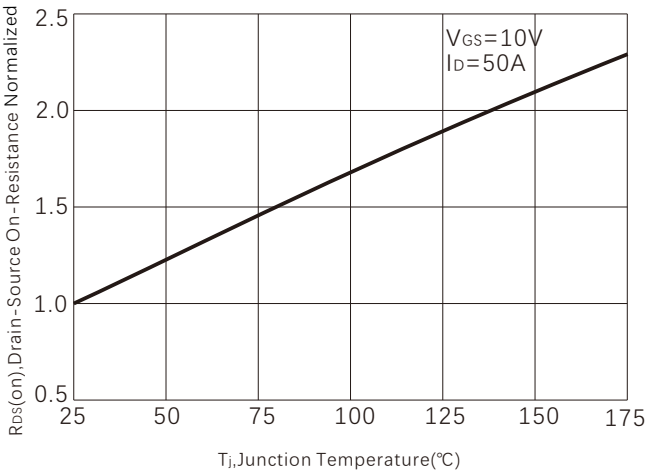


Figure 3.On-Resistance vs.Drain Current

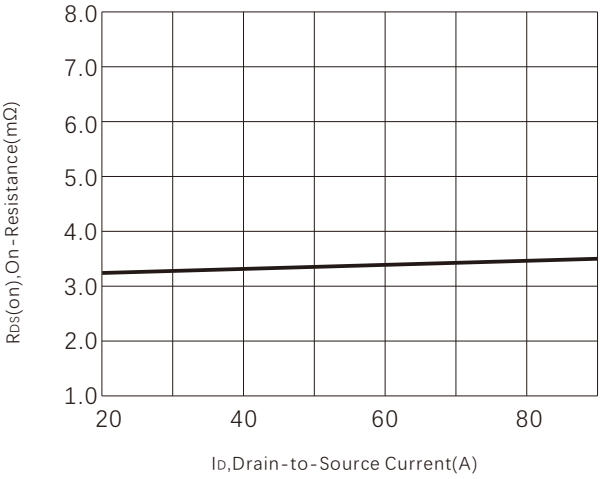


Figure 4. Capacitance

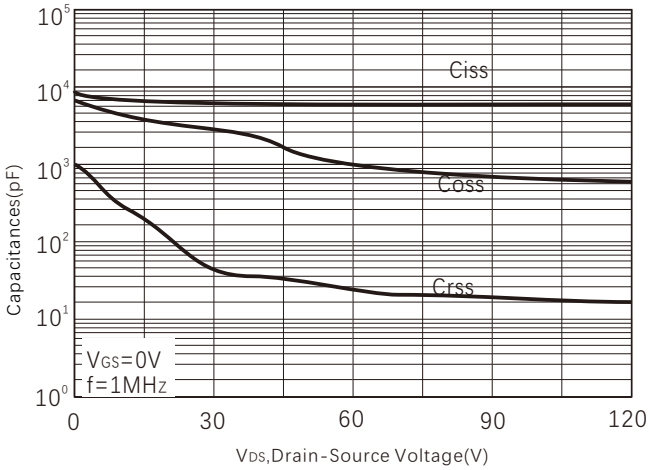


Figure 5.Gate charge

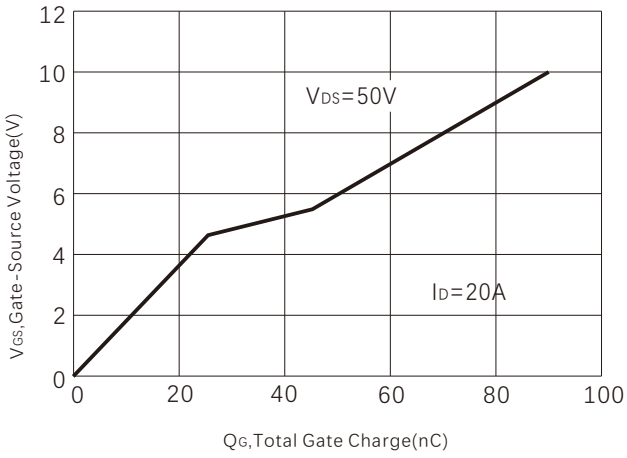


Figure 6.Source-Drain Diode Forward Voltage

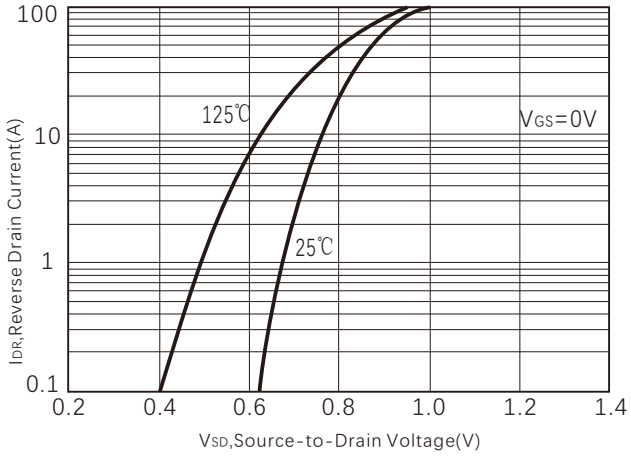


Figure7.Maximum Drain Current vs Temperature

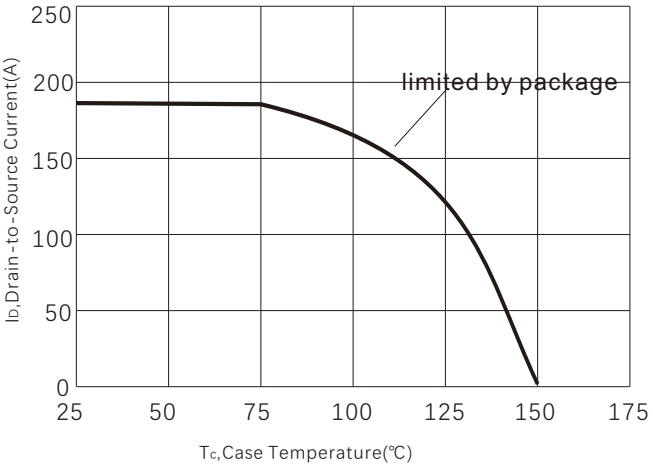


Figure 8.On-Resistance vs.Gate Voltage

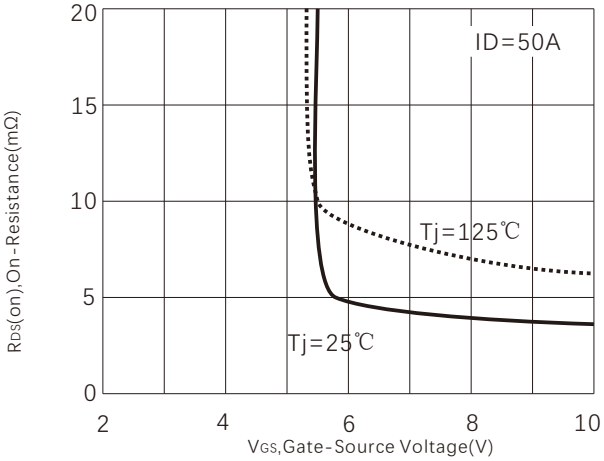


Figure 9. Safe operating area

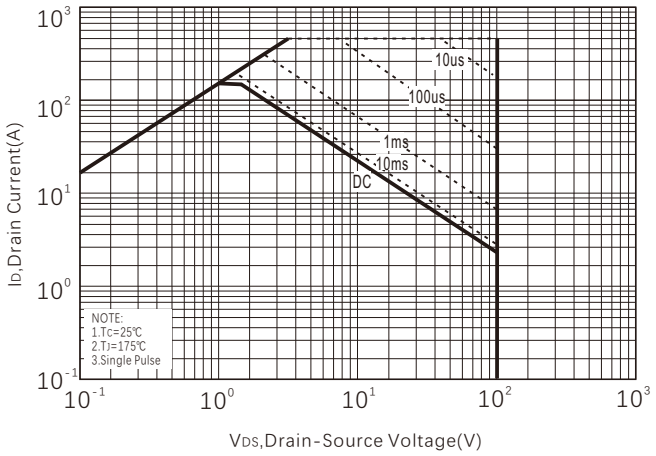


Figure 10. Power dissipation

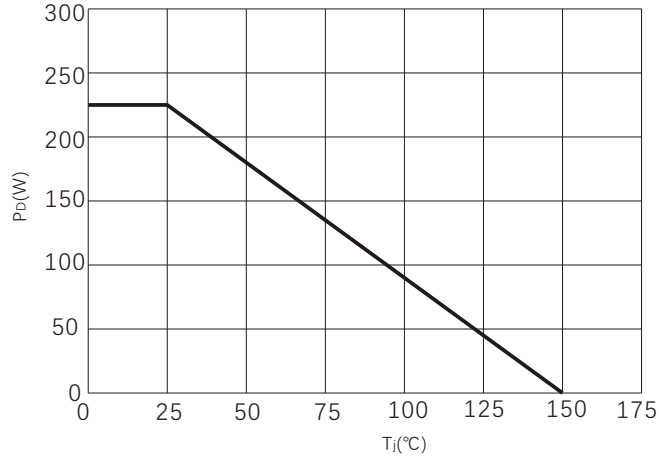
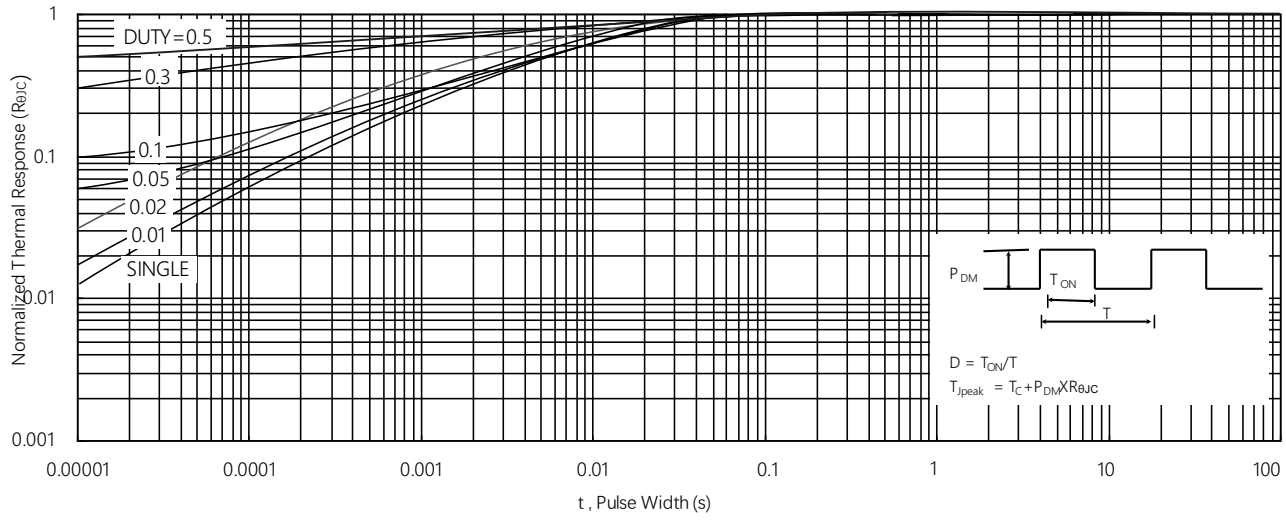
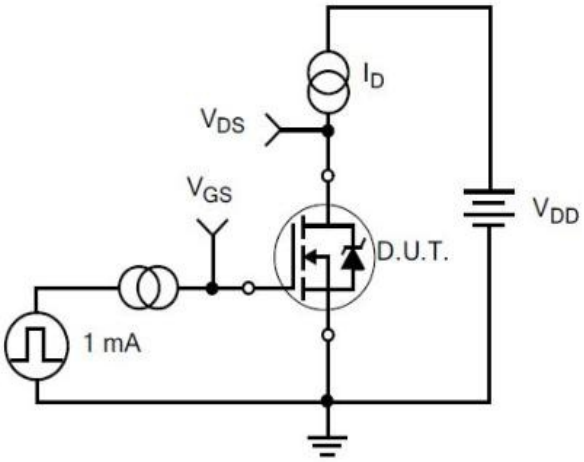


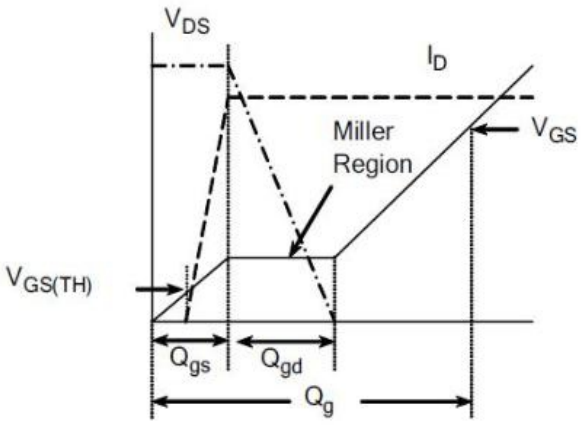
Figure 11.Normalized Maximum Transient Thermal Impedance



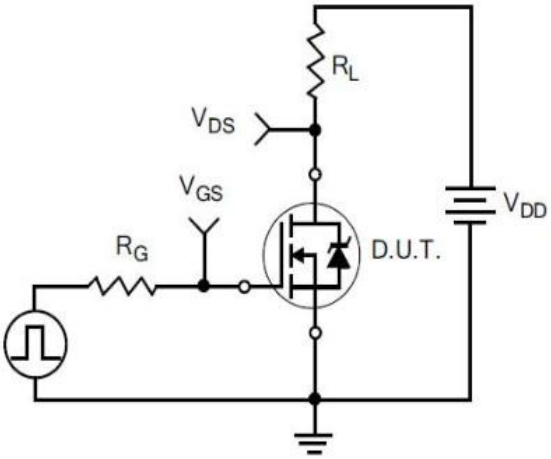
Typical Test Circuit



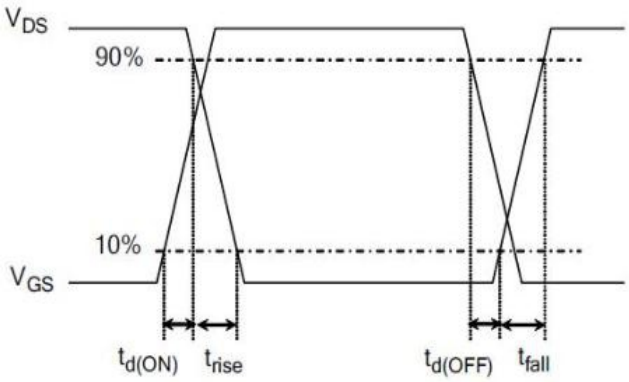
1) Gate Charge Test Circuit



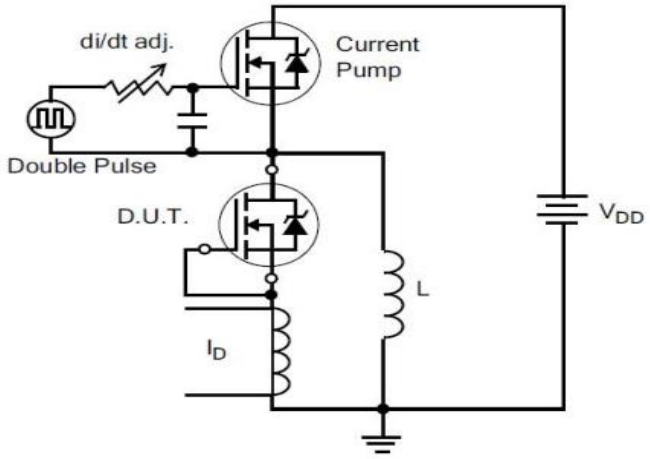
2) . Gate Charge Waveform



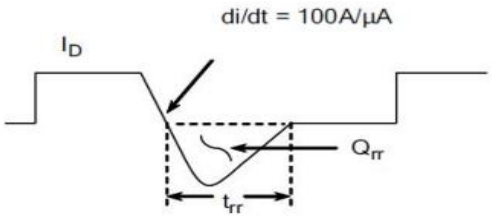
3) Resistive Switching Test Circuit



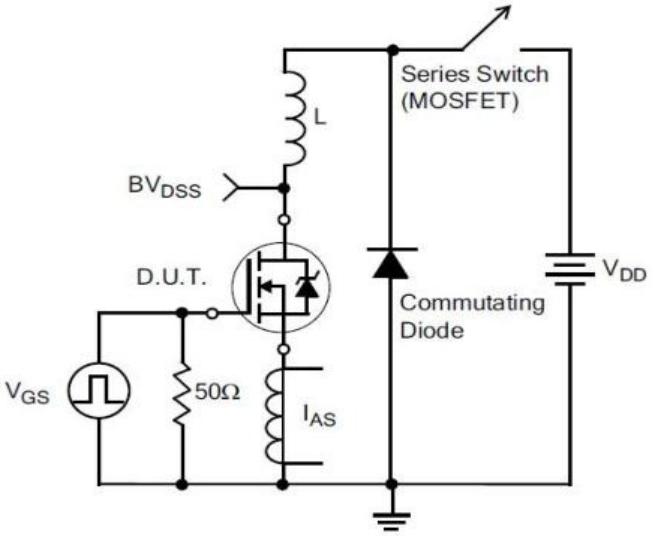
4) Resistive Switching Waveforms



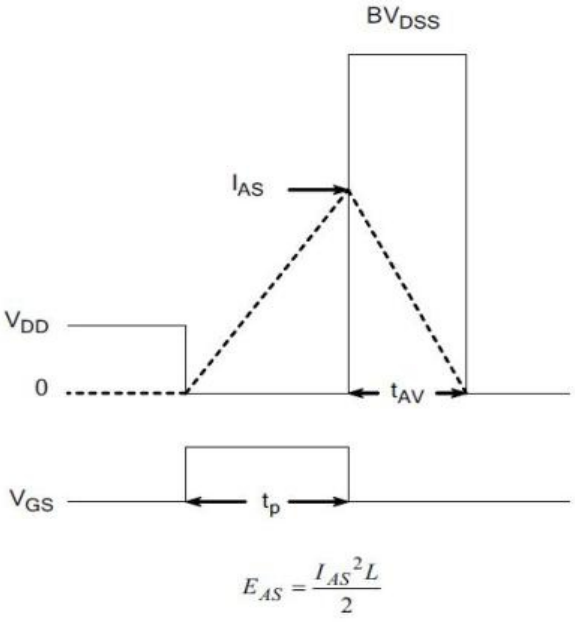
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



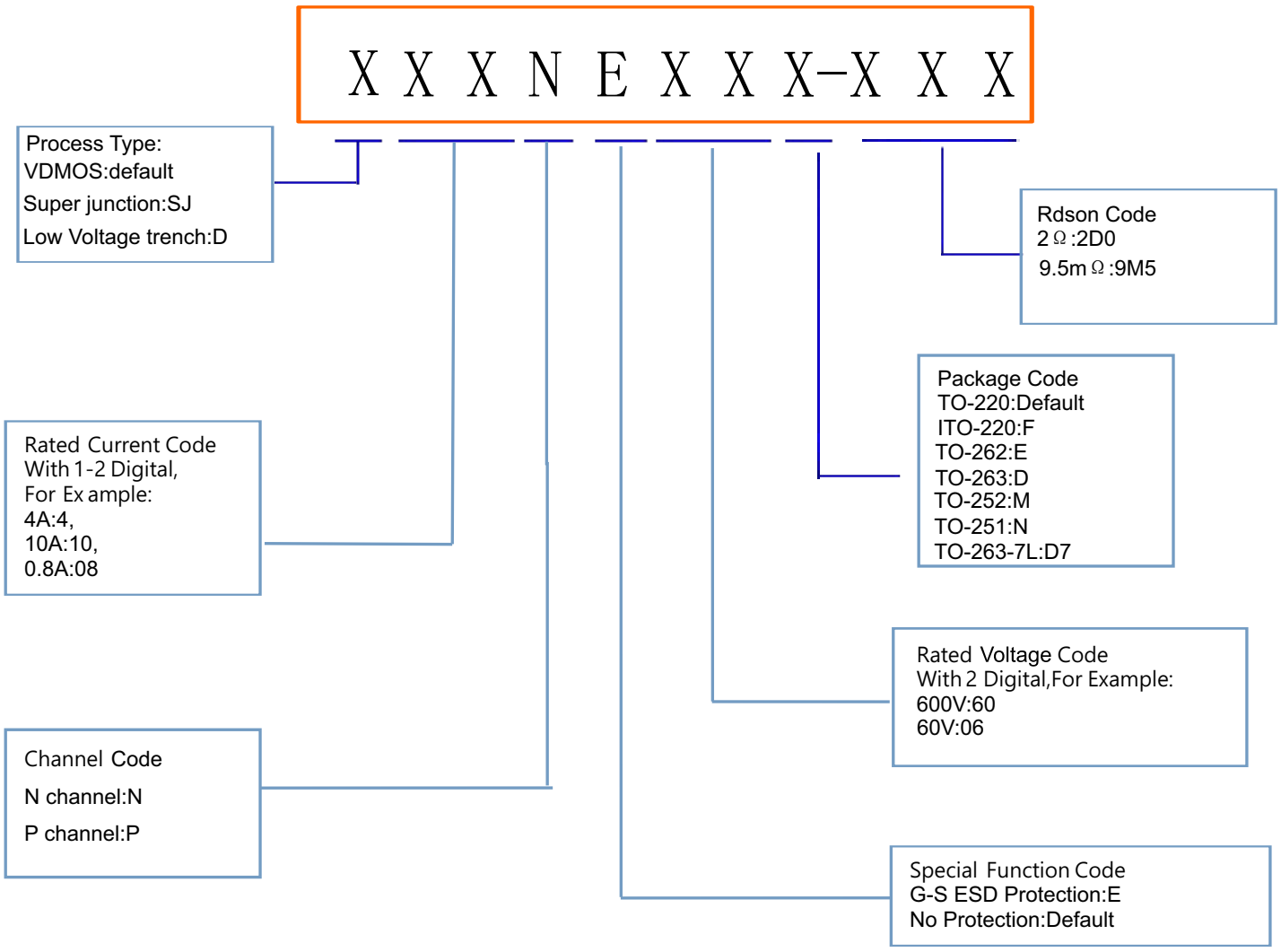
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

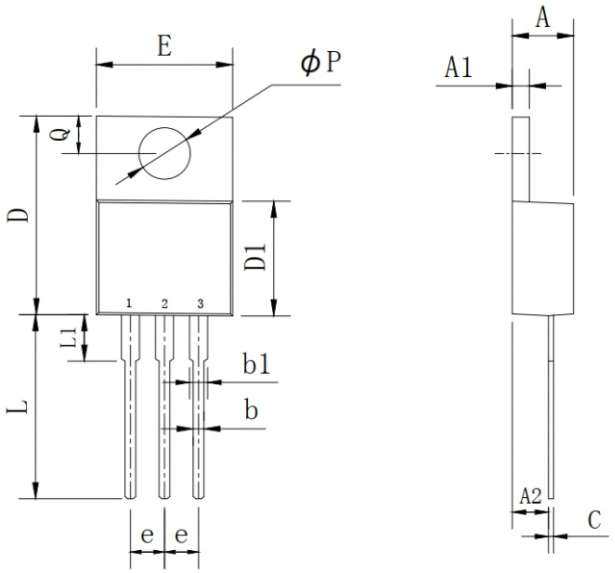
8) Unclamped Inductive Switching Waveforms

Product Names Rules



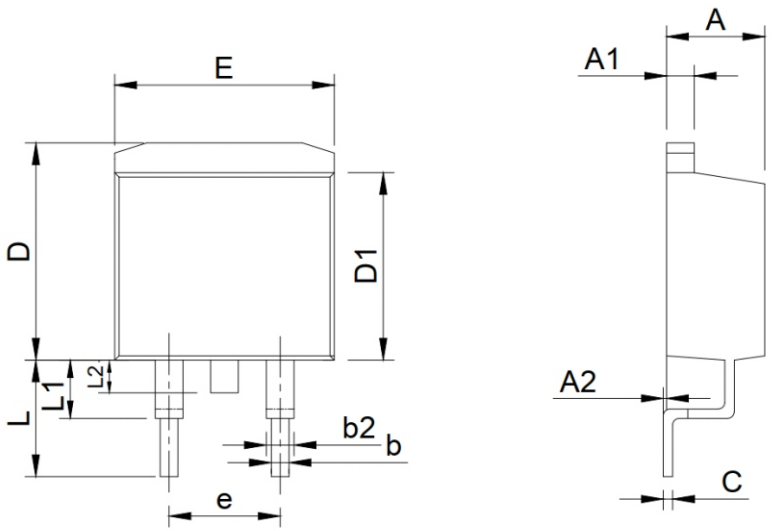
Dimensions

TO-220 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	4.25	4.87	0.167	0.192
A1	1.07	1.47	0.042	0.058
A2	2.03	2.92	0.080	0.115
b	0.51	1.11	0.020	0.044
b1	0.97	1.6	0.038	0.063
C	0.3	0.7	0.012	0.028
D	14.6	15.9	0.575	0.626
D1	8.04	9.3	0.317	0.366
E	9.57	10.57	0.377	0.416
e	2.34	2.74	0.092	0.108
L	12.58	14.3	0.495	0.563
L1	2.8	4.2	0.110	0.165
P	3.4	4.14	0.134	0.163
Q	2.45	3	0.096	0.118

TO-263 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	4.25	4.87	0.167	0.192
A1	1.07	1.47	0.042	0.058
A2	0	0.25	0.000	0.010
b	0.61	1.01	0.024	0.040
b1	1.2	1.34	0.047	0.053
C	0.3	0.6	0.012	0.024
D	9.48	10.84	0.373	0.427
D1	8.49	9.3	0.334	0.366
E	9.7	10.31	0.382	0.406
e	4.88	5.28	0.192	0.208
L	4.46	5.85	0.176	0.230
L1	1.33	2.33	0.052	0.092
L2	0	2.2	0.000	0.087

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