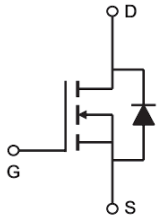
SEMICONDUCTOR

GSR4510T

N-Channel Super Trench PowerMOSFET

Description

The GSR4510T uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.



Schematic Diagram

General Features

- V_{DS} =45V,I_D =20A
  $R_{DS(ON)}$=10m Ω (typical) @ V_{GS}=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS and Rg tested

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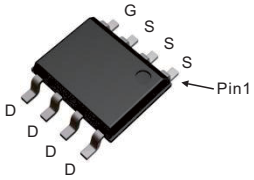

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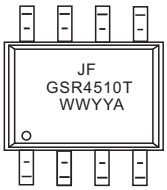

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
GSR4510T	GSR4510T	SOP-8	330mm	12mm	4K/Reel

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	45	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous（Silicon Limited） [A]	I_D	20	A
Drain Current-Continuous(T_C=100℃)	I_D(100°C)	6.5	A
Pulsed Drain Current（Package Limited） [B]	I_{DM}	80	A
Maximum Power Dissipation [A]	P_D	1.7	W
Single pulse avalanche energy L=0.3mH	E_{AS}	79	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Thermal Characteristic

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	$R_{\theta JA}$	59	75	℃/W
Maximum Junction-to-Lead [C]	$R_{\theta JL}$	16	24	℃/W

GSR4510T

Electrical Characteristics (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	45	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=45V,V_{GS}=0V	-	-	100	nA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=10A			10	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=10A		75		S
Dynamic Characteristics						
Input Capacitance	Ciss	V_{GS}=0V,V_{DS}=20V f=1.0MHz		1500	1950	pF
Output Capacitance	Coss			215		pF
Reverse Transfer Capacitance	Crss			315		pF
Switching Characteristics						
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=20V R_L=2Ω,R_{GEN}=3Ω		6. 4		nS
Turn-on Rise Time	t_f			17. 2		nS
Turn-Off Delay Time	$t_{D(off)}$			29.6		nS
Turn-Off Fall Time	tr			16.8		nS
Total Gate Charge	Qg	V_{GS}=10V,V_{DS}=20V，I_D=10A		27.2	37	nC
Gate-Source Charge	Qgs			4.5		nC
Gate-Drain Charge	Qgd			6.4		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	Vsd	I_S=1A,V_{GS}=0V		0.72	1.0	V
Diode Forward Current	I_S				2. 5	A
Reverse Recovery Time	trr	I_F=10A,dI/dt=100A/μs		39	40	nS
Reverse Recovery Charge	Qrr			19		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25℃. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using t<= 300μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.

F. The current rating is based on the t<= 10s thermal resistance rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

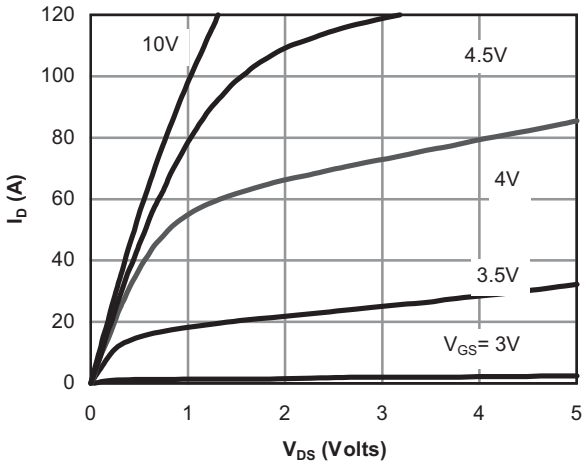

Figure 1: On-Region Characteristics

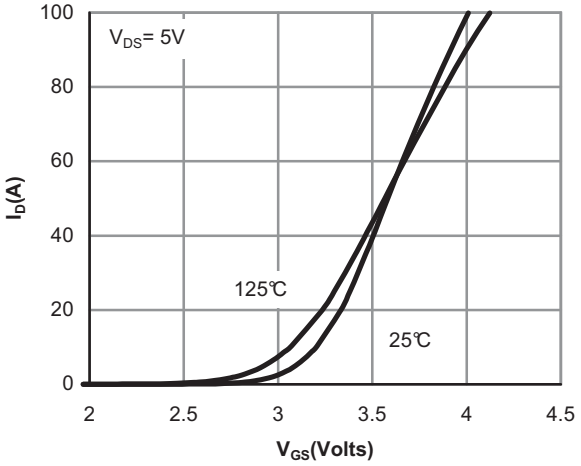

Figure 2: Transfer Characteristics

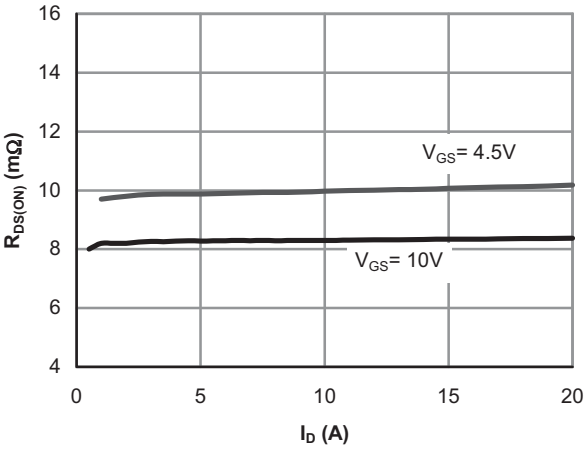

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

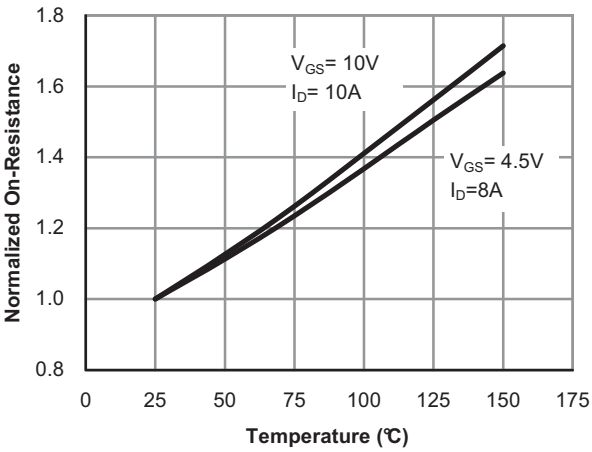

Figure 4: On-Resistance vs. Junction Temperature

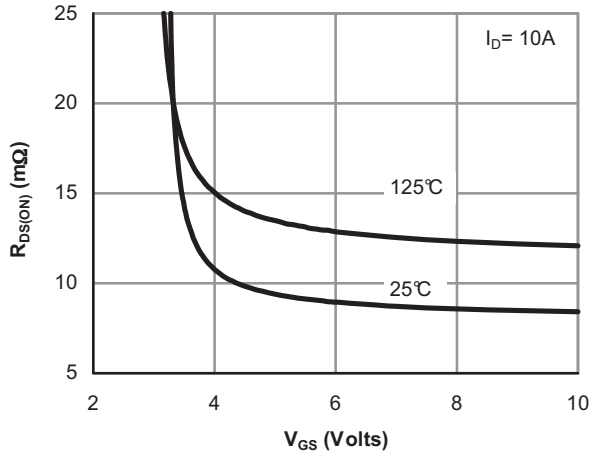

Figure 5: On-Resistance vs. Gate-Source Voltage

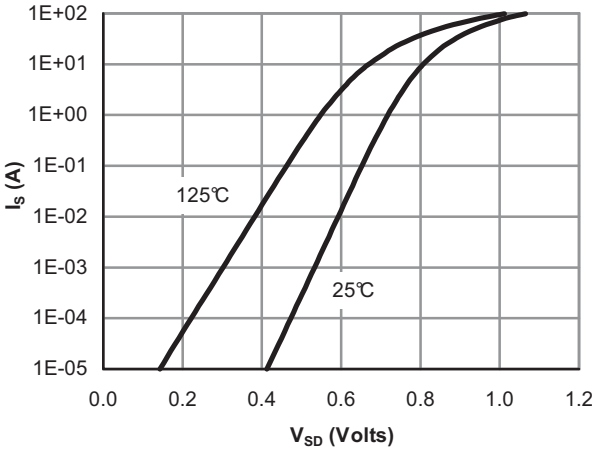

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

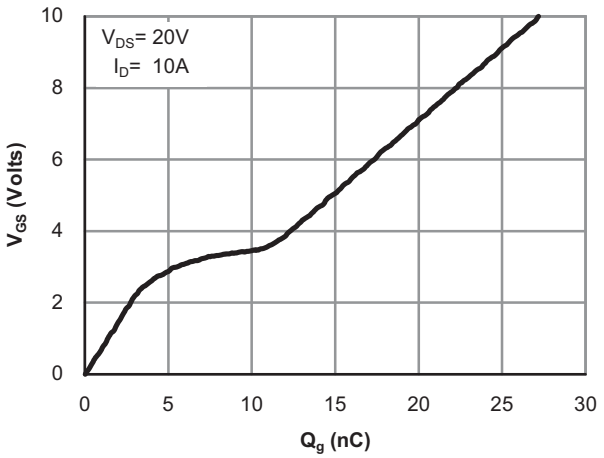

Figure 7: Gate-Charge Characteristics

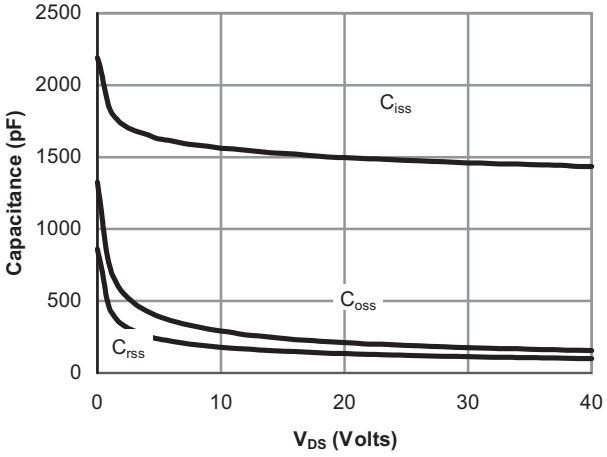

Figure 8: Capacitance Characteristics

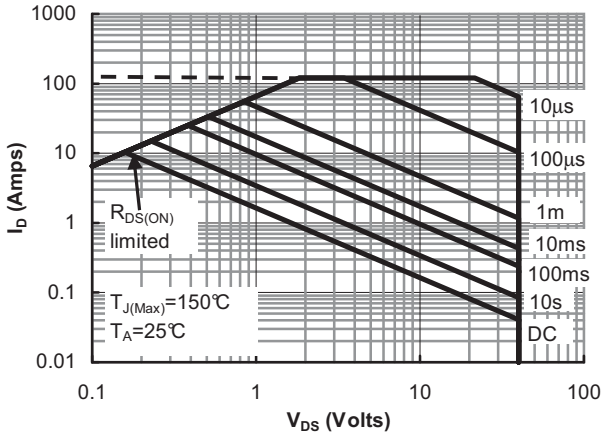

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

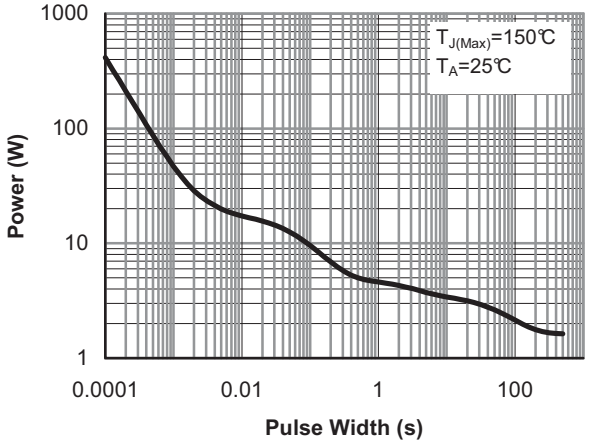

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

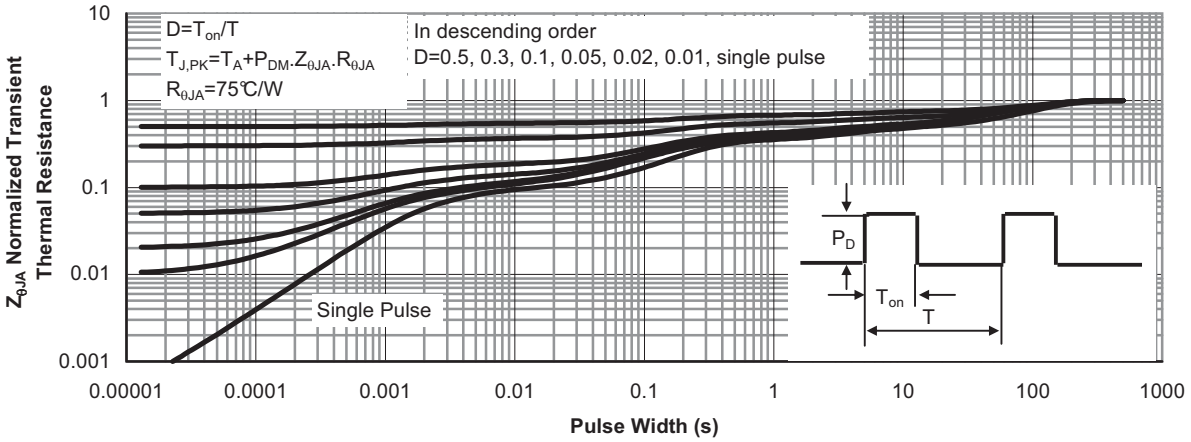

Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

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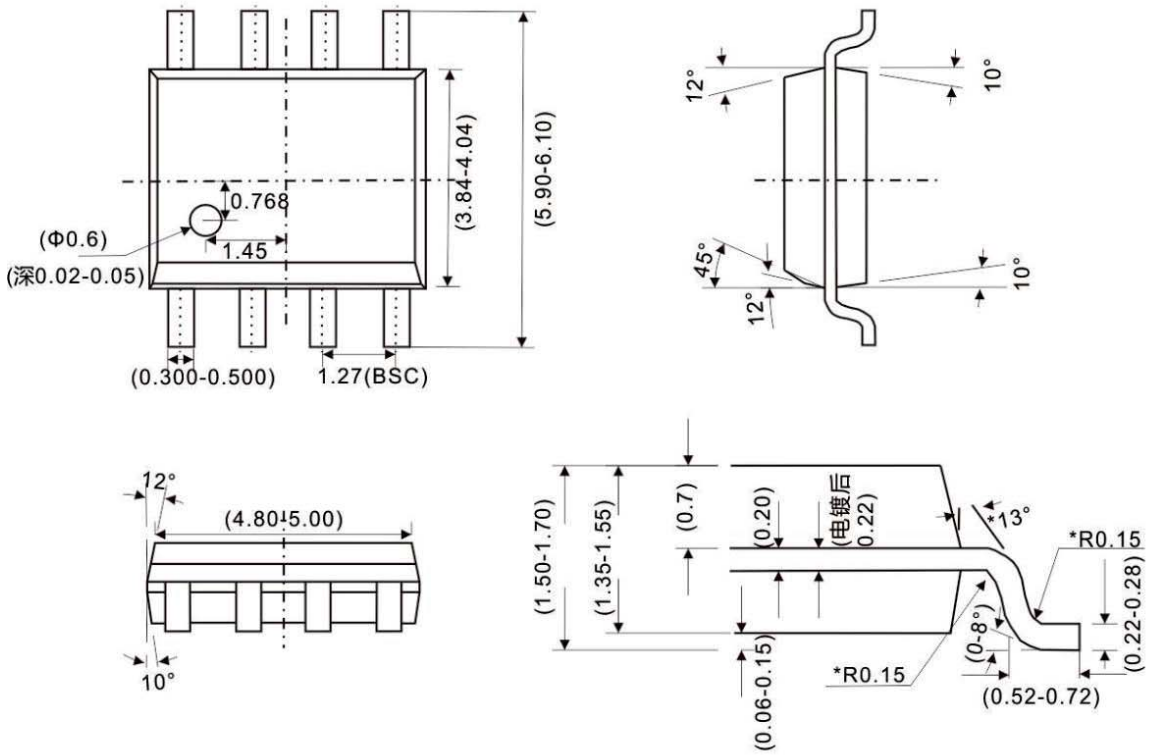

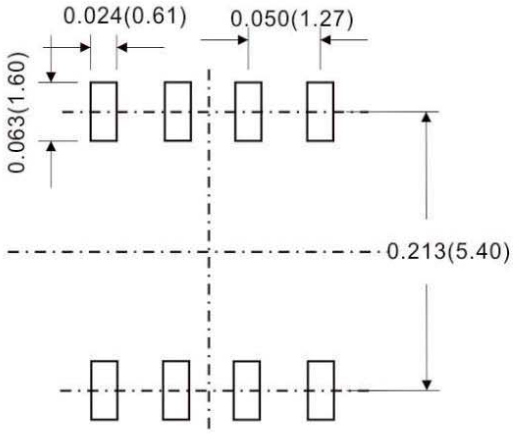

Suggested Pad Layout

Dimensions in inches and (millimeters)