# 20N50P

## 20A 500V N-Channel Enhancement Mode Power MOSFET

## Genaral Description

These Slicon N-channel enhanced vdmosfets, is obtained by the self-aligned planar used technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. Which accords with the RoHS standard.

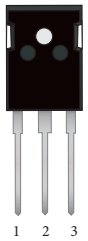
| Product Summary | | | |
|---|---|---|---|
| $V_{DS}$ | $R_{DS(on)}$ (Ω) Typ | $I_D$ (A) | Qg (Typ) |
| 500V | 0. 24@ 10V | 20 | 52nc |

## Features

- Fast switching
- Low on-resistance
- Low gate charge
- 100% avalanche tested

TO-247

20N50P




## Mechanical Data

- Case:TO-247 Package

## Application

- Switching applications

## Ordering Information

| Part No. | Package Type | Package | Quality(box) |
|---|---|---|---|
| 20N50P | TO-247 | Tube | 360 |

## Block Diagram

Pin Definition:

1. Gate
2. Drain
3. Source

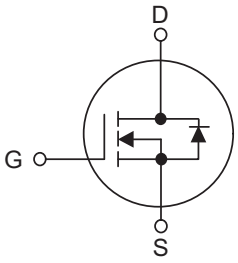



Table1 Absolute Maximum Ratings ($T_C$=25 ℃ , unless otherwise specified)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 20 | A |
| | $T_C$=100°C | | 12.5 | |
| Pulsed Drain Current (Note 1) | | $I_{DM}$ | 80 | A |
| Single Pulse Avalanche Energy(Note 2) | | $E_{AS}$ | 1300 | mJ |
| Peak Diode Recovery dv/dt | | dv/dt | 5 | V/ns |
| Power Dissipation $T_C$=25°C | | $P_D$ | 277 | W |
| Operating Junction and Storage Temperature | | $T_J$/$T_{STG}$ | -55 ~ +150 | ℃ |
| Maximum Temperature for soldering | | $T_L$ | 300 | ℃ |

Table 2.Thermal Characteristics

| Parameter | Symbol | TO-247 | Unit |
|---|---|---|---|
| Thermal resistance Junction to Ambient | $R_{\theta JA}$ | 62.5 | C/W |
| Thermal resistance Junction to Case | $R_{\theta JC}$ | 0. 45 | C/W |

Table 3. Electrical Characteristics ($T_J$=25 ℃ unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Off Characteristics | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250μA | 500 | | | V |
| Drain-Source Leakage Current | | $I_{DSS}$ | $V_{DS}$=500V,$V_{GS}$=0V | | | 1 | μA |
| Gate- Source Leakage Current | Forward | $I_{GSS}$ | $V_{GS}$=30V,$V_{DS}$=0V | | | 100 | nA |
| | Reverse | | $V_{GS}$=-30V,$V_{DS}$=0V | | | -100 | nA |
| On Characteristics(Note 4) | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 2 | | 4 | V |
| Static Drain-Source On-State Resistance | | $R_{DS(ON)}$ | $V_{GS}$=10V,$I_D$=10A | | 0.24 | 0.3 | Ω |
| Dynamic Characteristics(Note 5) | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{DS}$=25V,$V_{GS}$=0V,f=1MHz | | 2919 | | pF |
| Output Capacitance | | $C_{OSS}$ | | | 277 | | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | | | 16 | | pF |
| Switching Characteristics (Note 5) | | | | | | | |
| Turn-On Delay Time | | td(on) | $V_{DD}$=250V,$I_D$=20A, $R_G$=10Ω | | 34 | | ns |
| Turn-On Rise Time | | $t_R$ | | | 65 | | ns |
| Turn-Off Delay Time | | td(off) | | | 82 | | ns |
| Turn-Off Fall Time | | tf | | | 45 | | ns |
| Total Gate Charge | | $Q_G$ | $V_{DD}$=400V,$I_D$=20A, $V_{GS}$=10V | | 52 | | nC |
| Gate-Source Charge | | $Q_{GS}$ | | | 12.6 | | nC |
| Gate-Drain Charge | | $Q_{GD}$ | | | 18.6 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | | |
| Drain-Source Diode Forward Voltage | | $V_{SD}$ | $V_{GS}$=0V, $I_S$=20A | | | 1.5 | V |
| Maximum Continuous Drain-Source Diode Forward Current | | $I_S$ | | | | 20 | A |
| Reverse Recovery Time | | trr | $V_{GS}$=0V, $I_S$=20A dI$_F$/dt=100A/μs | | 535 | | ns |
| Reverse Recovery Charge | | $Q_{RR}$ | | | 75 | | nC |

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=10mH, $I_D$ =16.1A,Starting $T_J$=25°C
4 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
5 Guaranteed by design,not subject to production

## Typical Characteristics Diagrams

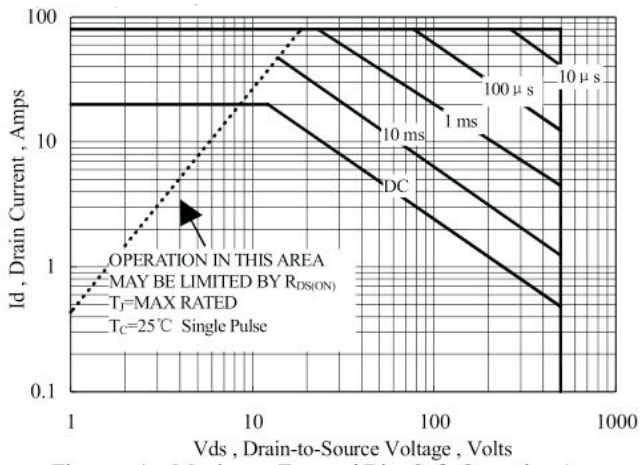



Figure 1 Maximum Forward Bias Safe Operating Area

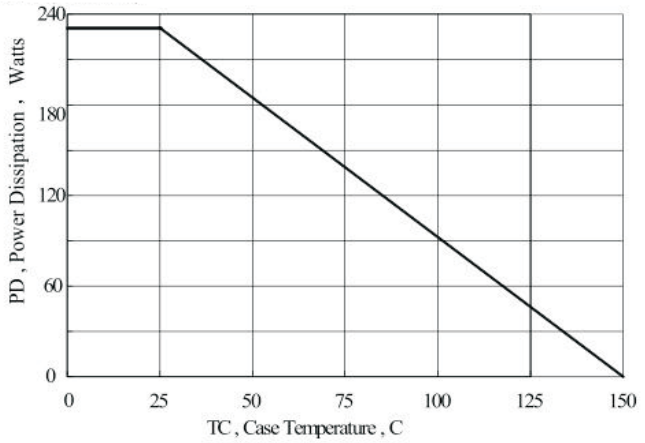



Figure 2 Maximum Power Dissipation vs Case Temperature

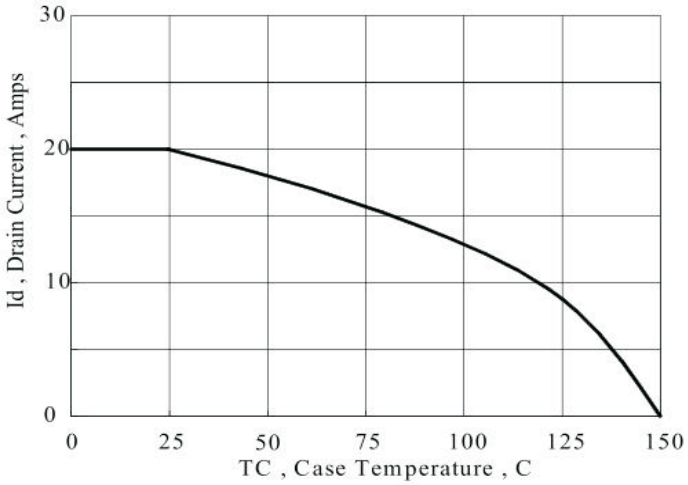



Figure 3 Maximum Continuous Drain Current vs Case Tempera

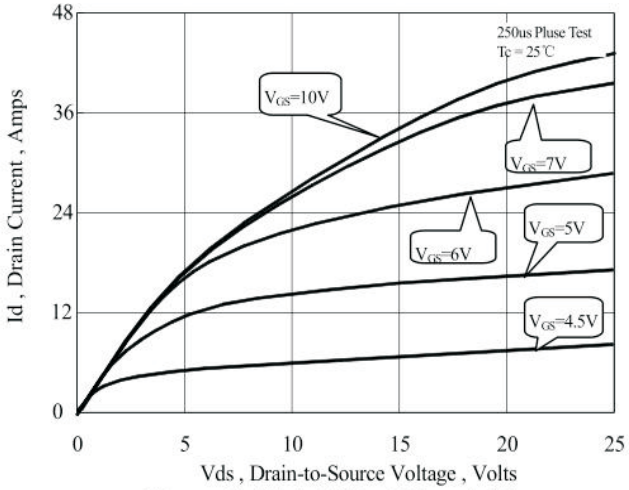



Figure 4 Typical Output Characteristics

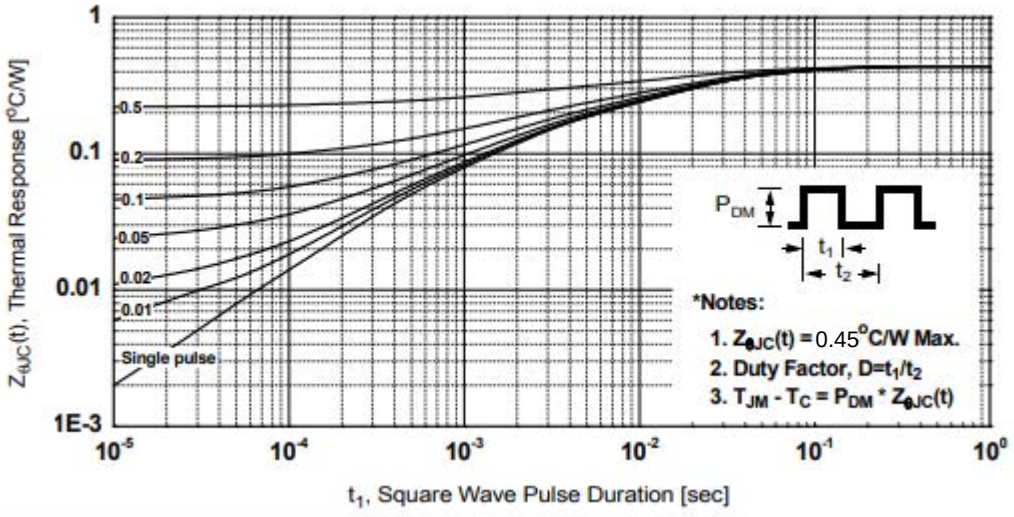



Figure 5 Maximum Effective Thermal Impedance , Junction to Case

## Typical Characteristics Diagrams

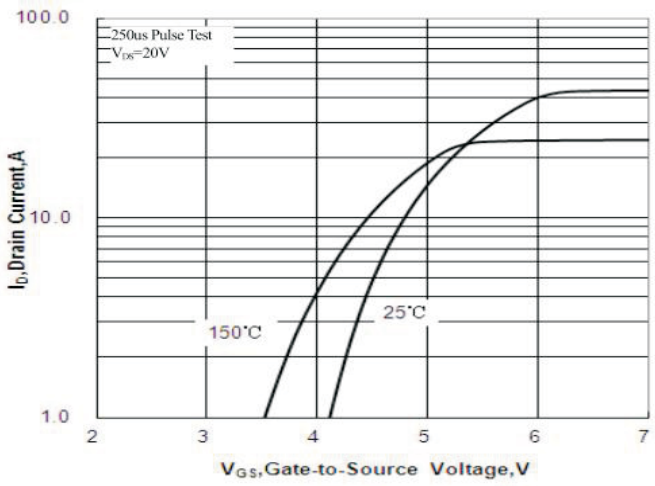



Figure 6 Typical Transfer Characteristics

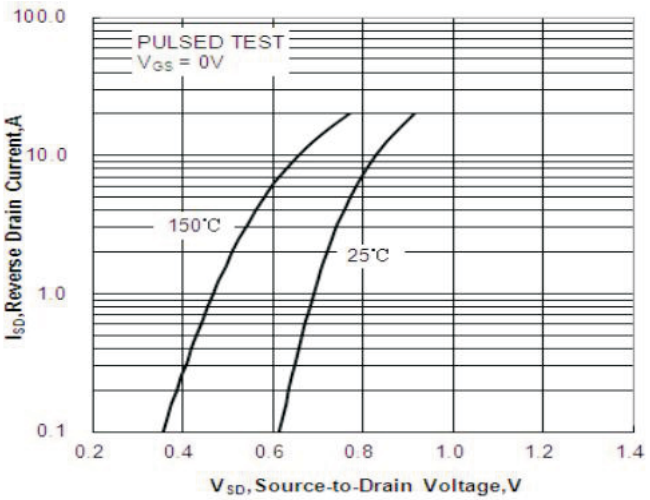



Figure 7 Typical Body Diode Transfer Characteristics

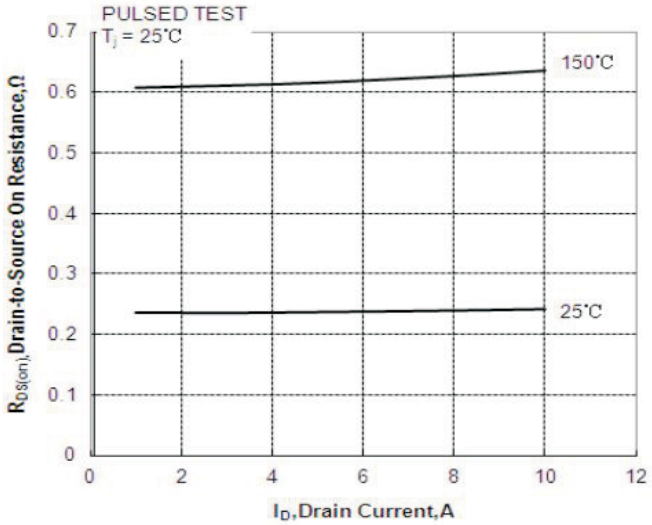



Figure 8 Typical Drain to Source ON Resistance vs Drain Current

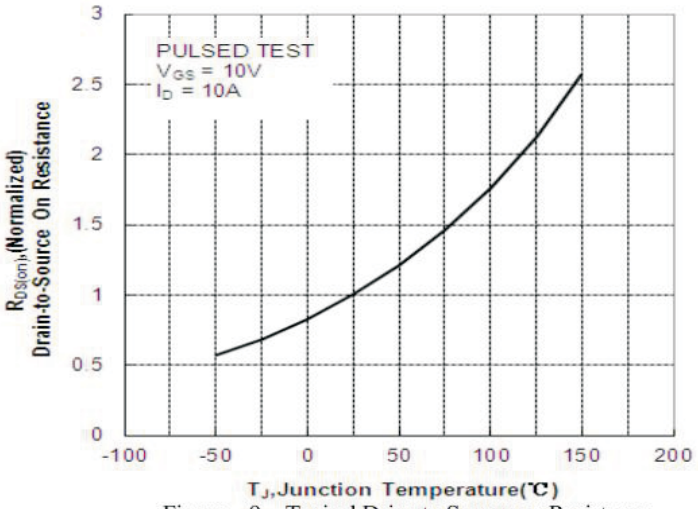



Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

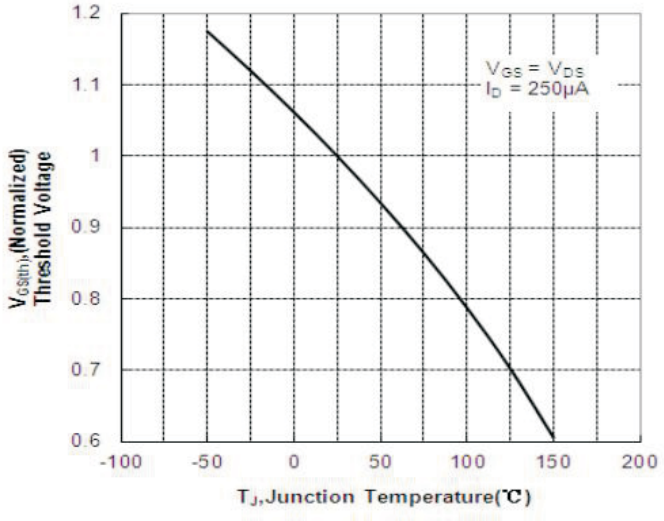



Figure 10 Typical Theshold Voltage vs Junction Temperature

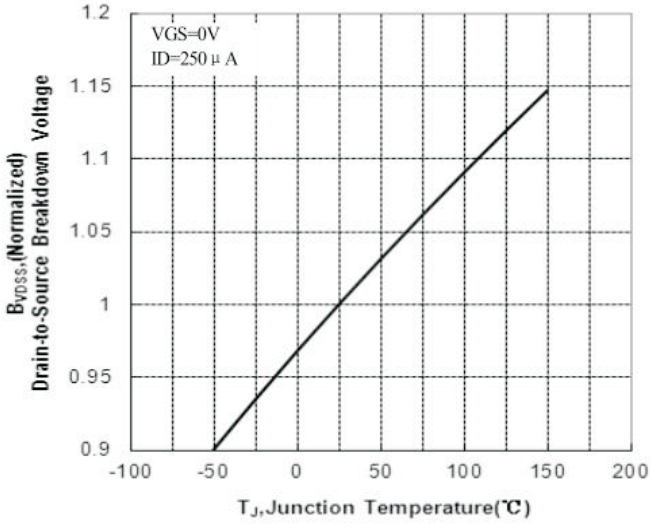



Figure 11 Typical Breakdown Voltage vs Junction Temperature

## Typical Characteristics Diagrams

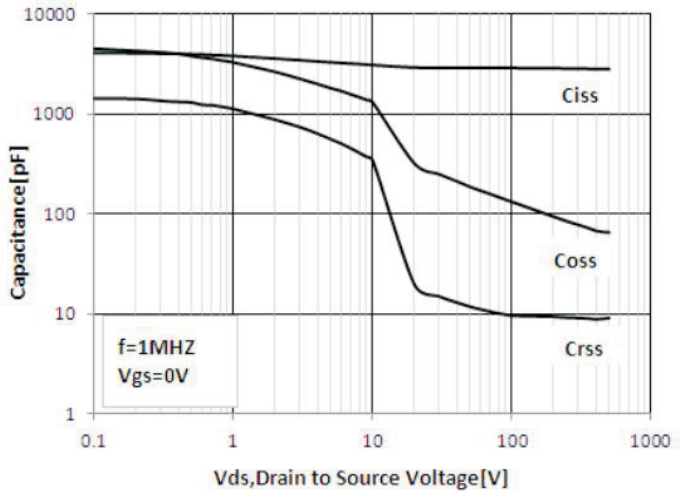



Figure 12 Typical Capacitance vs Drain to Source Voltage

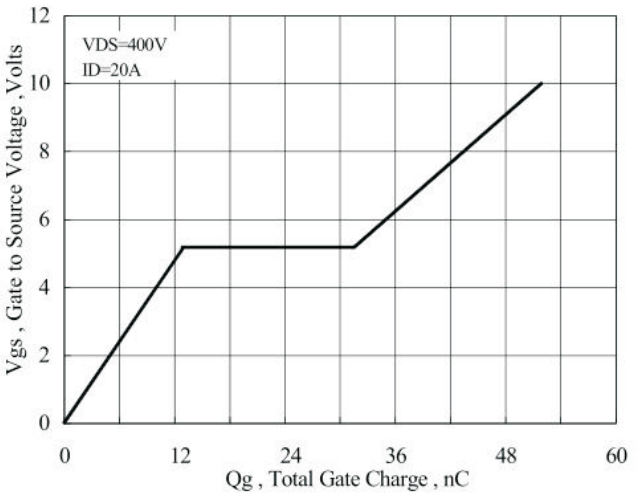
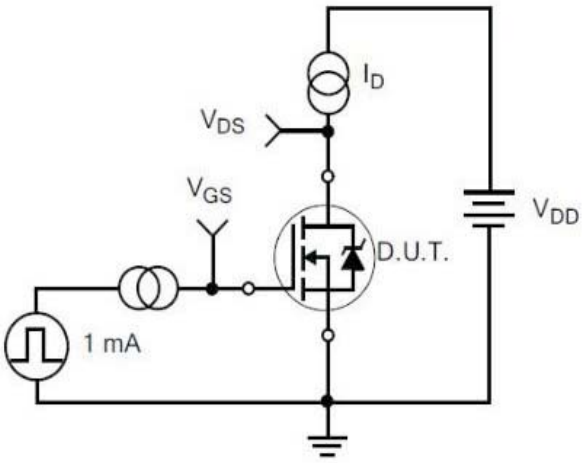
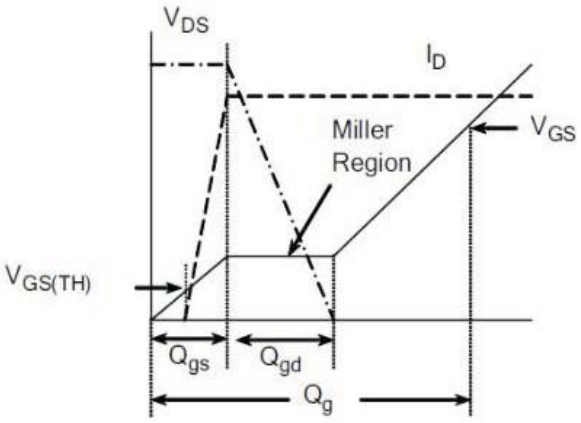



Figure 13 Typical Gate Charge vs Gate to Source Voltage

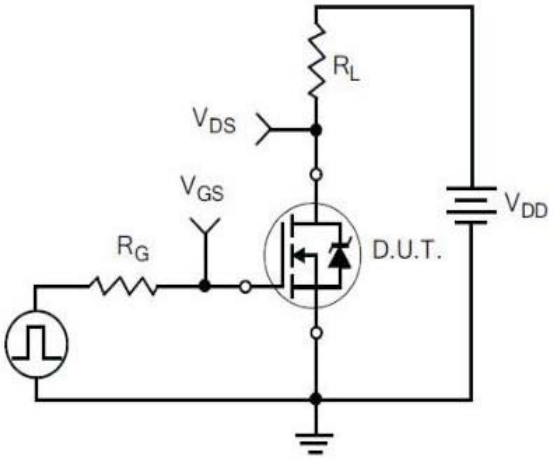
## Typical Test Circuit



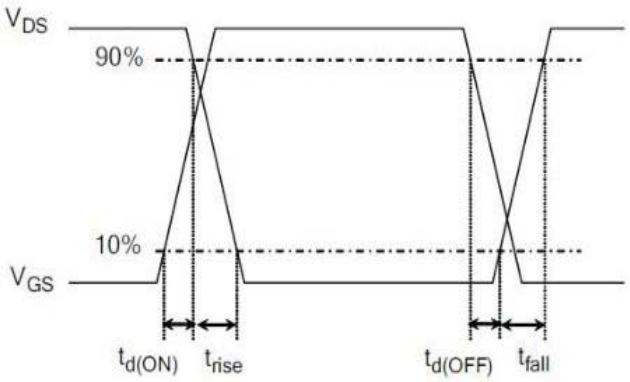

1) Gate Charge Test Circuit




2) . Gate Charge Waveform

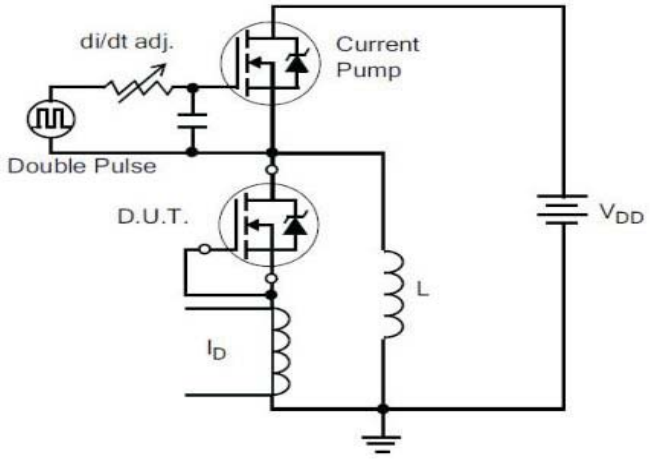



3) Resistive Switching Test Circuit

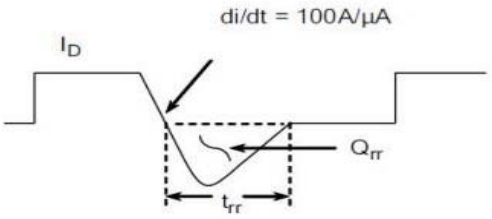



4) Resistive Switching Waveforms

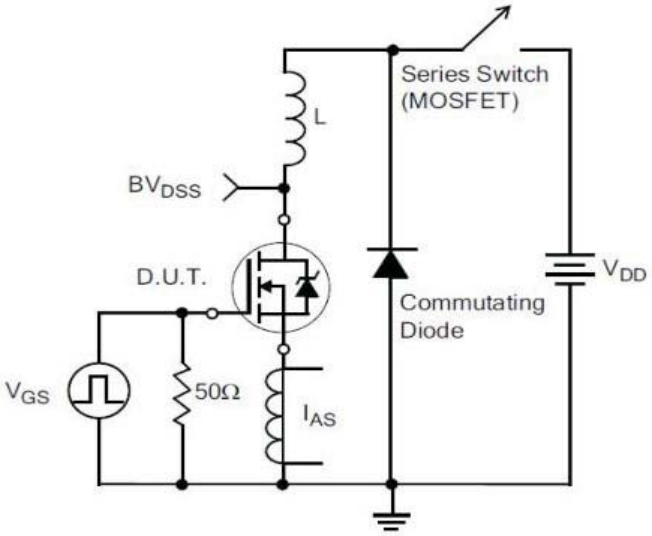
## Typical Test Circuit



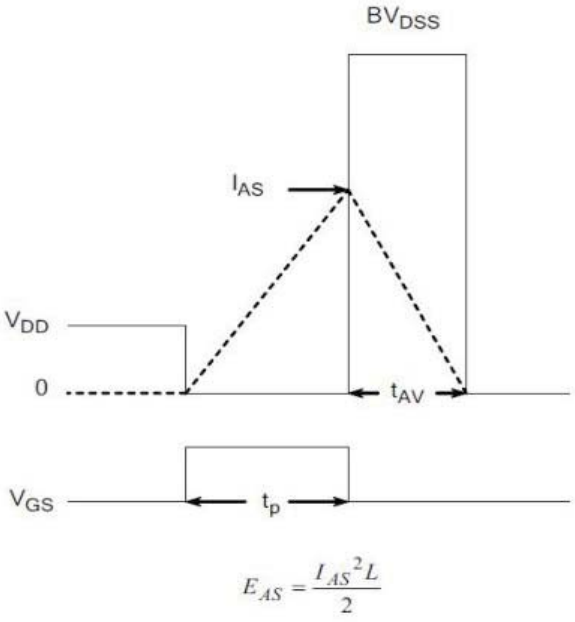

5) Diode Reverse Recovery Test Circuit




6) Diode Reverse Recovery Waveform

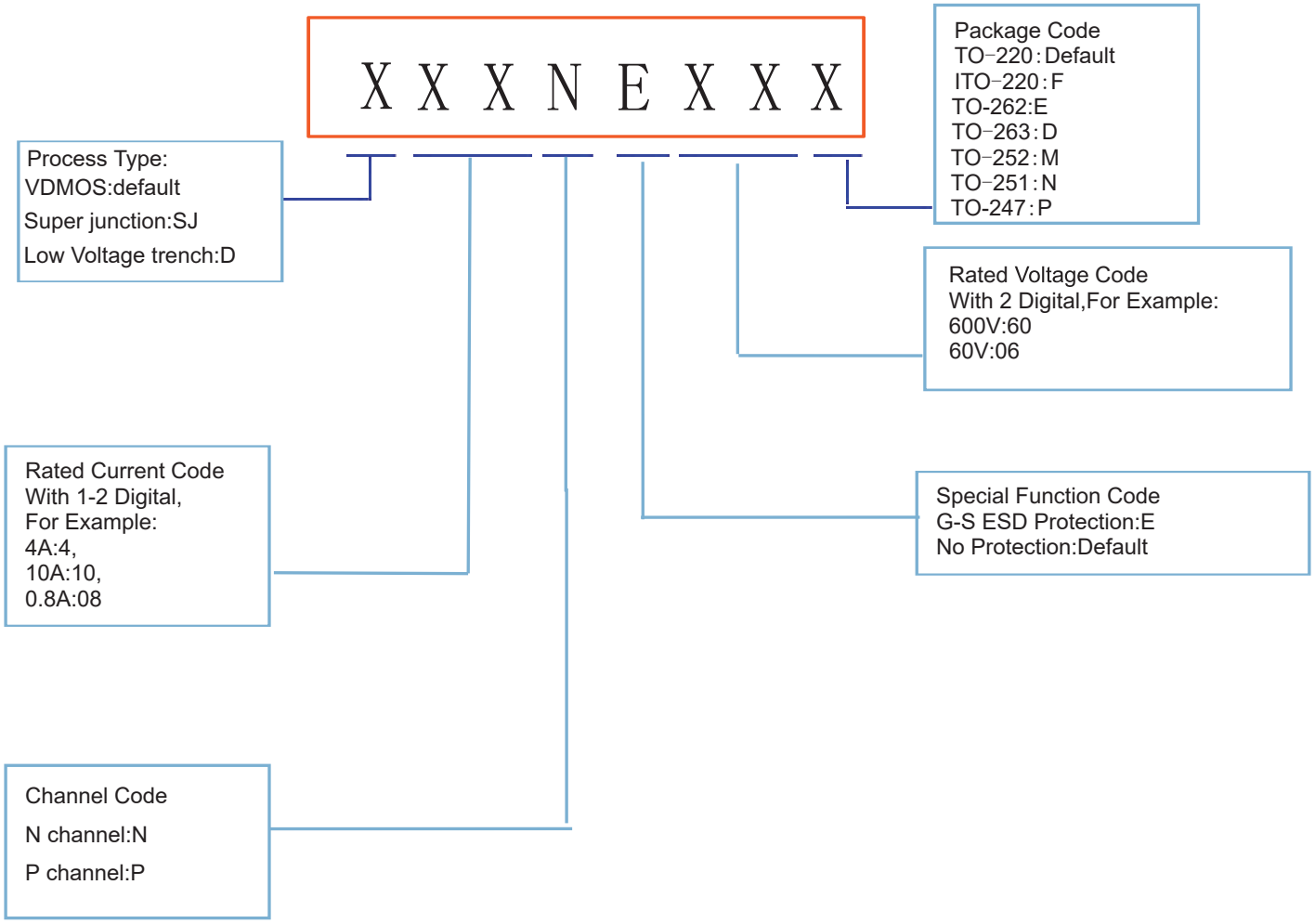



7) . Unclamped Inductive Switching Test Circuit



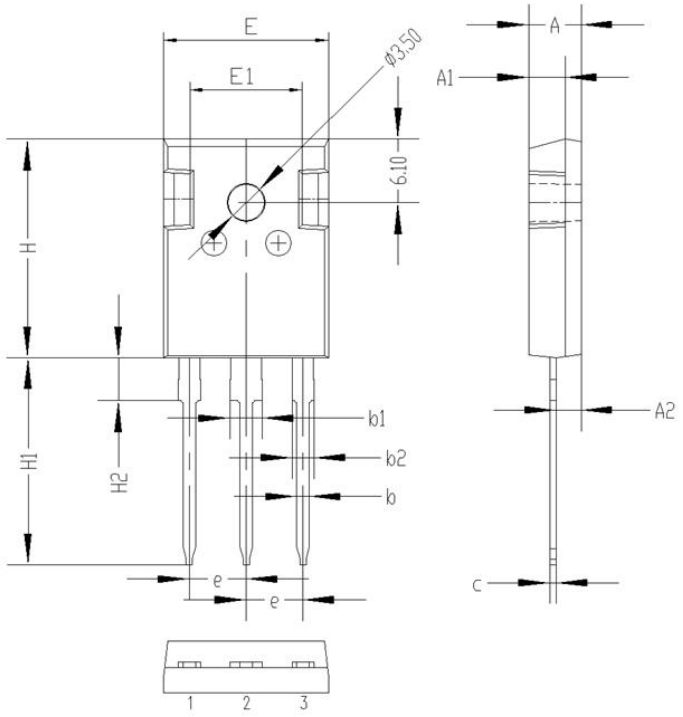

8) Unclamped Inductive Switching Waveforms

## Product Names Rules



Dimensions

## TO-247 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions(millimeters) | |
|---|---|---|
| | Min. | Max. |
| A | 4.80 | 5.20 |
| A1 | 3.30 | 3.70 |
| A2 | 2.10 | 2.50 |
| b | 1.00 | 1.40 |
| b1 | 2.90 | 3.30 |
| b2 | 1.90 | 2.30 |
| c | 0.40 | 0.80 |
| e | 5.25 | 5.65 |
| E | 15.6 | 16.0 |
| E1 | 10.6 | 11.00 |
| H | 20.8 | 21.2 |
| H1 | 19.4 | 20.4 |
| H2 | 3.90 | 4.30 |
| G | 5.90 | 6.30 |
| ΦP | 3.30 | 3.70 |

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