SEMICONDUCTOR

20N80P

20A 800V Silicon N-Channel Power MOSFET

Genaral Description

20N80P the silicon N-channel Enhanced VDMOSFETS, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

Product Summary			
V_{DS}	$R_{DS(on)}$ (Ω) Typ	I_D (A)	Qg (Typ)
800V	0.5 @ 10V 8.5A	20	74nc

Features

- Low on-resistance
- Low reverse transfer capacitance
- 100% avalanche tested

TO-247
20N80P

Mechanical Data

- Case:TO-247 Package

Application

- Power switch circuit of adaptor and charger

Ordering Information

Part No.	Package Type	Package	Quality(box)
20N80P	TO-247	Tube	360

Pin Definition:

1. Gate
2. Drain
3. Source

Block Diagram

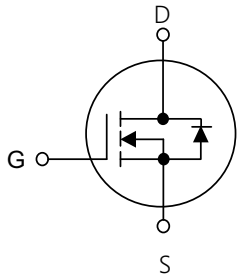


Table1 Absolute Maximum Ratings (T_C=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	800	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	20	A
	T_C=100°C		15	
Pulsed Drain Current (Note 1)		I_{DM}	80	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	2500	mJ
Power Dissipation T_C=25°C		P_D	400	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55~+150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	20N80P	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	55	°C/W
Thermal resistance Junction to Case	$R_{\theta JC}$	0.32	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	800	-	-	V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=800V,V_{GS}=0V	-	-	10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	1	μA
	Reverse		V_{GS}=-30V,V_{DS}=0V	-	-	-1	μA
On Characteristics(Note 3)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.5	-	4.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=8.5A	-	0.5	0.65	Ω
Dynamic Characteristics(Note 4)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz	-	4150	-	pF
Output Capacitance		C_{OSS}		-	310	-	pF
Reverse Transfer Capacitance		C_{RSS}		-	55	-	pF
Switching Characteristics (Note 4)							
Turn-On Delay Time		td(on)	V_{DD}=400V,I_D=10A R_G=9.1Ω,	-	60	-	ns
Turn-On Rise Time		t_R		-	105	-	ns
Turn-Off Delay Time		td(off)		-	39	-	ns
Turn-Off Fall Time		tf		-	80	-	ns
Total Gate Charge		Q_G	V_{DS}=400V,I_D=10A, V_{GS}=10V	-	74	-	nC
Gate-Source Charge		Q_{GS}		-	20	-	nC
Gate-Drain Charge		Q_{GD}		-	33	-	nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=20A	-	-	1.5	V
Maximum Continuous Drain-Source Diode Forward Current		I_S		-	-	20	A
Reverse Recovery Time		trr	V_{GS}=0V, I_F=20A dI$_F$/dt=100A/μs (Note 1)	-	510	-	ns
Reverse Recovery Charge		Q_{RR}		-	2.1	-	μC

Notes : 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 I_D=23A,L=10mH,Starting T_J=25°C
3 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
4 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

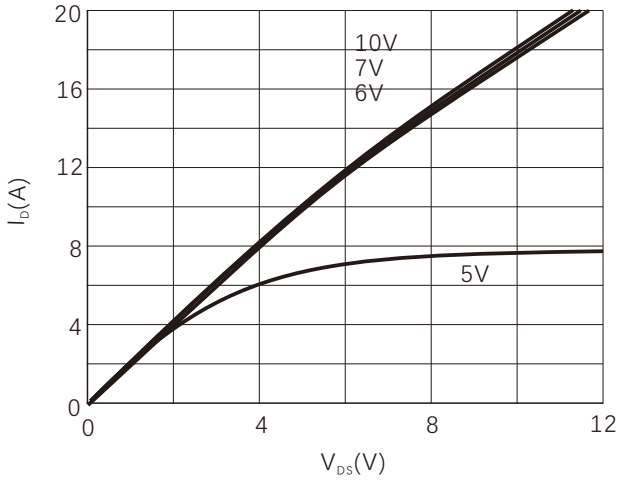


Figure2.Normalized $R_{DS(ON)}$ vs Temperature

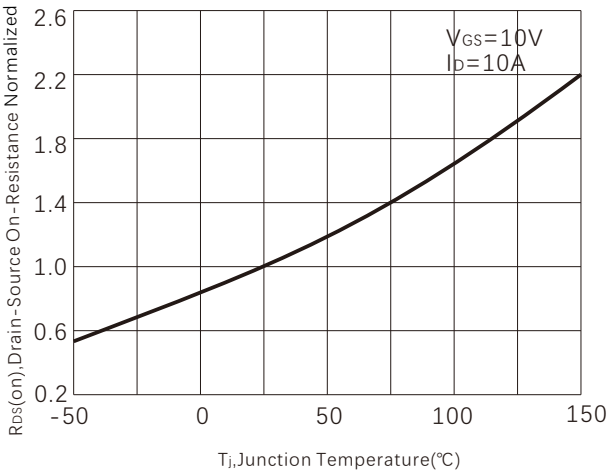


Figure 3.On-Resistance vs.Drain Current

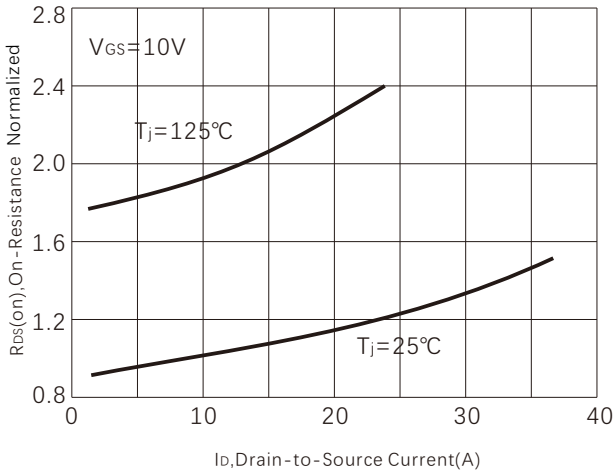


Figure 4. Capacitance

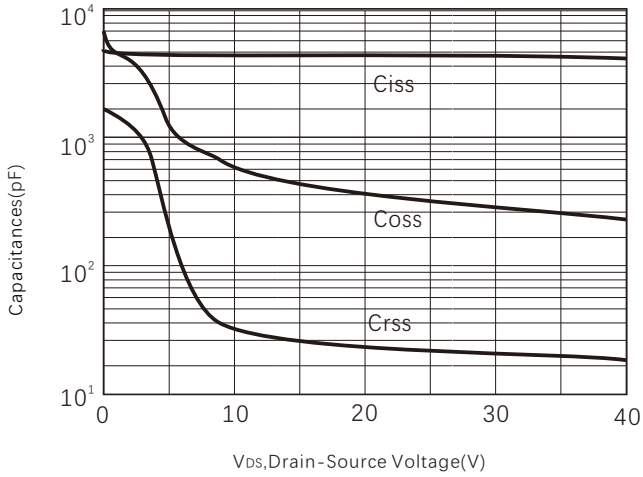


Figure 5.Gate charge

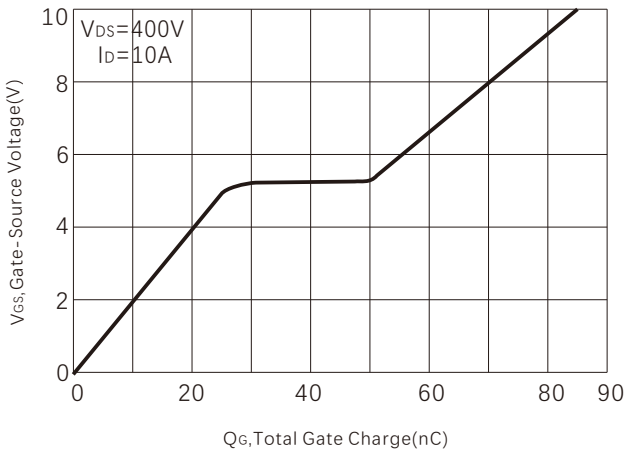


Figure 6.Source-Drain Diode Forward Voltage

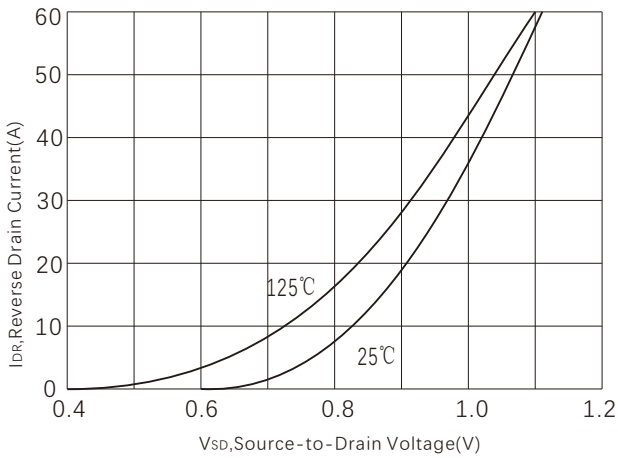


Figure 7.Input Admittance

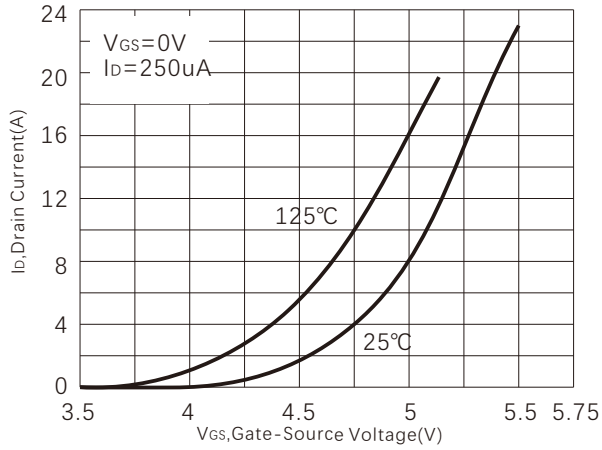


Figure 8. Power dissipation

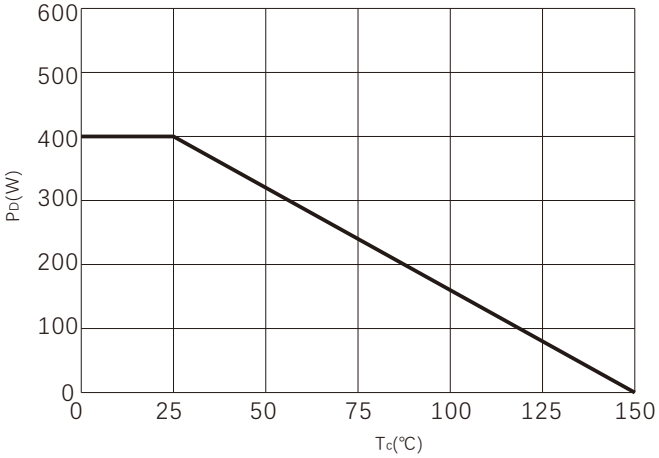


Figure 9. Safe operating area

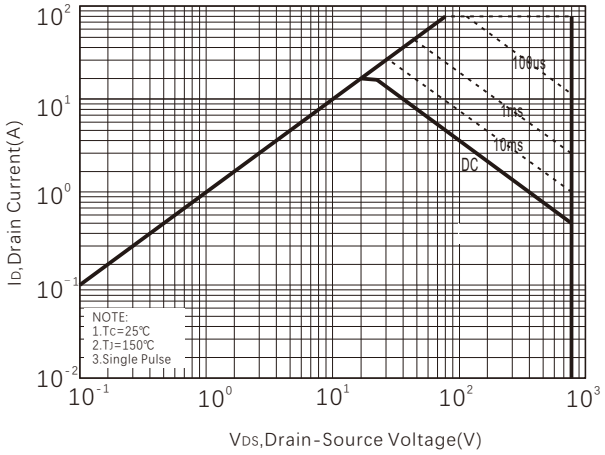


Figure 10.ID Current De-rating

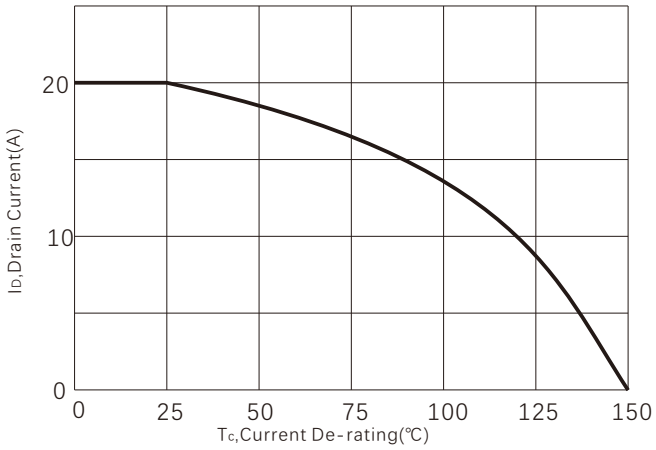
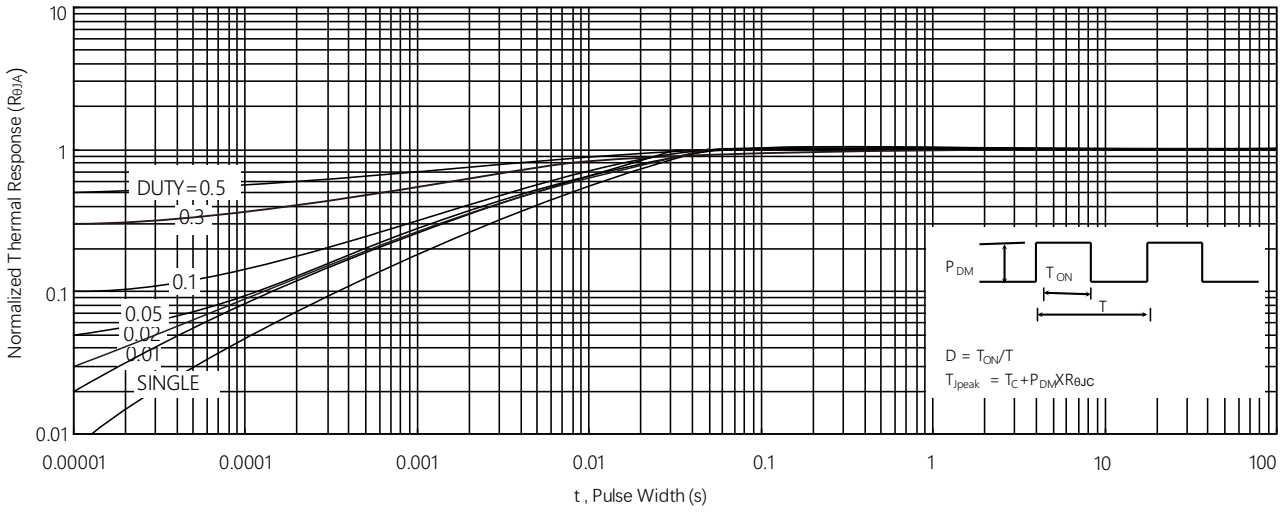
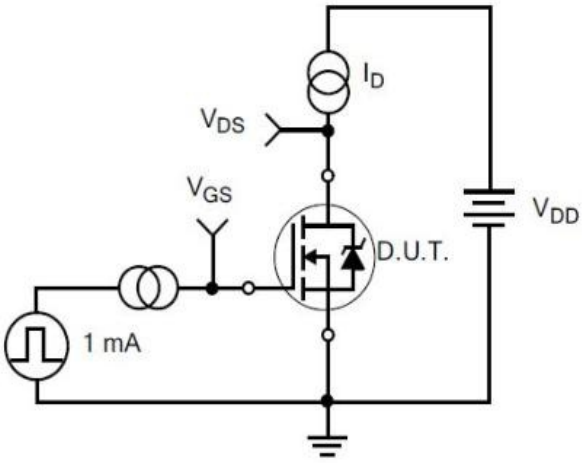


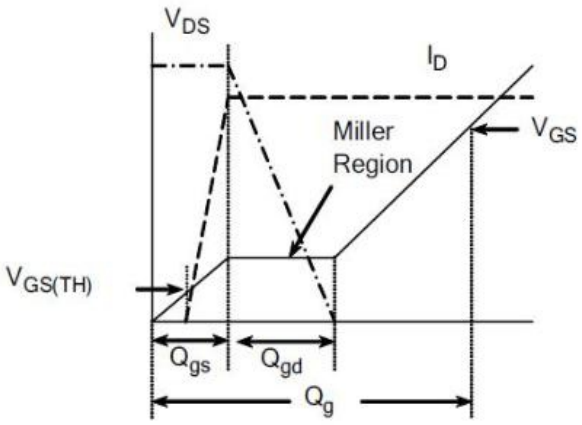
Figure 11.Normalized Maximum Transient Thermal Impedance



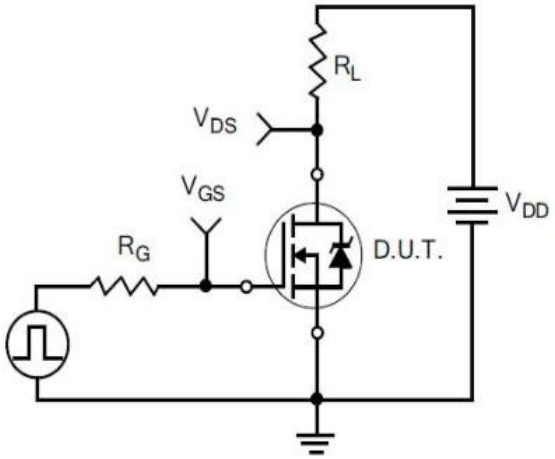
Typical Test Circuit



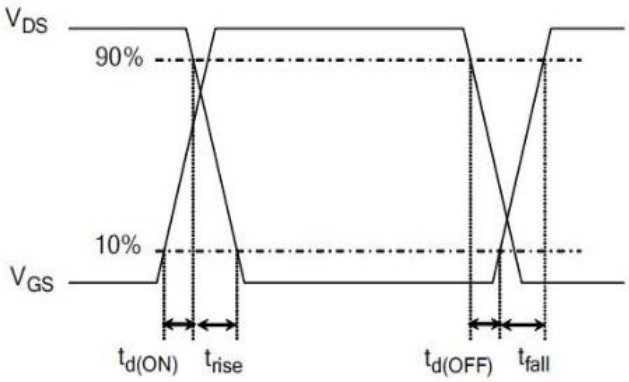
1) Gate Charge Test Circuit



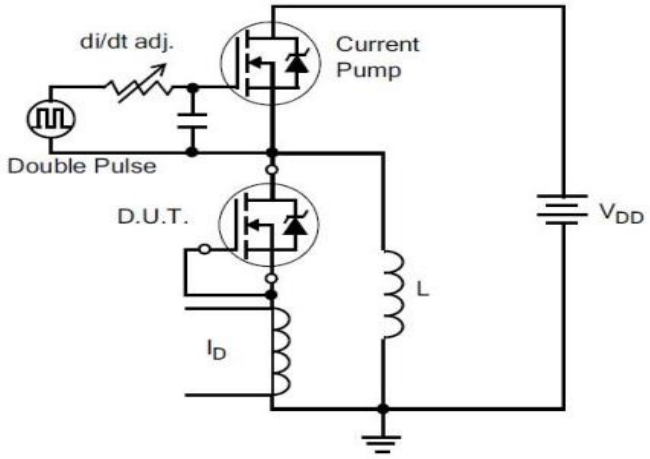
2) . Gate Charge Waveform



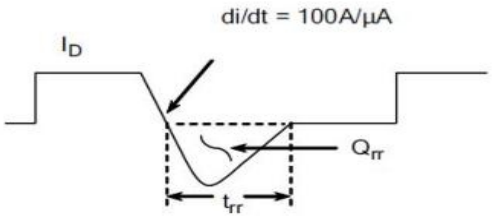
3) Resistive Switching Test Circuit



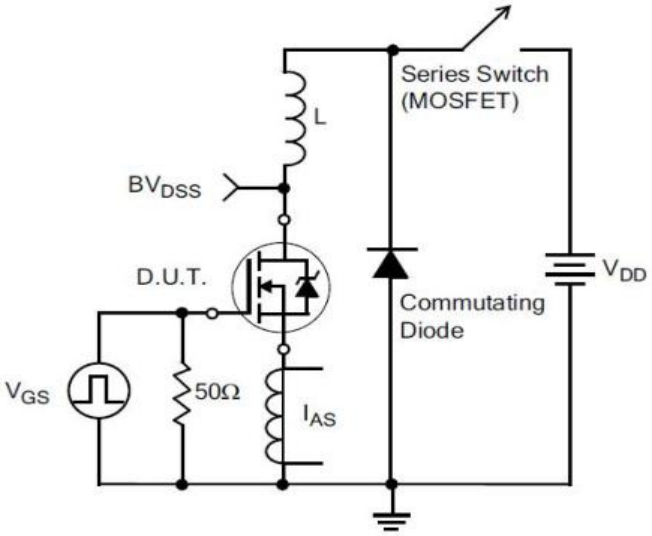
4) Resistive Switching Waveforms



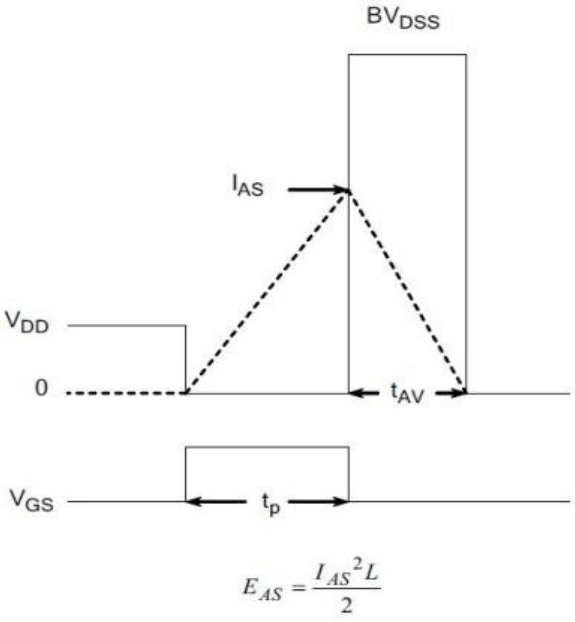
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



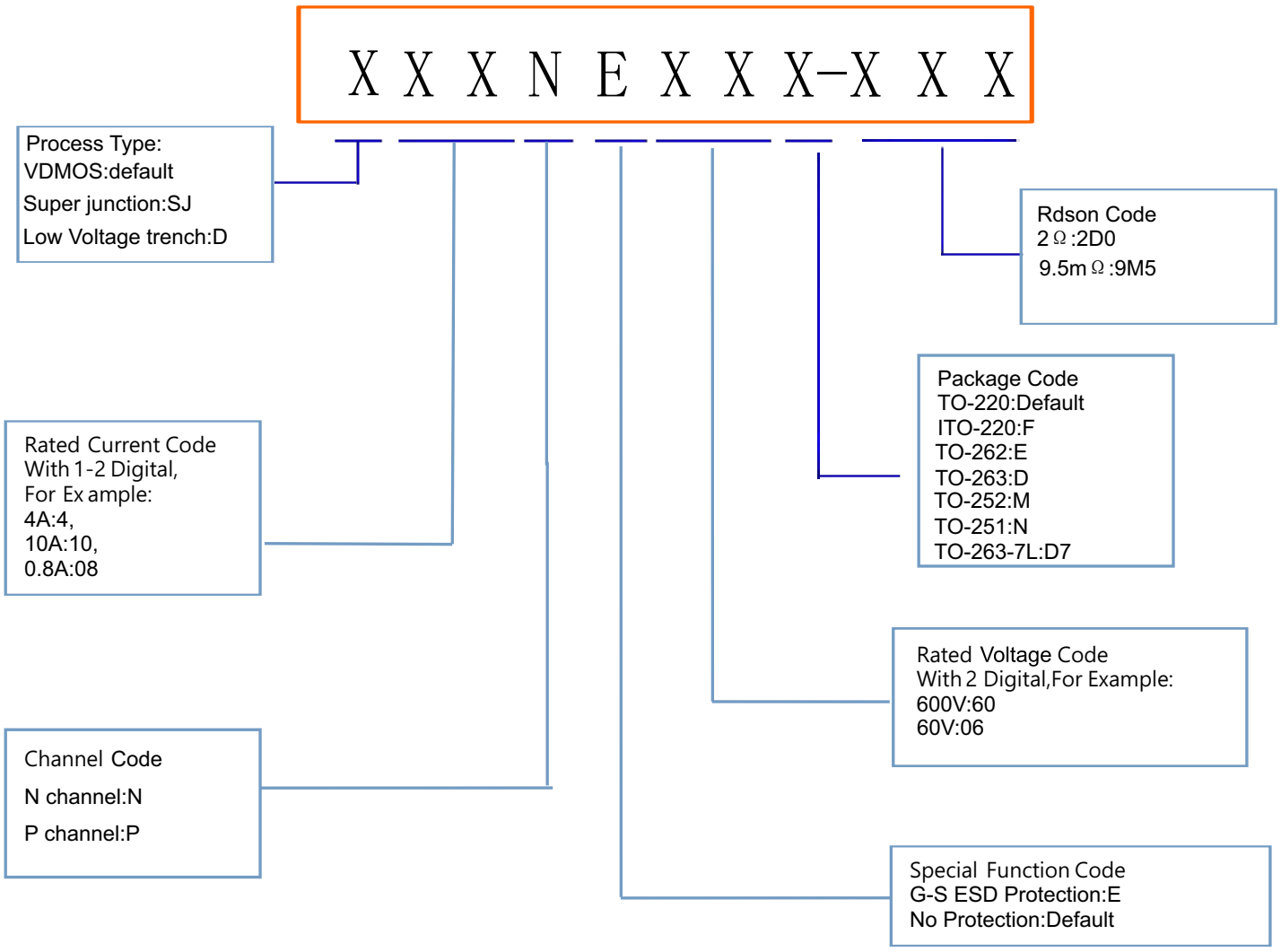
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

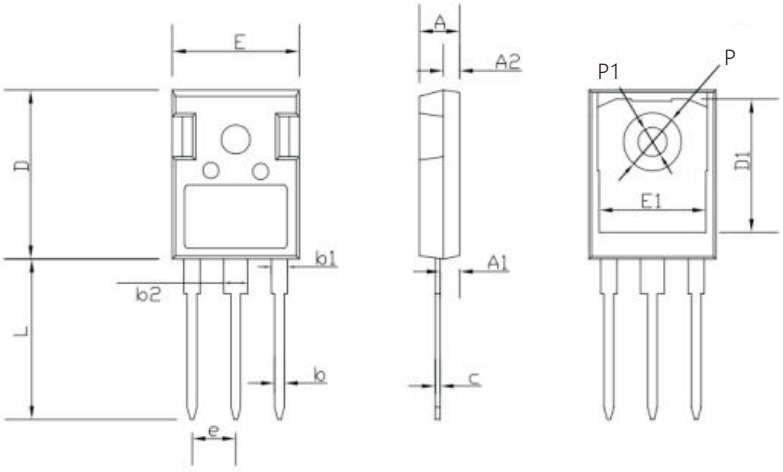
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-247 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.06	0.0772	0.0812
b2	2.96	3.06	0.117	0.121
c	0.59	0.66	0.0232	0.0260
D	20.90	21.10	0.8235	0.8313
D1	16.25	16.85	0.6403	0.6639
E	15.70	15.90	0.6186	0.6265
E1	13.10	13.50	0.5161	0.5319
e	5.44		0.2143	
L	19.80	20.10	0.7801	0.7919
ΦP	3.50	3.70	0.1379	0.1458
ΦP1	0	7.30	0	0.2876

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