SEMICONDUCTOR

5N50
500V Silicon N-Channel Power MOSFET

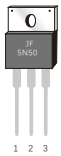
Genaral Description

5N50 the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220, which accords with the RoHS standard.

Product Summary			
V_{DS}	$R_{DS(on)}$(Ω)Typ	I_D(A)	Qg(Typ)
500V	1.35 @ 10V,2.5A	5	12.5nc

TO-220

5N50



Features

- Low on-resistance
- Low gate charge and Fast Switching
- 100% avalanche tested
- Rohs compliant

Mechanical Data

- Case:TO-220 Package

Application

- Power switch circuit of adaptor and charger

Block Diagram

Pin Definition:

1.Gate
2.Drain
3.Source

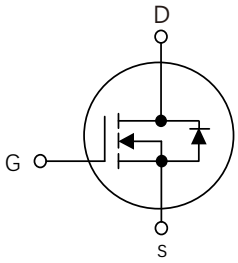


Table1 Absolute Maximum Ratings (TC=25°C, unless otherwise specified)

Parameters		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±30	V
Contionous Drain Current	TC=25°C	I_D	5	A
	TC=100°C		3.1	
Pulsed Drain Current (Note 1)		I_{DM}	20	A
Single Pulse Avalanche Energy(Note 2)		EAS	210	mJ
Reverse Diode Recovery dv/dt(Note 3)		dv/dt	5.0	V/ns
Power Dissipation TC=25°C		P_D	65	W
Operating Junction and Storage Temperature		TJ/TSTG	-55 ~ +150	℃

Table 2.Thermal Characteristics

Parameters	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	96. 5	℃/W
Thermal resistance Junction to Case	$R_{\theta JC}$	1.67	℃/W

Table 3. Electrical Chatacteristics (T_J=25℃, unless otherwise specified)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V,V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			10	μA
	Reverse		V_{GS}=-30V,V_{DS}=0V			-10	μA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	2.0	3.0	4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=2.5A		1.35	1.45	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1MHz		520		pF
Output Capacitance		C_{OSS}			40		pF
Reverse Transfer Capacitance		C_{RSS}			2.3		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=250V,I_D=5A, V_{GS}=10V,R_G=10Ω		10		ns
Turn-On Rise Time		tr			9		ns
Turn-Off Delay Time		td(off)			28		ns
Turn-Off Fall Time		tf			13		ns
Total Gate Charge		Q_G	V_{DS}=250V,I_D=5A, V_{GS}=10V		12.5		nC
Gate-Source Charge		Q_{GS}			2.7		nC
Gate-Drain Charge		Q_{GD}			6		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V,I_S=5A			1.5	V
Maximum Continuous Drain-Source Diode Forward Current(Note 4)		I_S				5	A
Reverse Recovery Time		trr	V_{GS}=0V,I_S=5A dI$_F$/dt=100A/μs(Note 4)		318		ns
Reverse Recovery Charge		Q_{RR}			1520		nC

Notes: 1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=10mH,I_D=5.3A,Starting T_J=25°C
3 I_{SD}=5A,di/dt≤100A/μS,V_{DD}≤BV_{DSS},starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS,Duty cycle≤2%
5 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

Figure 1.Output Characteristics

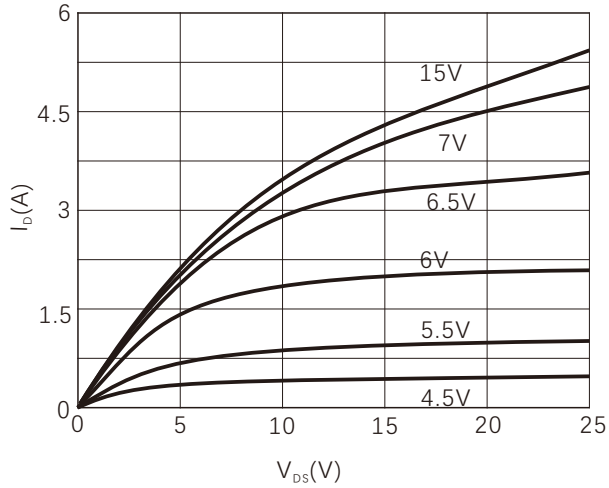


Figure 2.$R_{DS(ON)}$ vs Junction Temperature

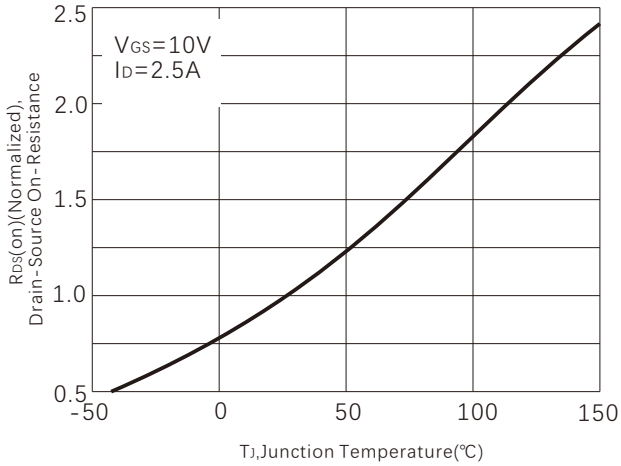


Figure 3.$R_{DS(on)}$ vs.Drain Current

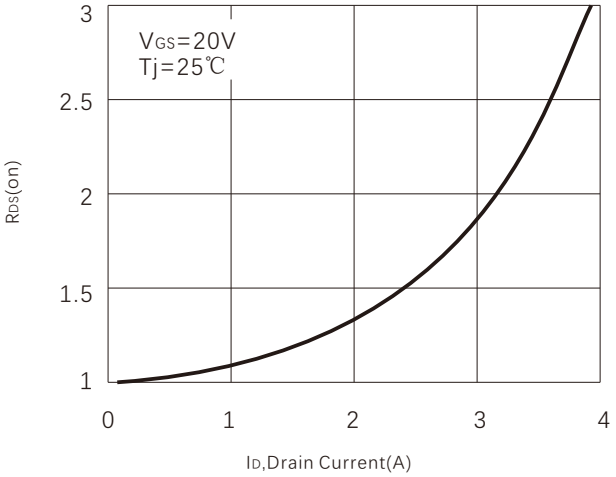


Figure 4. Capacitance

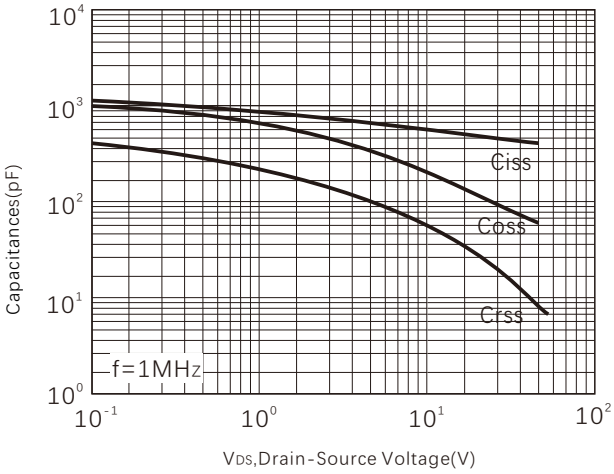


Figure 5.Gate charge

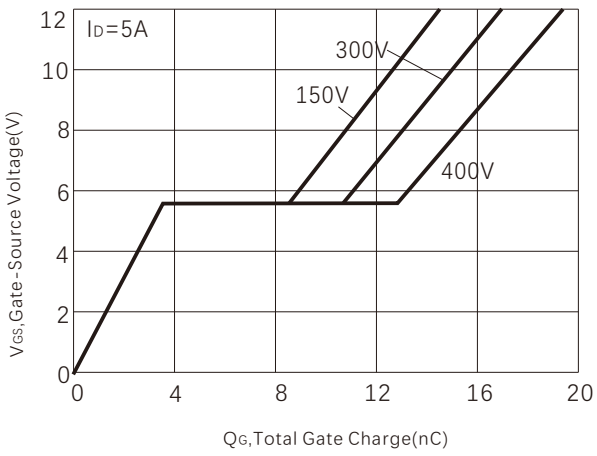


Figure 6. Typical Body Diode Transfer Characteristics

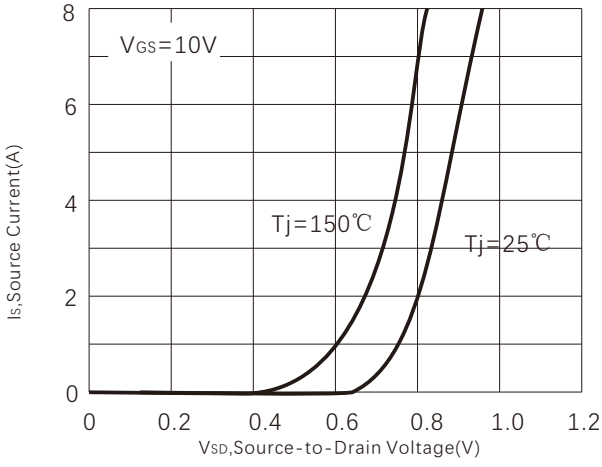


Figure7.Power dissipation

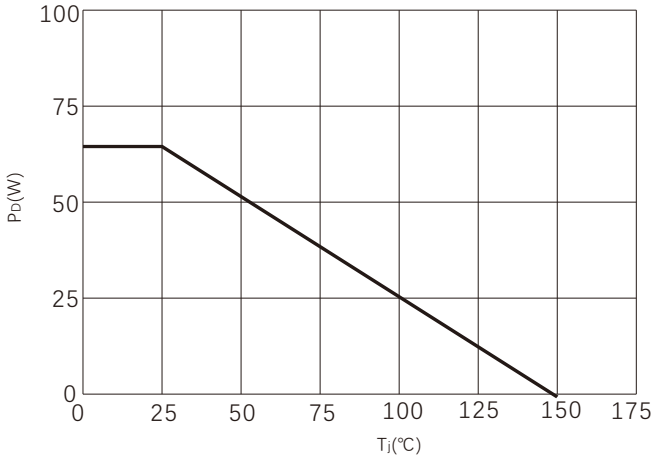


Figure 8. Safe operating area

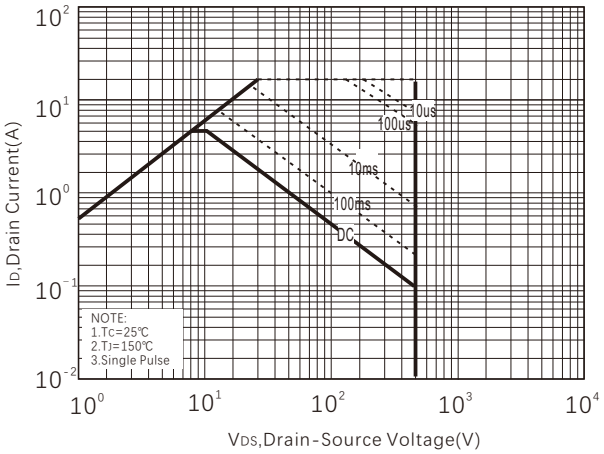


Figure 9. Drain Current

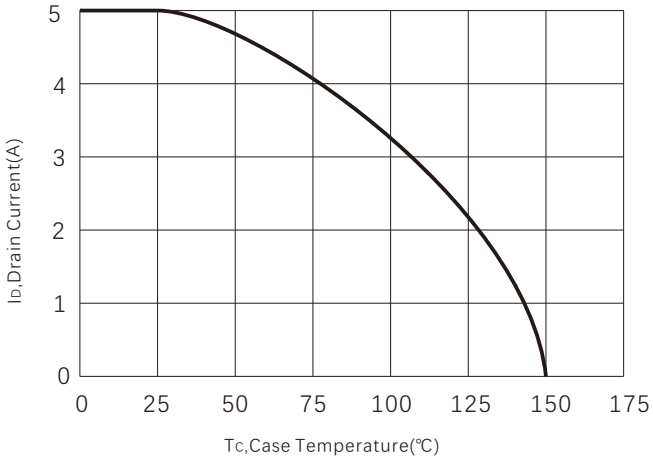
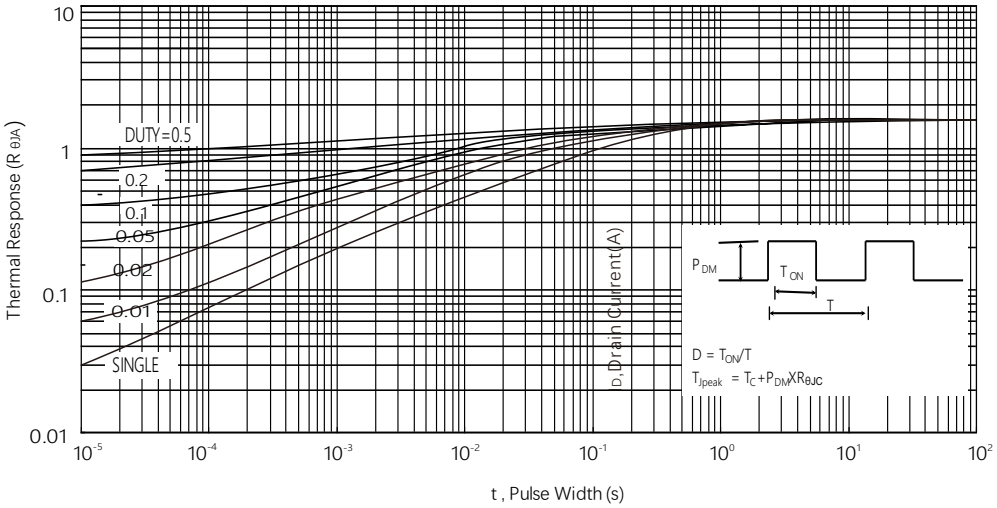
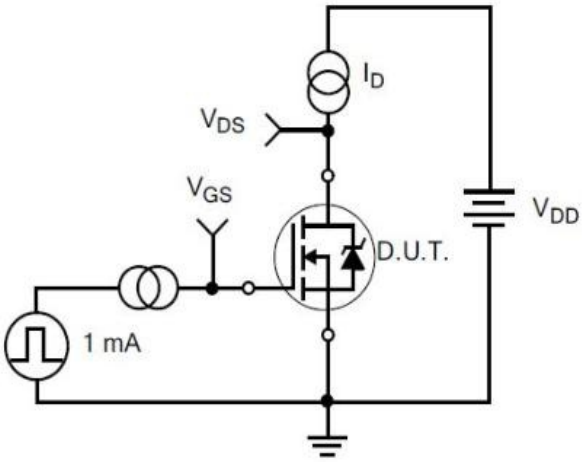


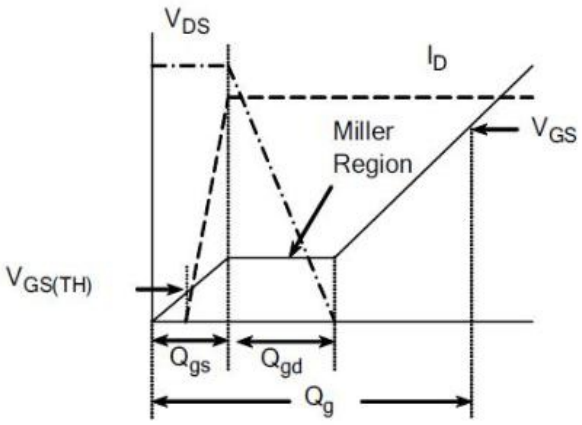
Figure 10. Maximum Transient Thermal Impedance



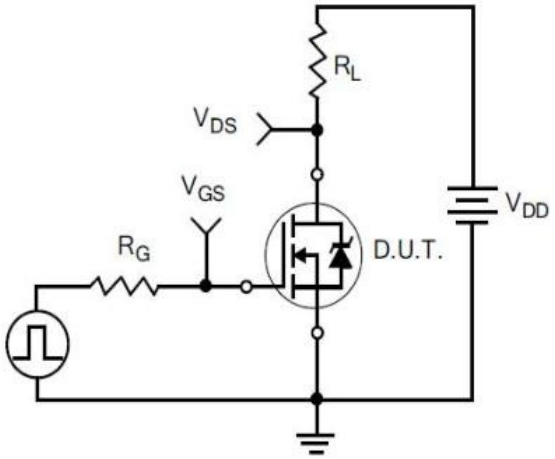
Typical Test Circuit



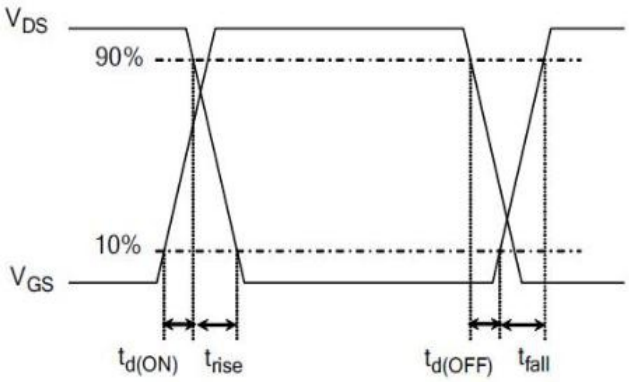
1) Gate Charge Test Circuit



2) . Gate Charge Waveform

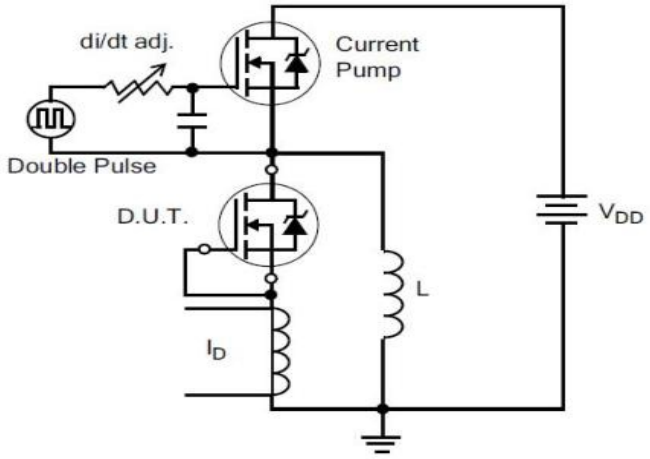


3) Resistive Switching Test Circuit

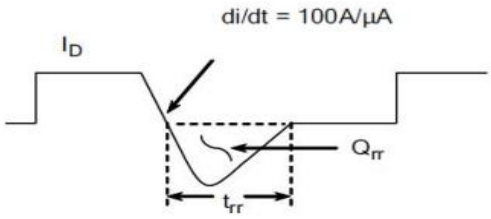


4) Resistive Switching Waveforms

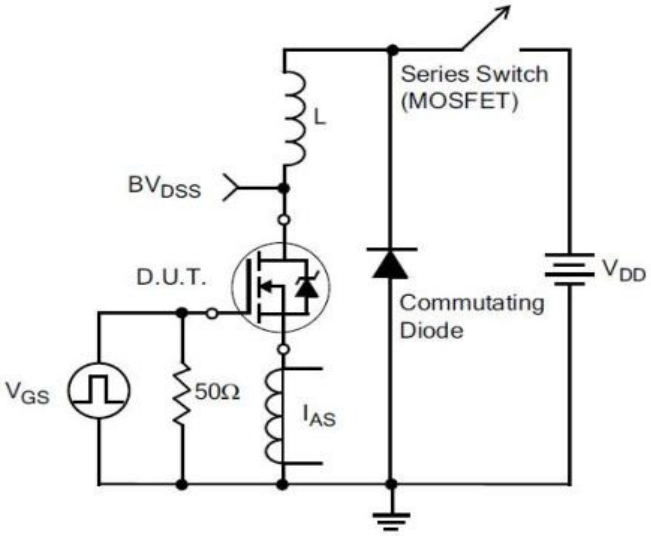
Typical Test Circuit



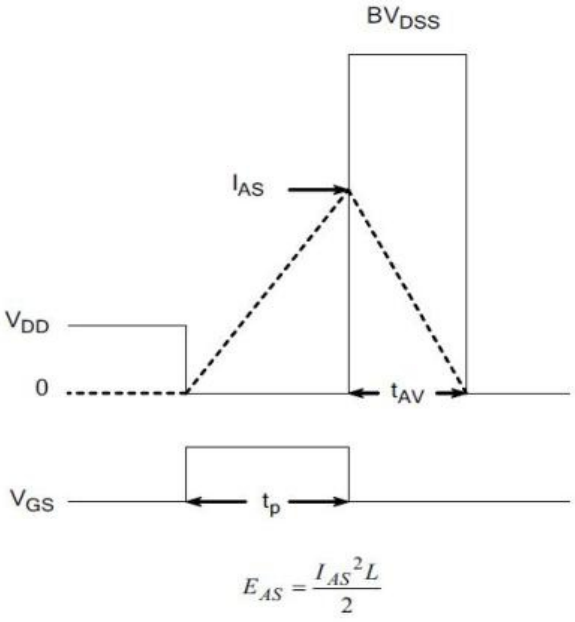
5) Diode Reverse Recovery Test Circuit



6) Diode Reverse Recovery Waveform



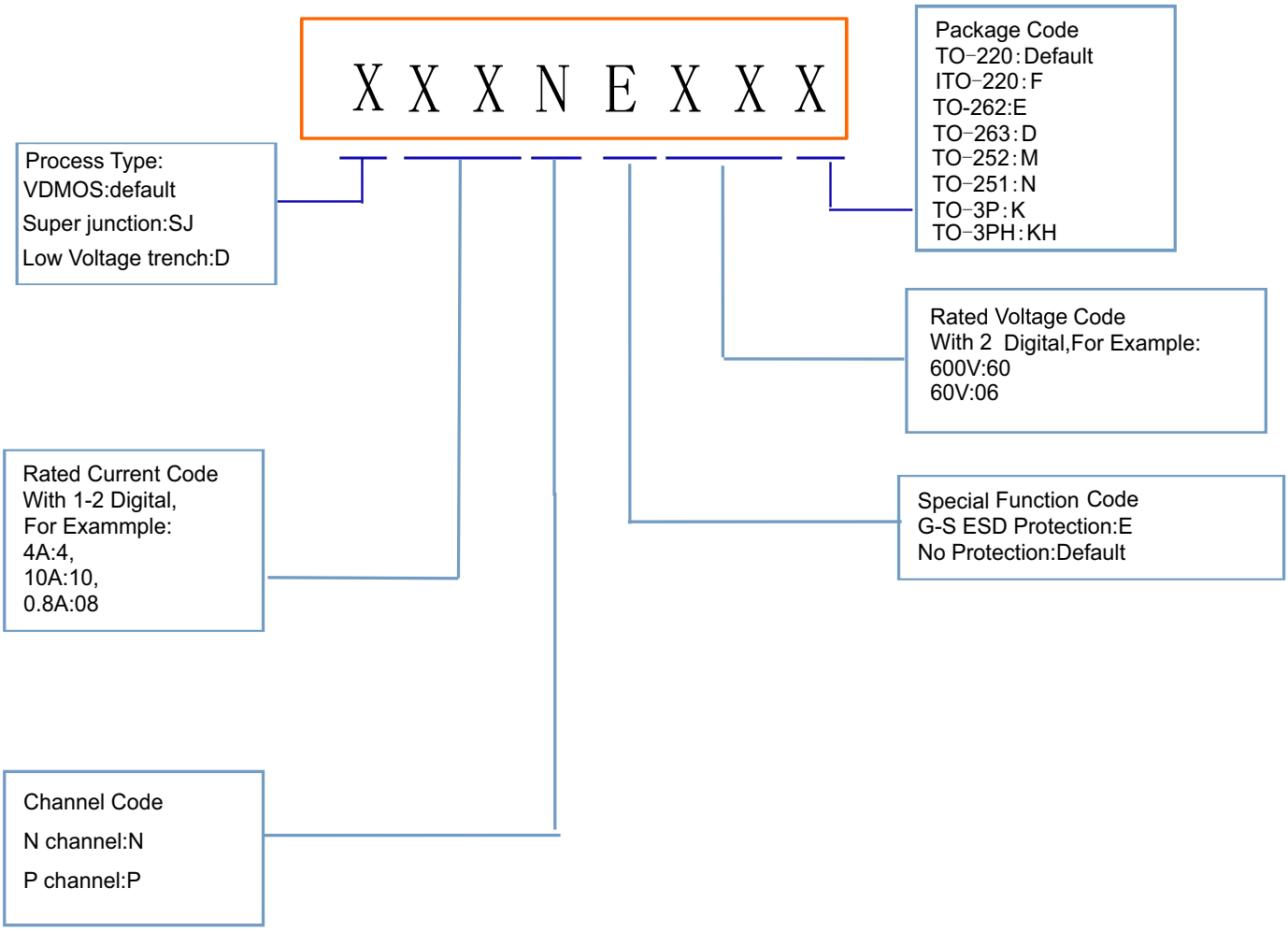
7) . Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

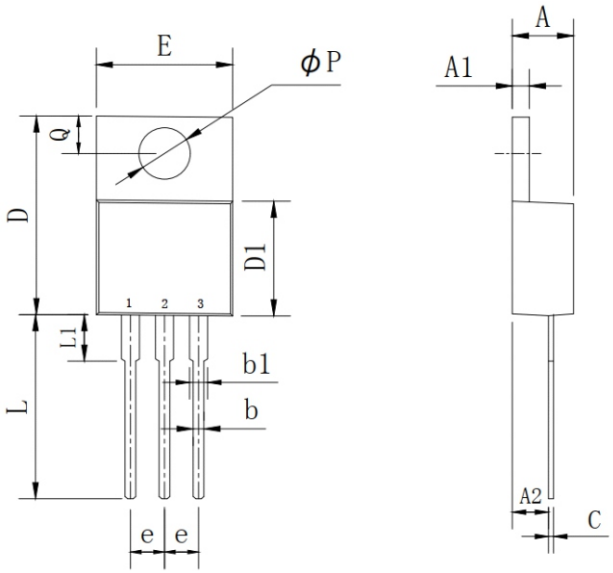
8) Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-220 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	4.25	4.87	0.167	0.192
A1	1.07	1.47	0.042	0.058
A2	2.03	2.92	0.080	0.115
b	0.51	1.11	0.020	0.044
b1	0.97	1.6	0.038	0.063
C	0.3	0.7	0.012	0.028
D	14.6	15.9	0.575	0.626
D1	8.04	9.3	0.317	0.366
E	9.57	10.57	0.377	0.416
e	2.34	2.74	0.092	0.108
L	12.58	14.3	0.495	0.563
L1	2.8	4.2	0.110	0.165
P	3.4	4.14	0.134	0.163
Q	2.45	3	0.096	0.118

Friendship Reminder

■ JiNan JingHeng（hereinafter referred to as JH） reserves the right to make changes to this document and its products and specifications at anytime without notice.

■ Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

■ JH makes no warranty, representation or guarantee regarding the suitability ofi ts products for any particular purpose, nor does JH assume any liability for application assistance or customer product design.

■ JH does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

■ No license is granted by implication or otherwise under any intellectual property rights of JH.

■ JH's products are not authorized for use as critical components in life support devices or systems without express written approval of JH.