

Features

- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

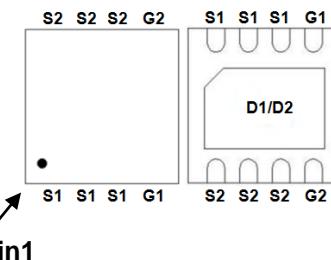
BVDSS	RDS(ON)	ID
12V	4.3mΩ	56A

General Description

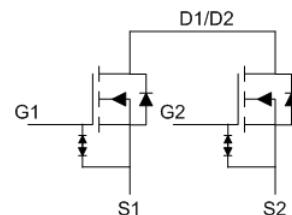
The JHQ1030 is the low RDS(ON) trenched N-CH MOSFETs with robust ESD protection. This product is suitable for Lithium-ion battery pack applications.

The JHQ1030 meet the RoHS and Green Product requirement with full function reliability approved.

DFN3x3 Pin Configuration



Pin1



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	12	V
V _{GS}	Gate-Source Voltage	±8	V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	56	A
I _D @T _c =100°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	35.6	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	19	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 4.5V ¹	15	A
I _{DM}	Pulsed Drain Current ²	100	A
P _D @T _c =25°C	Total Power Dissipation ¹	31	W
P _D @T _A =25°C	Total Power Dissipation ¹	3.6	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	35	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	4	°C/W

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	12	---	---	V
$\text{R}_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=3\text{A}$	2.3	3.3	4.3	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.0\text{V}, \text{I}_D=3\text{A}$	2.4	3.4	4.4	
		$\text{V}_{\text{GS}}=3.1\text{V}, \text{I}_D=3\text{A}$	2.6	3.6	4.7	
		$\text{V}_{\text{GS}}=2.5\text{V}, \text{I}_D=3\text{A}$	3	4	5.6	
		$\text{V}_{\text{GS}}=1.8\text{V}, \text{I}_D=3\text{A}$	4	5.4	7.6	
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{GS}}=\text{V}_{\text{DS}}, \text{I}_D=250\mu\text{A}$	0.4	0.6	1.0	V
I_{DSS}	Drain-Source Leakage Current	$\text{V}_{\text{DS}}=12\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=25^{\circ}\text{C}$	---	---	1	uA
		$\text{V}_{\text{DS}}=12\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{GS}}=\pm 8\text{V}, \text{V}_{\text{DS}}=0\text{V}$	---	---	± 10	uA
gfs	Forward Transconductance	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=3\text{A}$	---	42	---	S
Q_g	Total Gate Charge (4.5V)	$\text{V}_{\text{DS}}=10\text{V}, \text{I}_D=3\text{A}$	---	38	---	nC
	Total Gate Charge (3.9V)		---	33	---	
Q_{gs}	Gate-Source Charge		---	4.5	---	
Q_{gd}	Gate-Drain Charge		---	12	---	
$\text{T}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=10\text{V}, \text{V}_{\text{GS}}=4.5\text{V}, \text{R}_G=6\Omega$	---	22	---	ns
T_r	Rise Time		---	41	---	
$\text{T}_{\text{d(off)}}$	Turn-Off Delay Time		---	77	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=10\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{f}=1\text{MHz}$	---	3165	---	pF
C_{oss}	Output Capacitance		---	380	---	
C_{rss}	Reverse Transfer Capacitance		---	325	---	

Diode Characteristics

I_s	Continuous Source Current ¹	$\text{V}_G=\text{V}_D=0\text{V}, \text{Force Current}$	---	---	30	A
I_{SM}	Pulsed Source Current ²		---	---	100	A
V_{SD}	Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_s=3\text{A}, \text{T}_J=25^{\circ}\text{C}$		---	1.2	V

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t \leq 10\text{s}$.

2.The data tested by pulsed , pulse width $\leq 10\text{us}$, duty cycle $\leq 1\%$

Typical Characteristics

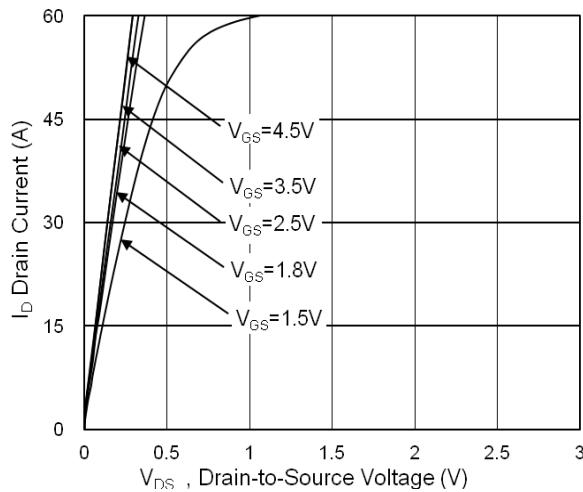


Fig.1 Typical Output Characteristics

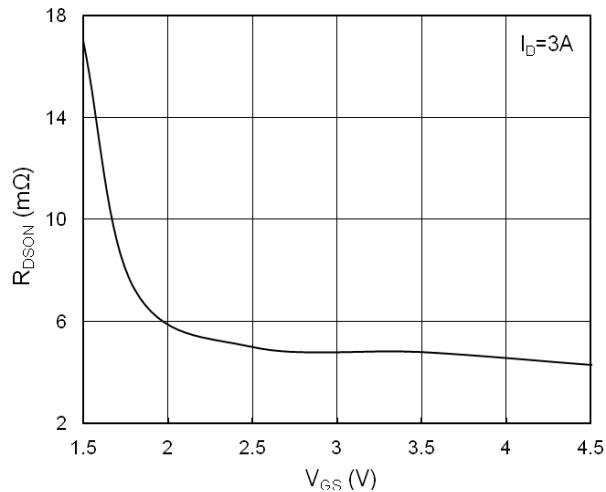


Fig.2 On-Resistance vs. Gate-Source Voltage

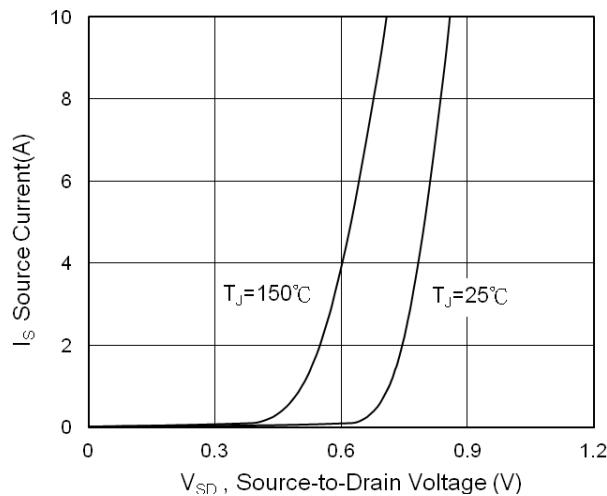


Fig.3 Source Drain Forward Characteristics

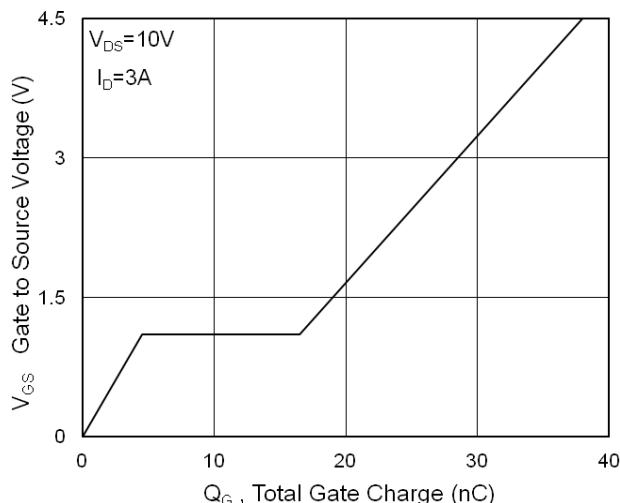


Fig.4 Gate-Charge Characteristics

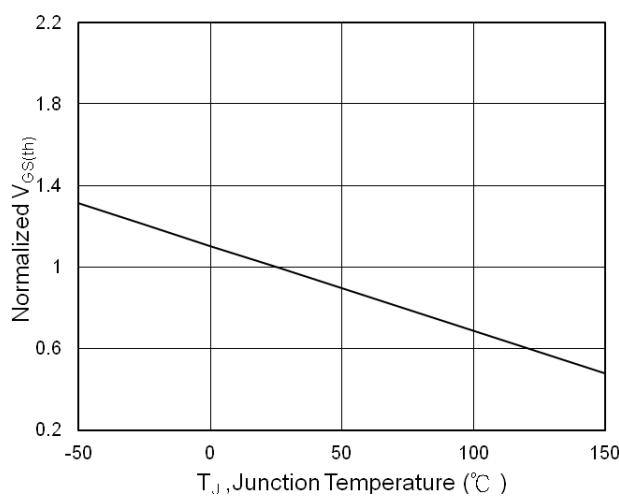


Fig.5 $V_{GS(th)}$ vs. T_J

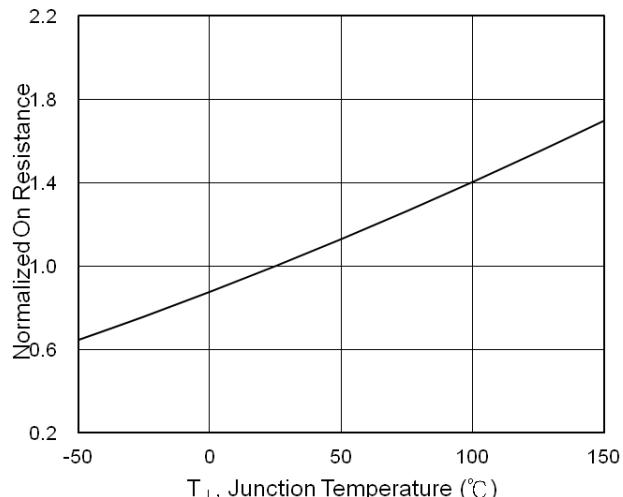
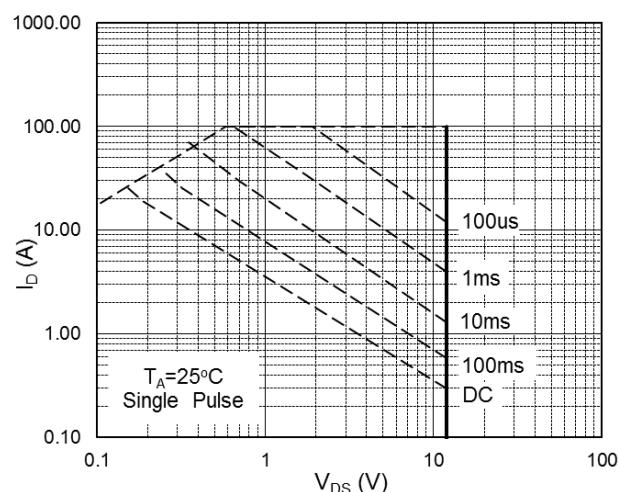
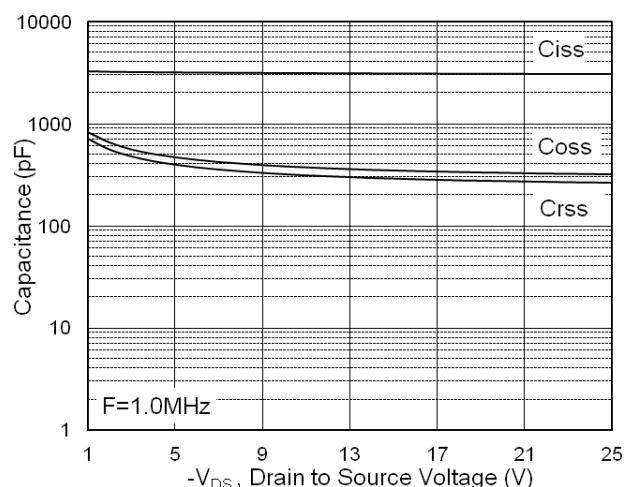
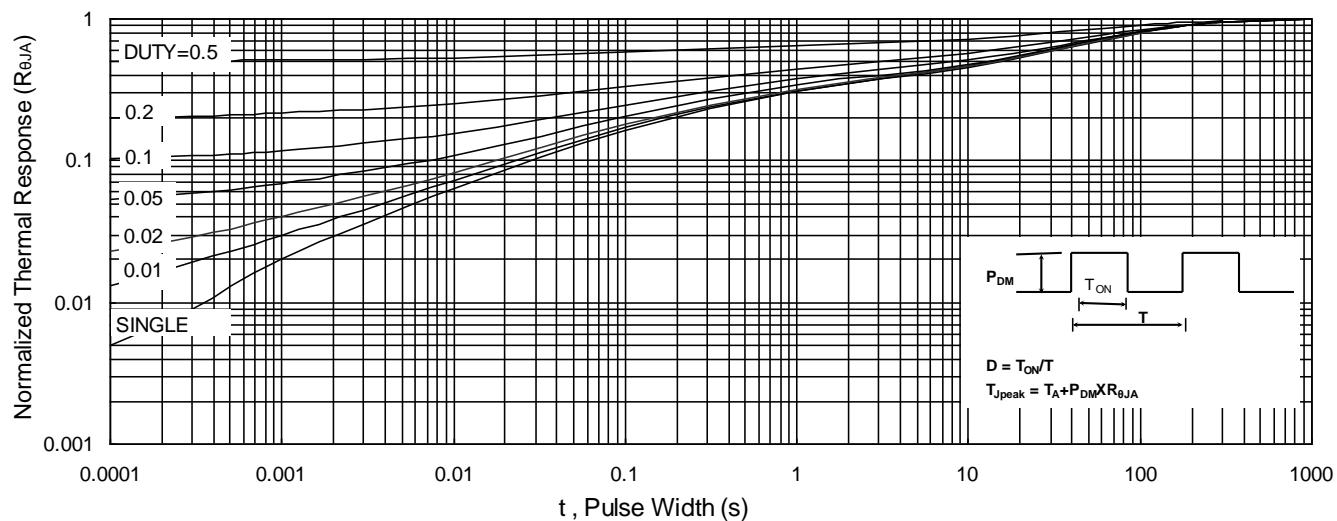
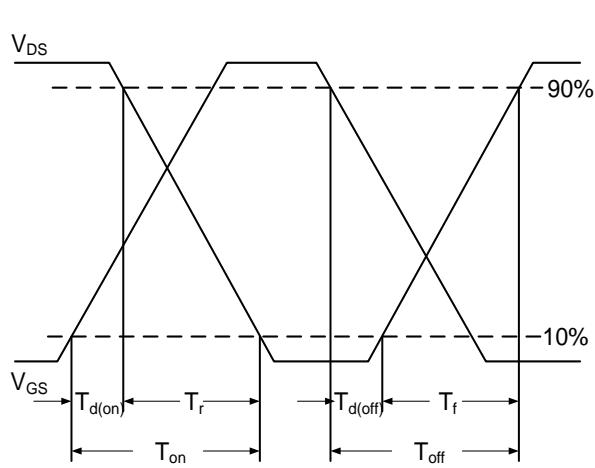
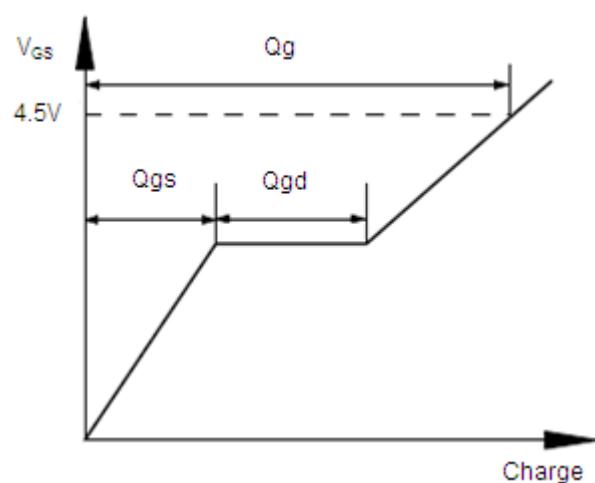
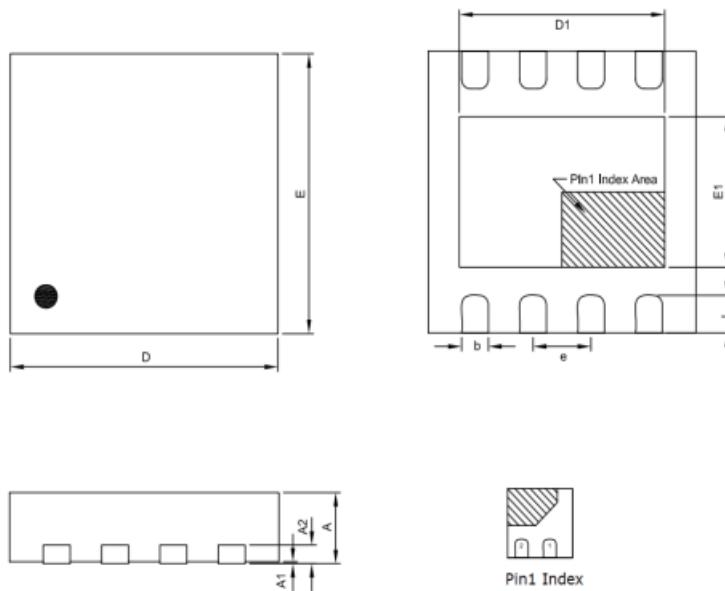


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

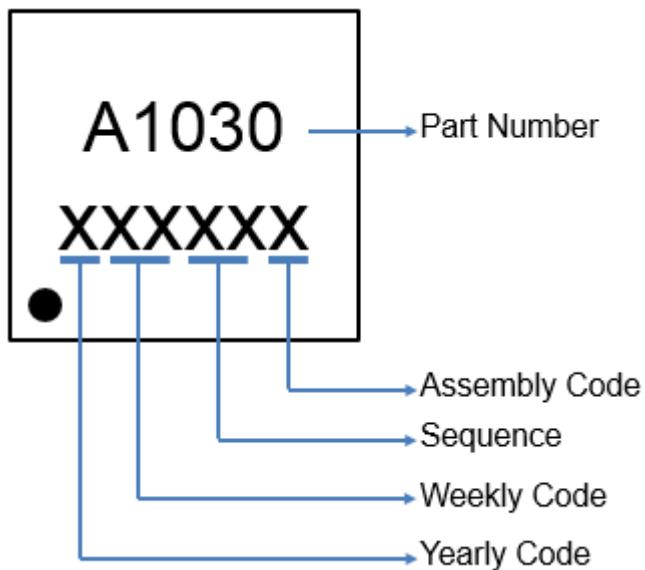

Fig.7 Safe Operating Area

Fig.8 Capacitance

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform

DFN3x3 Package Outline Dimensions

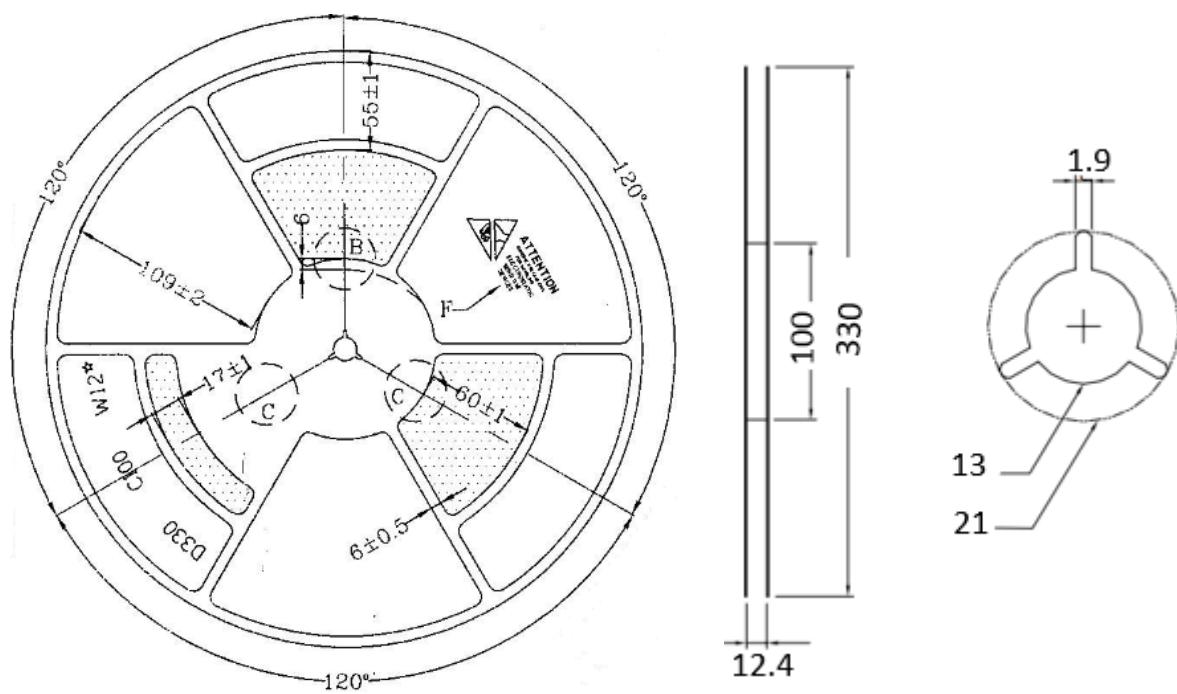
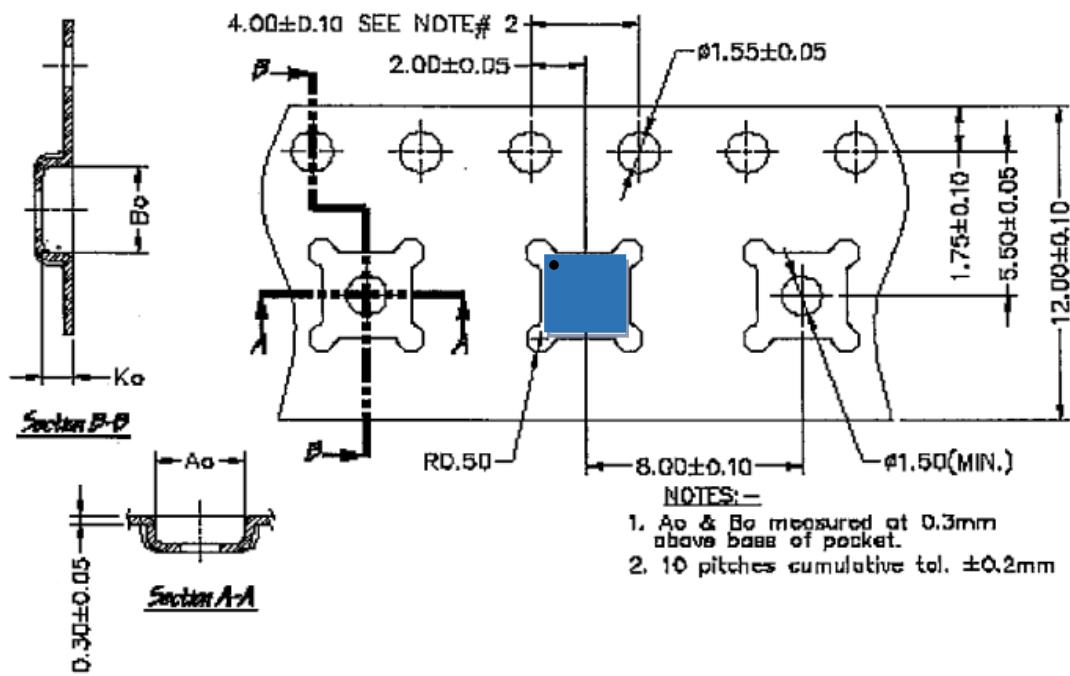


SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	--	0.05	0.000	--	0.002
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.25	2.30	2.35	0.0886	0.0906	0.0925
E1	1.55	1.6	1.65	0.061	0.063	0.065
L	0.35	0.40	0.45	0.0138	0.0177	0.0207
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	--	0.65	--	--	0.0256	--

Marking Instruction



DFN3x3 Tape and Reel Data



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