SEMICONDUCTOR

30N60P

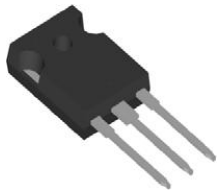
Silicon N-Channel Power MOSFET

Genaral Description

30N60P the silicon N-channel Enhanced VDMOSFET,is obtained by the self-aligned planar Technology which reduce the conduction loss，improve switching performance and enhance the avalanche energy.The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.which accords with the RoHS standard.

Product Summary			
V_{DS}	$R_{DS(on)}$ (Ω) Typ	I_D (A)	Qg (Typ)
600V	0.21 @ 10V	30	64nc

TO-247



Features

- Fast switching
- Low Gate Charge
- Low on resistance
- Excellent avalanche characteristics

Mechanical Data

- Case:TO-247 Package

Application

- Power switch circuit of adaptor and charger.

Pin Definition:

1. Gate
2. Drain
3. Source

Block Diagram

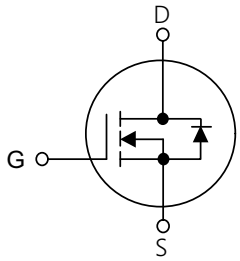


Table1 Absolute Maximum Ratings (Tc=25°C, unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	Tc=25°C	I_D	30	A
	Tc=100°C		15.7	
Pulsed Drain Current (Note 1)		I_{DM}	100	A
Single Pulse Avalanche Energy(Note 2)		E_{AS}	1500	mJ
Power Dissipation Tc=25°C		P_D	300	W
Operating Junction and Storage Temperature		T_J/T_{STG}	-55 ~ +150	°C

Table 2.Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal resistance Junction to Case	$R_{\theta JC}$	0.42	°C/W

Table 3. Electrical Characteristics (T_J=25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Off Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	600			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=600V,V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V			-100	nA
On Characteristics(Note 4)							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250mA	2		4	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V,I_D=15A		0.21	0.27	Ω
Dynamic Characteristics(Note 5)							
Input Capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHz		3487		pF
Output Capacitance		Coss			214		pF
Reverse Transfer Capacitance		C_{rss}			10		pF
Switching Characteristics (Note 5)							
Turn-On Delay Time		td(on)	V_{DD}=250V,I_D=30A, V_{GS}=10V,R_G=10Ω		37.2		ns
Turn-On Rise Time		t_R			64.4		ns
Turn-Off Delay Time		td(off)			86.8		ns
Turn-Off Fall Time		tf			46		ns
Total Gate Charge		Q_G	V_{DD}=400V,I_D=30A, V_{GS}=10V		64		nC
Gate-Source Charge		Q_{GS}			17		nC
Gate-Drain Charge		Q_{GD}			23		nC
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_S=30A			1.5	V
Maximum Continuous Drain-Source Diode Forward Current		I_S			30		A
Reverse Recovery Time		trr	V_{GS}=0V, I_S=30A dI_F/dt=100A/μs（Note 1）		490		ns
Reverse Recovery Charge		Q_{RR}			6246		nC

Notes：1 Repetitive Rating:Pulse width limited by maximum junction temperature
2 L=10mH, I_D=17.3A,Starting T_J=25°C
3 I_{SD}=30A,di/dt≤100A/μS,V_{DD}≤BV_{DSS},starting T_J=25℃
4 Pulse Test: Pulse width ≤300μS, Duty cycle≤2%
5 Guaranteed by design,not subject to production

Typical Characteristics Diagrams

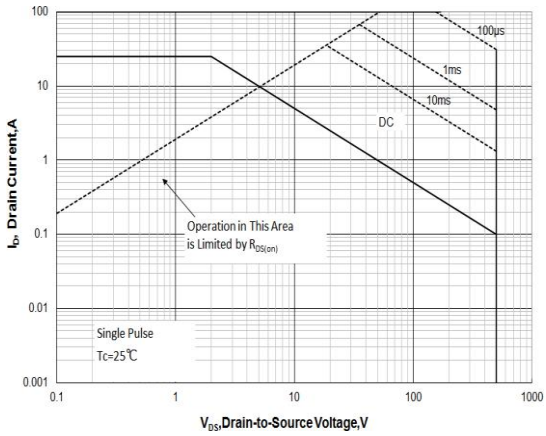


Figure 1 Maximum Forward Bias Safe Operating Area

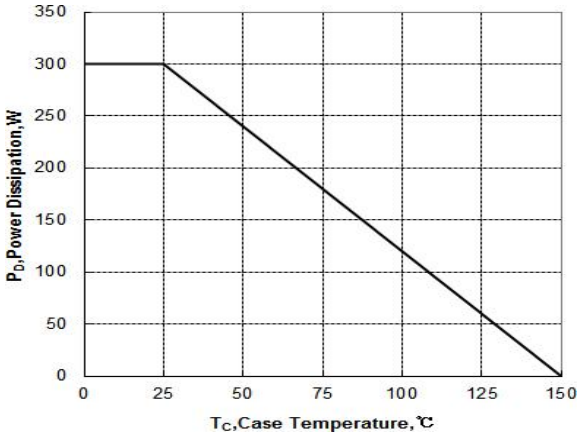


Figure 2 Maximum Power dissipation vs Case Temperature

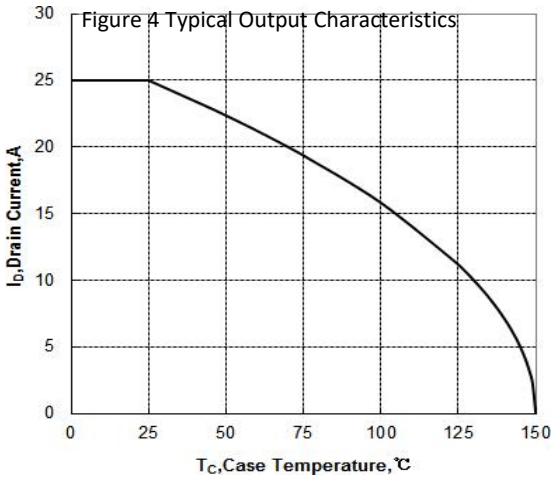


Figure 3 Maximum Continuous Drain Current vs Case Temperature

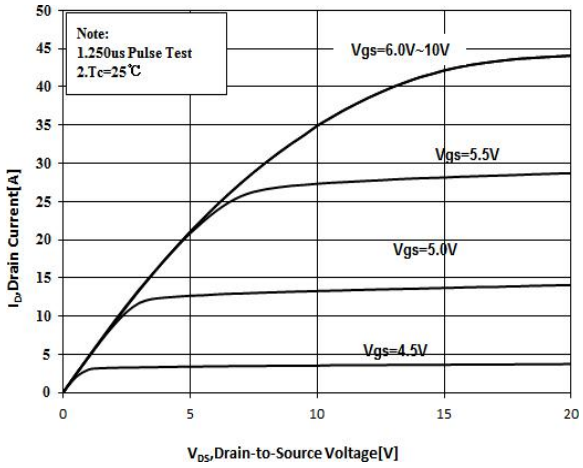


Figure 4 Typical Output Characteristics

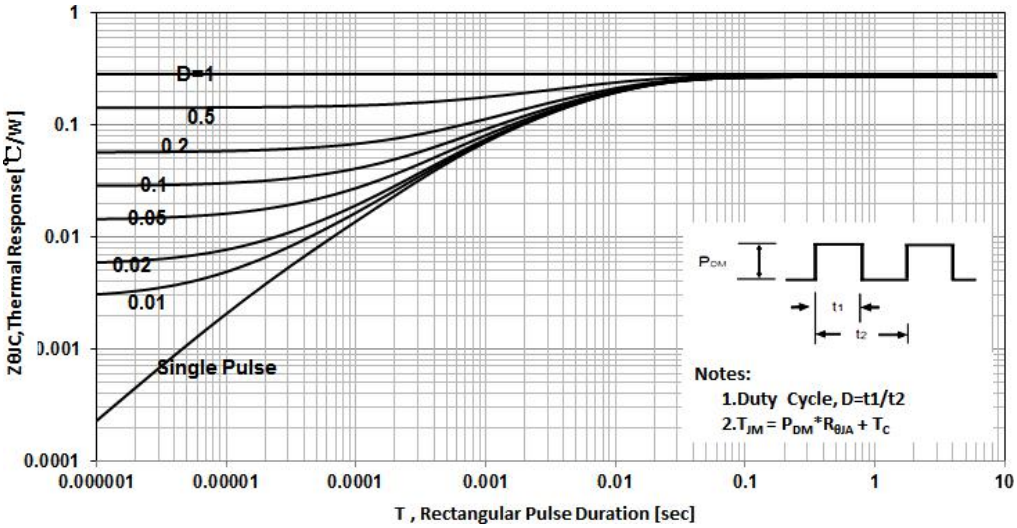


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

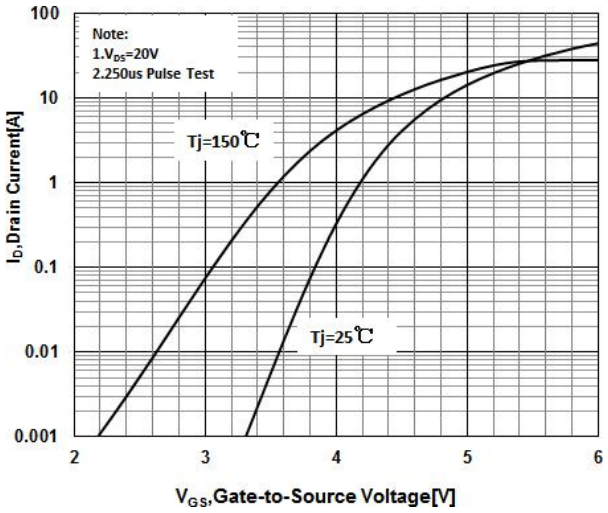


Figure 6 Typical Transfer Characteristics

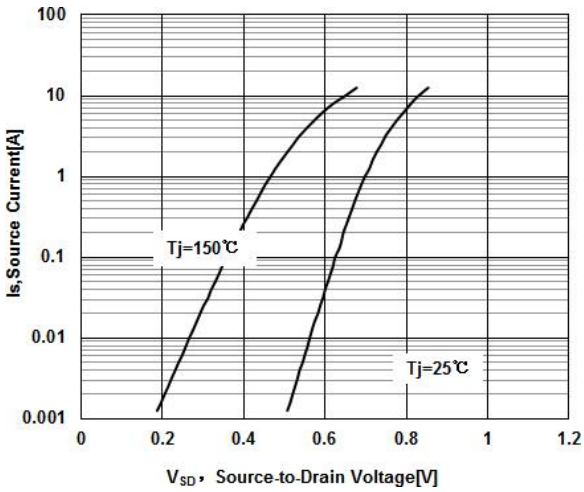


Figure 7 Typical Body Diode Transfer Characteristics

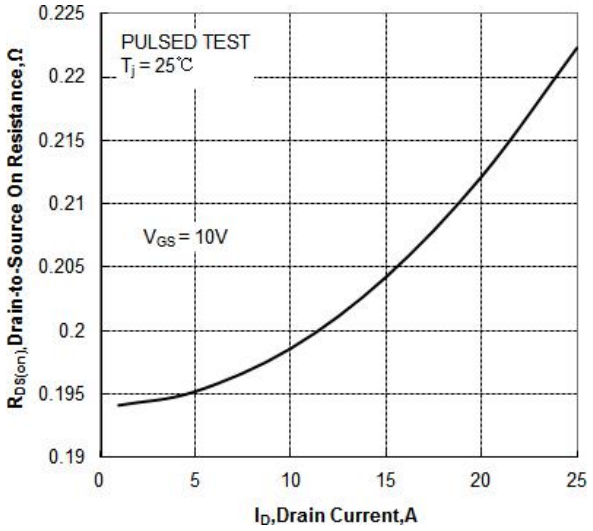


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

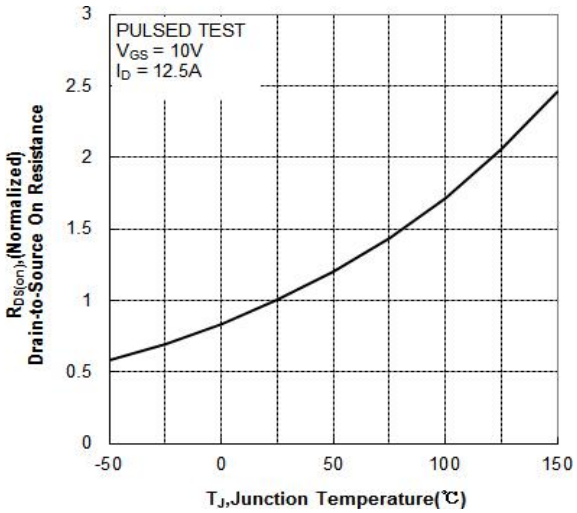


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

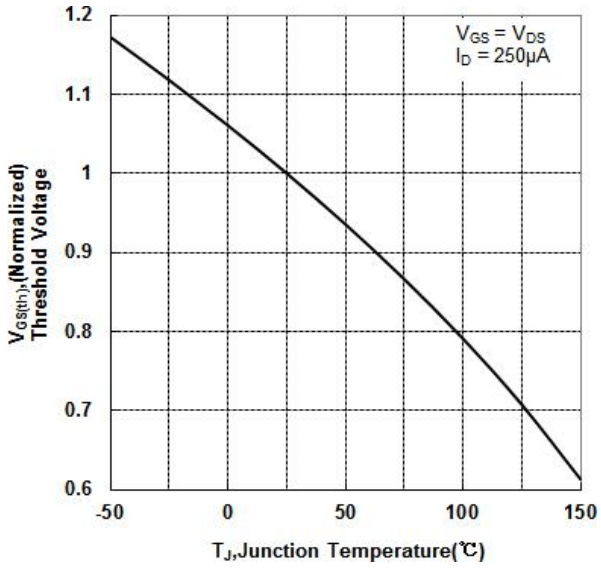


Figure 10 Typical Theshold Voltage vs Junction Temperature

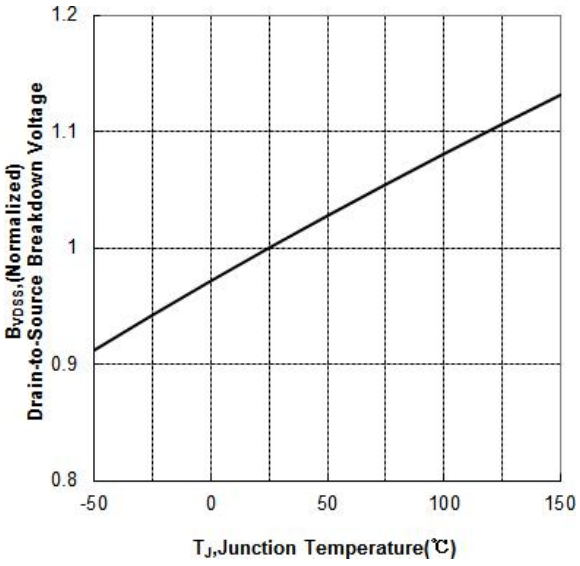


Figure 11 Typical Breakdown Voltage vs Junction Temperature

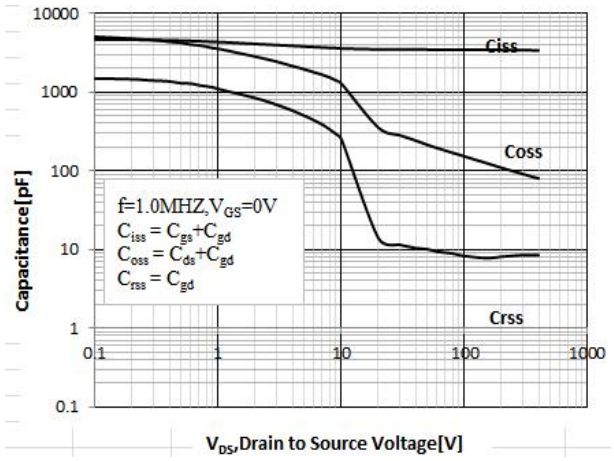


Figure 12 Typical Capacitance vs Drain to Source Voltage

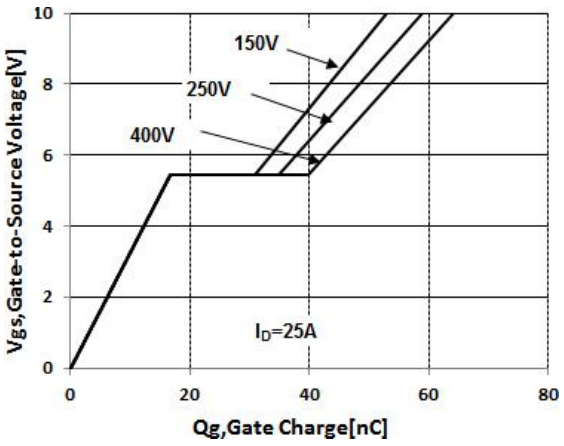


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Typical Test Circuit

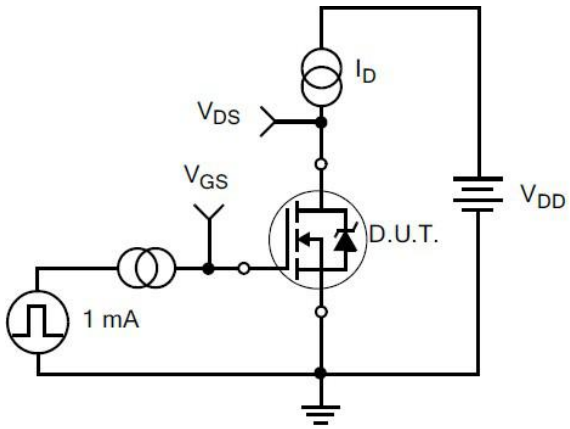


Figure 17. Gate Charge Test Circuit

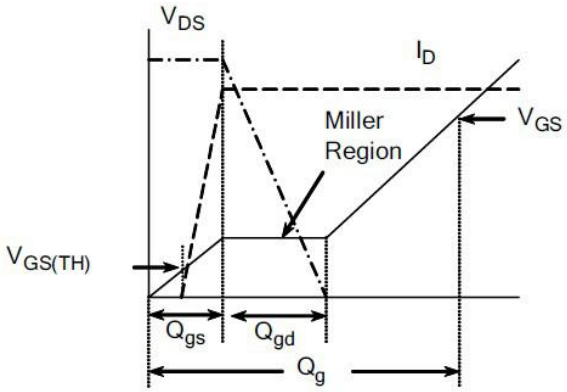


Figure 18. Gate Charge Waveform

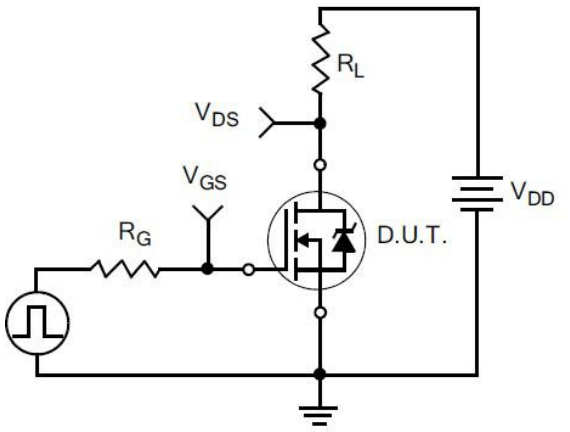


Figure 19. Resistive Switching Test Circuit

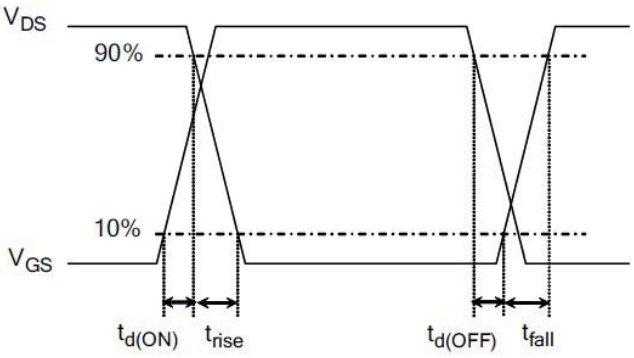


Figure 20. Resistive Switching Waveforms

Typical Test Circuit

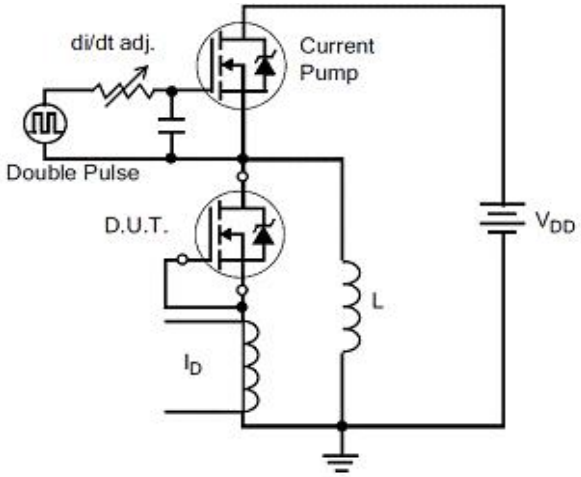


Figure 21. Diode Reverse Recovery Test Circuit

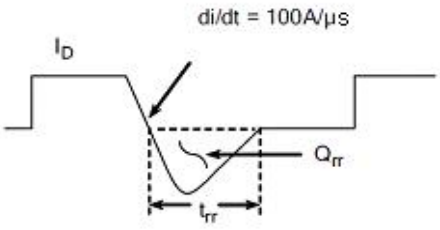


Figure 22. Diode Reverse Recovery Waveform

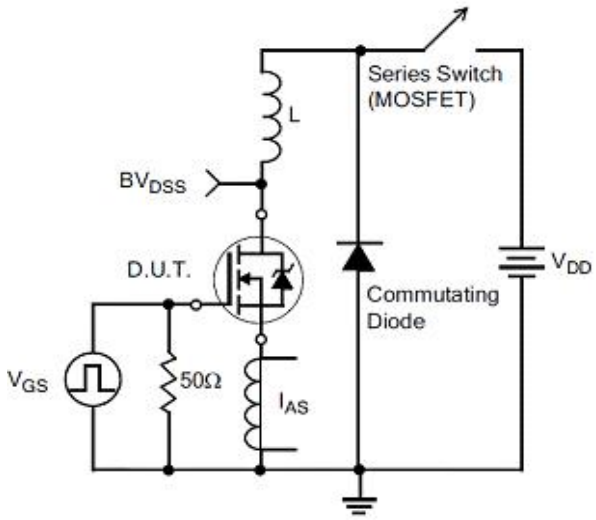
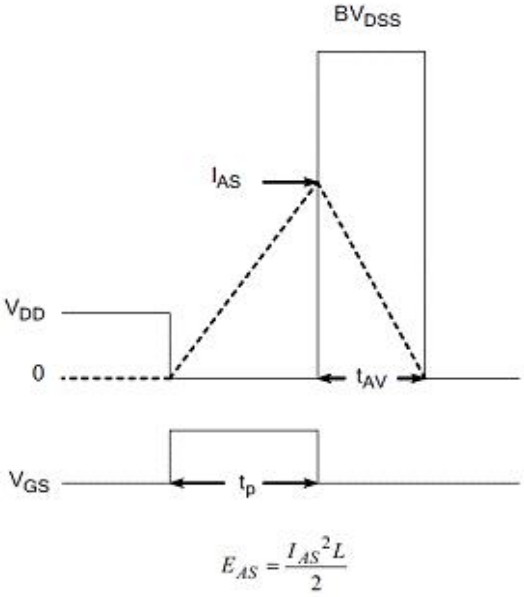


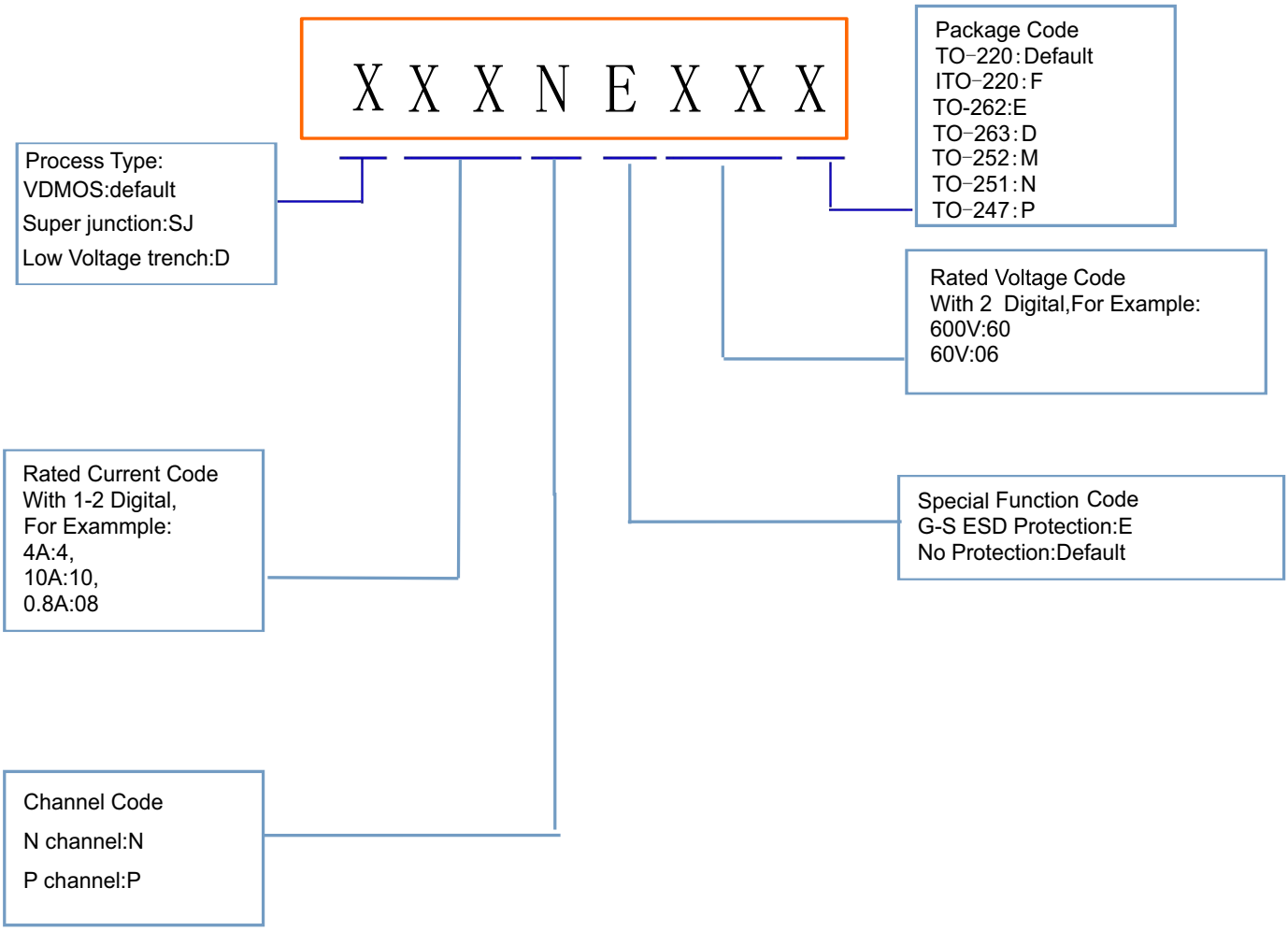
Figure 23. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

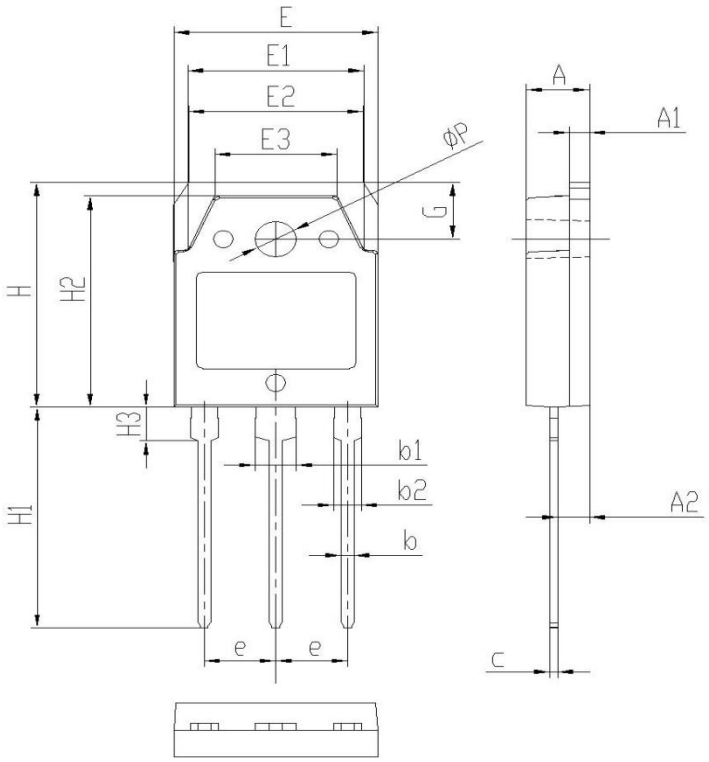
Figure 24. Unclamped Inductive Switching Waveforms

Product Names Rules



Dimensions

TO-3P PACKAGE



Symbol	UNIT mm		
	Min	**Typ**	Max
A	4.60	4.80	5.00
A1	1.3	1.5	1.7
A2	2.20	2.40	2.60
b	0.80	1.0	1.20
b1	2.90	3.10	3.30
b2	1.80	2.00	2.20
c	0.50	0.60	0.70
e	5.25	5.45	5.65
E	15.2	15.6	16.0
E1	13.2	13.4	13.6
E2	15.1	15.3	16.5
E3	9.1	9.3	9.5
H	19.8	20.0	20.2
H1	19.0	19.5	20.0
H2	18.3	18.5	18.7
H3	2.8	3.0	3.2
G	4.8	5.0	5.2
ΦP	3.00	3.20	3.40

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